Experiment No. 5

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Branch: CSE-AI/ML **Section/Group: 109-B**
Semester: II **Date of Performance: March 18, 2023**
Subject Name: Digital Electronics **Subject Code: 22ECH-101**

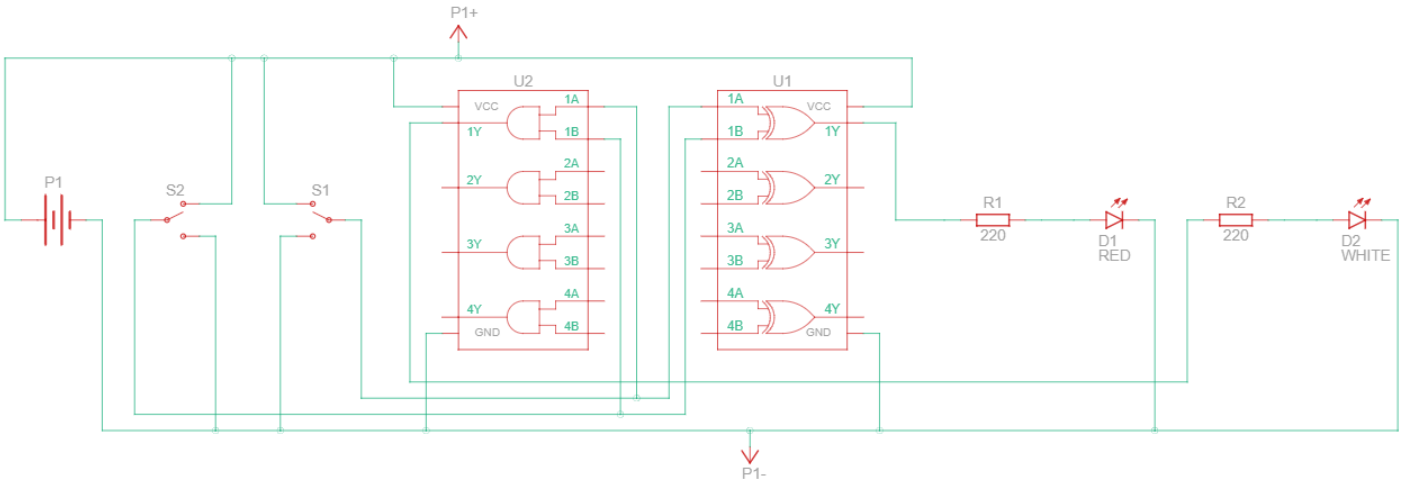
1. Aim: To Design and Verify the operation of Half Adder and Full Adder

2. Requirements :

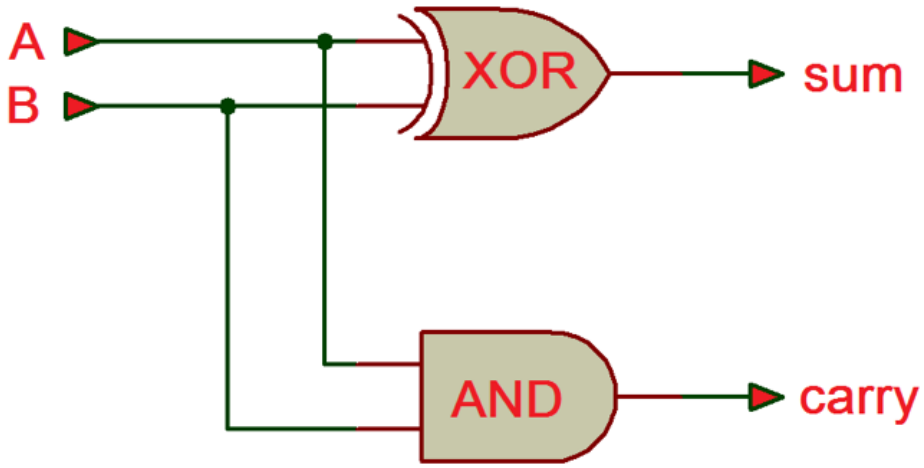
i. **Software :** TinkerCad
ii. **Hardware :** Breadboard, Connecting Wires, IC for 7408, 7432, 7486, Power Supply, Slideswitches , 220 ohm resistor, LED's.

3. Circuit Diagram:

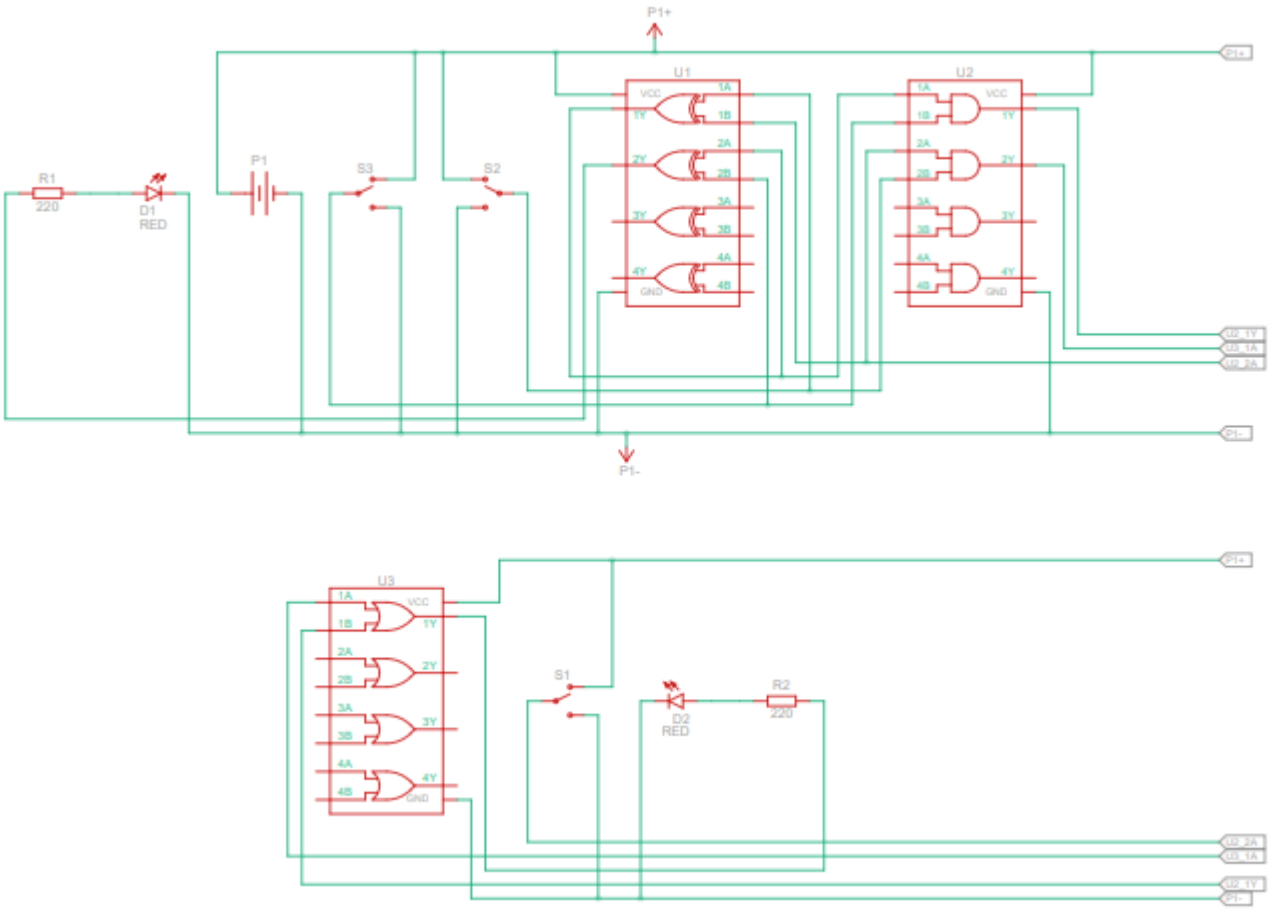
(a) Schematic Diagram for Half Adder :



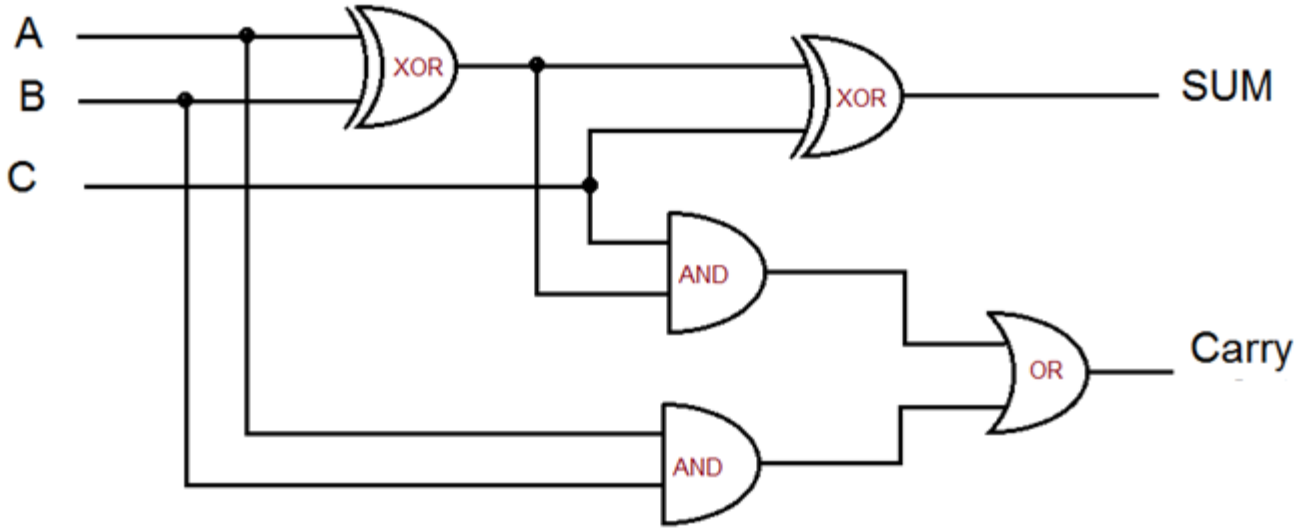
(b) Circuit Diagram for Half Adder :



(c) Schematic Diagram for Full Adder :



(d) Circuit Diagram for Full Adder :



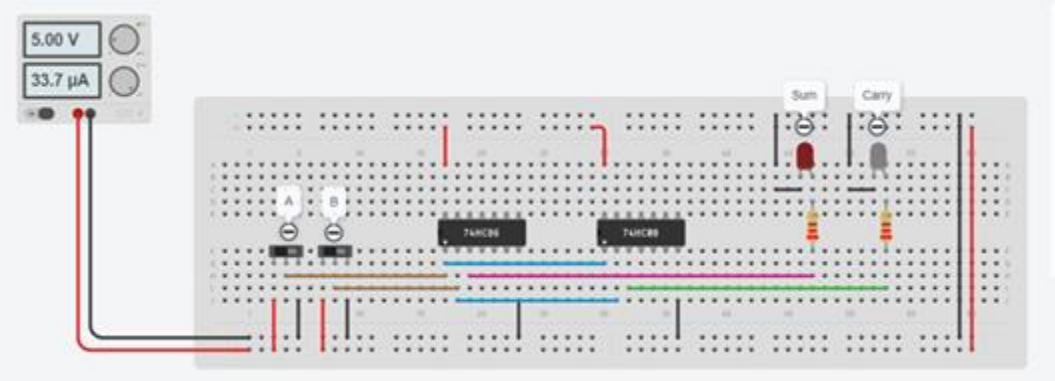
4. Simulation Results

(a.) Half Adder : A combinational logic circuit that performs the addition of two data bits, A and B, is called a half-adder. Addition will result in two output bits; one of which is the sum bit, S, and the other is the carry bit, C. The Boolean functions describing the half-adder are:

Sum = A XOR B

Carry = AB

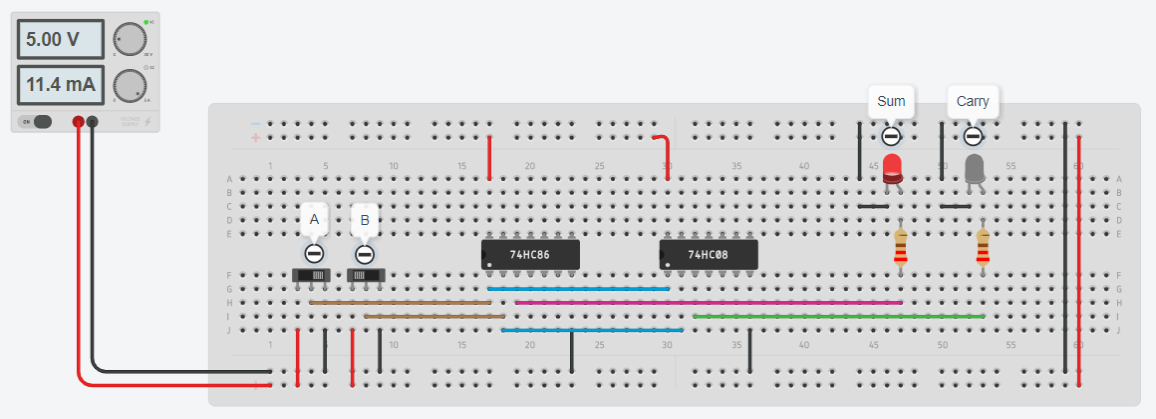
(i.) When A = 0 & B = 0



Truth Table :-

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

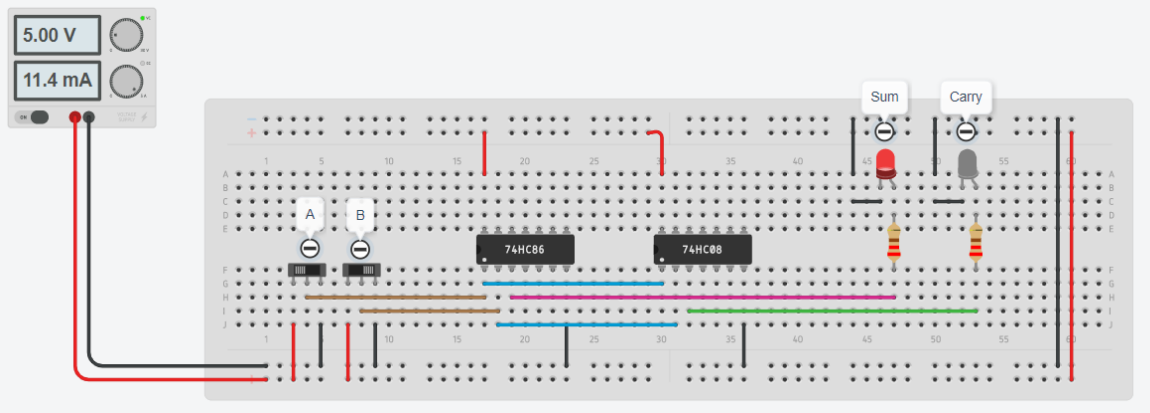
(ii.) When A = 0 & B = 1



Truth Table :-

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

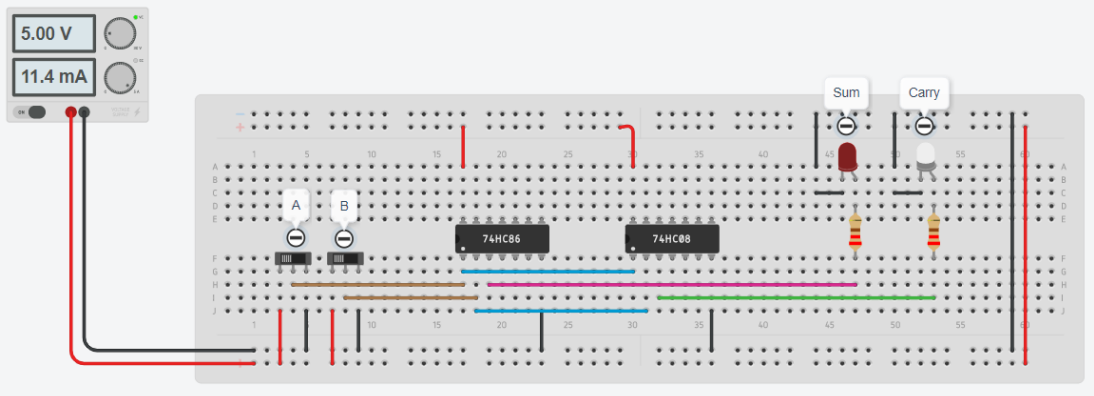
(iii.) When A = 1 & B = 0



Truth Table :-

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

(iv.) When A = 1 & B = 1



Truth Table :-

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Truth Table :-

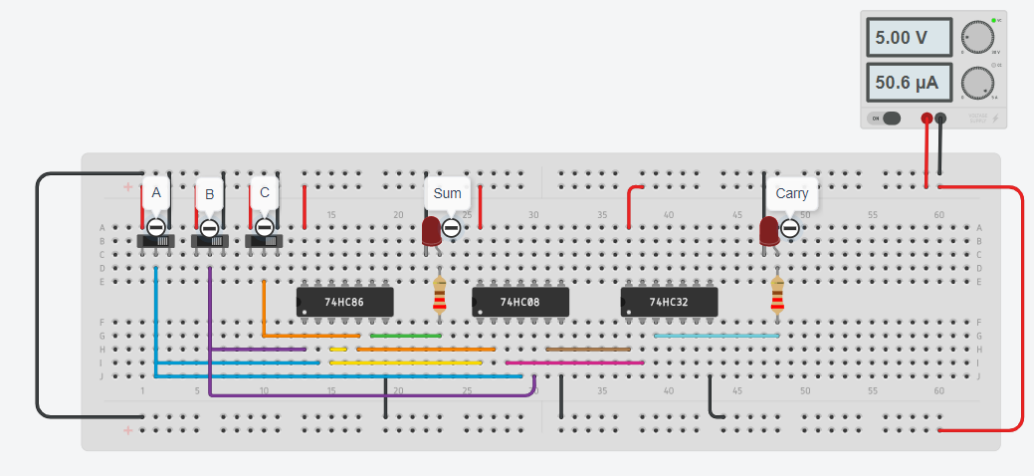
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

(b.) Full Adder : The Half Adder does not take the carry bit from its previous stage into account. This carry bit from its previous stage is called carry-in bit. A combinational logic circuit that adds the two data bits, A and B, and a carry-in bit, C is called a full-adder. The Boolean functions describing the Full Adder are:

Sum = (A XOR B) XOR C

Carry = AB + BC +AC

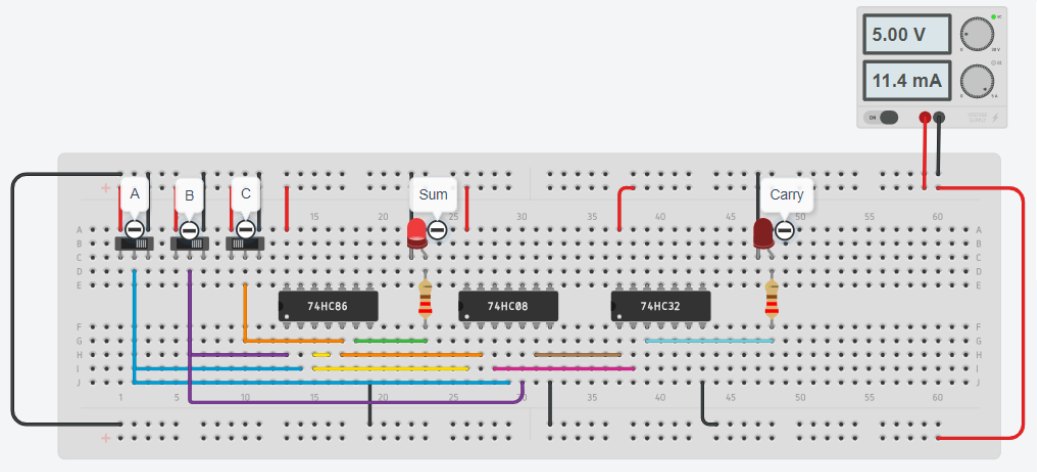
(i.) When A = 0, B = 0 & C = 0



Truth Table :-

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

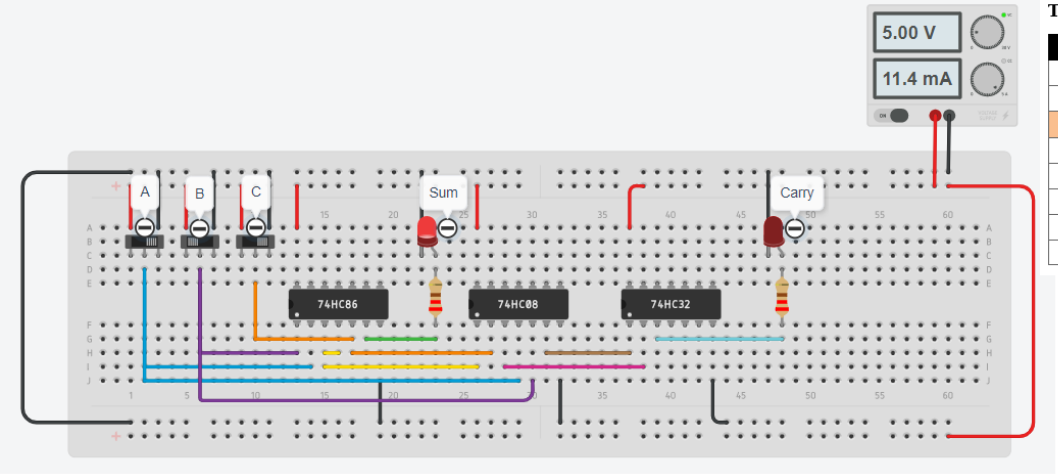
(ii.) When A,B = 0 & C = 1



Truth Table :-

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

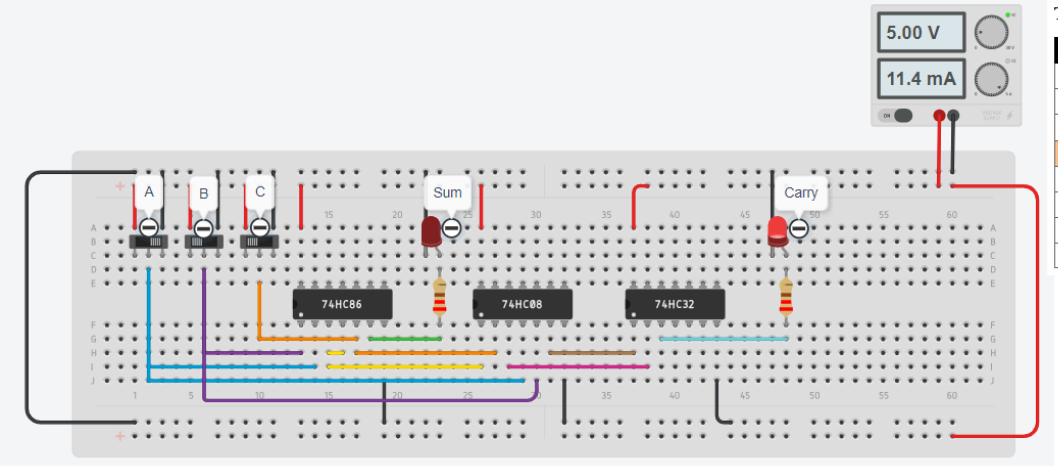
(iii.) When A,C = 0 & B = 1



Truth Table :-

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

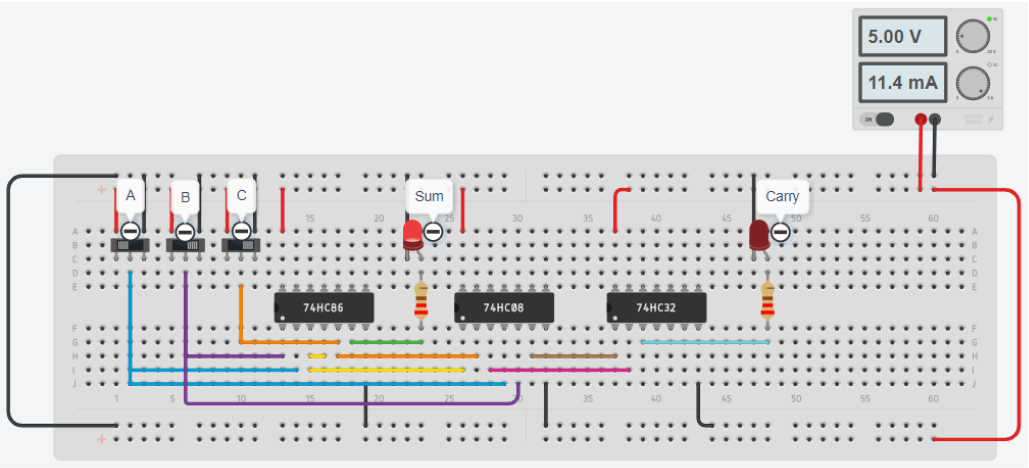
(iv.) When A = 0 & B,C = 1



Truth Table :-

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

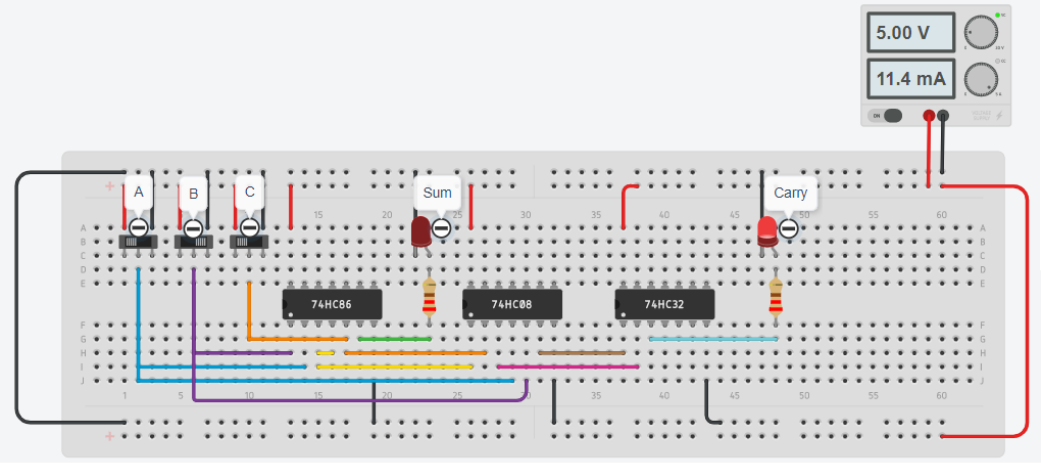
(v.) When A = 1 & B,C = 0



Truth Table :-

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

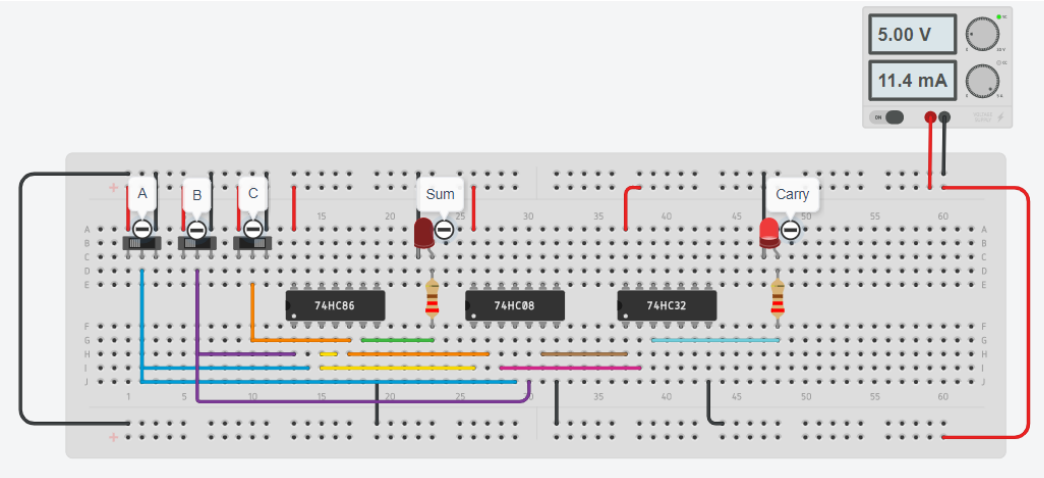
(vi.) When A,C = 1 & B = 0



Truth Table :-

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

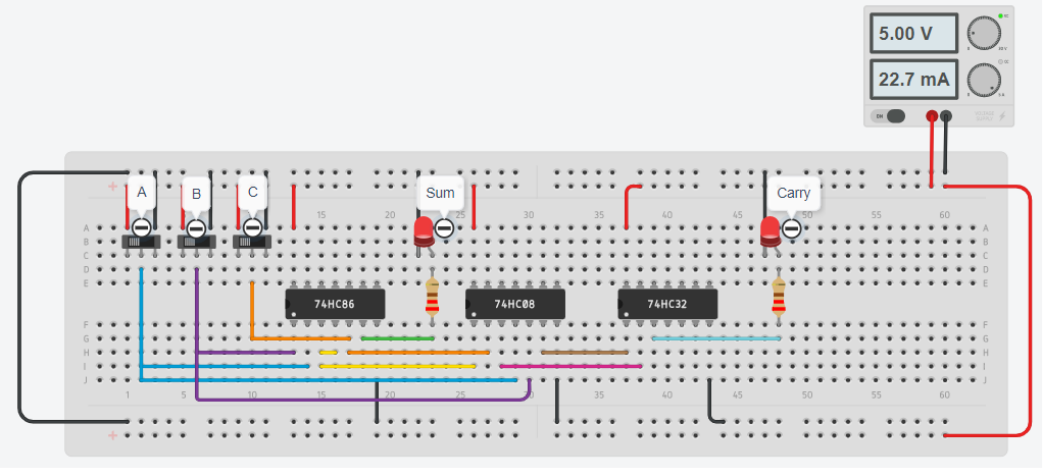
(vii.) When A,B = 1 & C = 0



Truth Table :-

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

(viii.) When A,B,C = 1



Truth Table :-

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Truth Table :-

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

5. Observations : Here are some observations for designing and verifying the operation of Half Adder and Full Adder:

1. **Half Adder:**

- A half adder is a digital circuit that adds two single-bit numbers and produces a two-bit output, which consists of the sum and carry.
- The circuit can be designed using XOR and AND gates. The XOR gate produces the sum while the AND gate produces the carry.
- The circuit can be tested using truth tables and by verifying the output using the logic equations derived from the design.

2. **Full Adder:**

- A full adder is a digital circuit that adds two single-bit numbers and a carry bit and produces a two-bit output, which consists of the sum and carry.
- The circuit can be designed using XOR, AND and OR gates. The XOR gates produce the sum, while the AND and OR gates produce the carry.
- The circuit can be tested using truth tables and by verifying the output using the logic equations derived from the design.

6. Troubleshooting:

1. Messy Circuit Connection & loose connection.

2. **Incorrect gate implementation:** Another error that can occur is when the gate is not implemented correctly. For example, if you are testing an AND gate and accidentally implement an OR gate instead, you will get incorrect results. Double-check your gate implementation to make sure it matches the logic symbol for the gate you are testing.

3. **Faulty equipment:** Finally, it's possible that the error is not related to the gate or the truth table, but rather to faulty equipment. Make sure that your testing equipment is working properly and is calibrated correctly.

7. Result: We have successfully Designed and Verified the operation of Half Adder and Full Adder**.**

Learning outcomes (What I have learnt):

1. Understanding the basic principles of binary addition and how it can be implemented using logic circuits.
2. Gaining knowledge about the design and operation of Half Adder and Full Adder circuits.
3. Learning how to use logic gates to implement Half Adder and Full Adder circuits.
4. Developing skills in verifying the functionality of Half Adder and Full Adder circuits through TinkerCad.

Evaluation Grid:

Sr. No.	Parameters	Marks Obtained	Maximum Marks
1.	Worksheet completion including writing learning objectives/Outcomes.(To be submitted at the end of the day).		12
2.	Viva		8
3.	Student Engagement in Simulation/Demonstration/Performance and Controls/Pre-Lab Questions.		10
	Signature of Faculty (with Date):	Total Marks Obtained:	