Experiment Title. 3

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Subject Name: Digital Electronics **Subject Code: 22ECH-101**

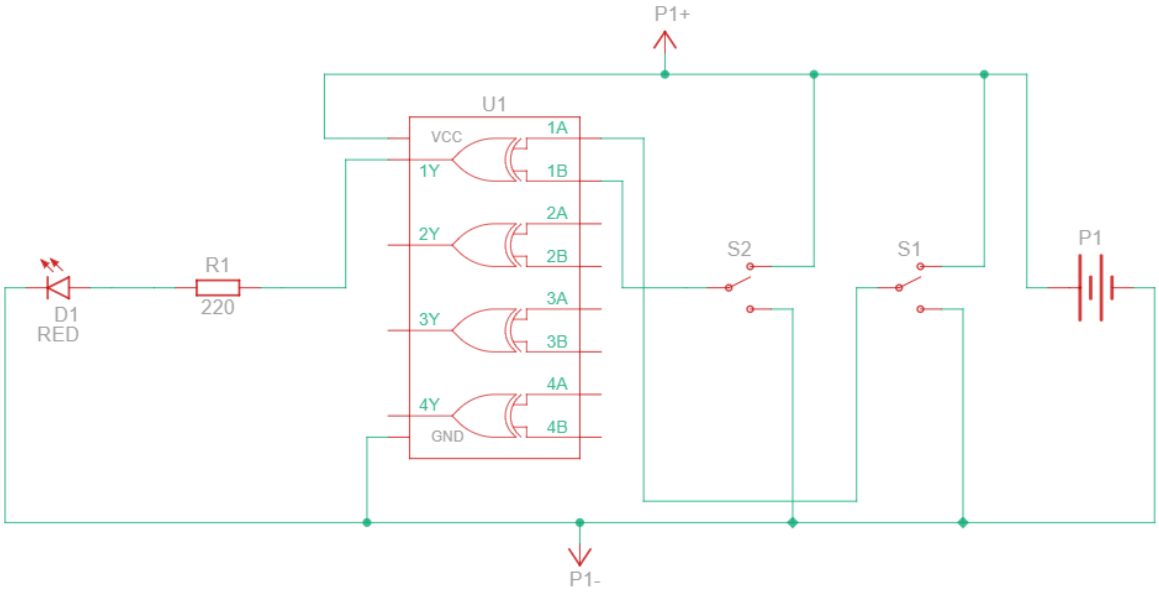
1. Aim: (a) Design a two – way switch for room light using XOR Gate.
(b) Design a multiplayer game trigger mechanism using NOR Gate.

2. Requirements :

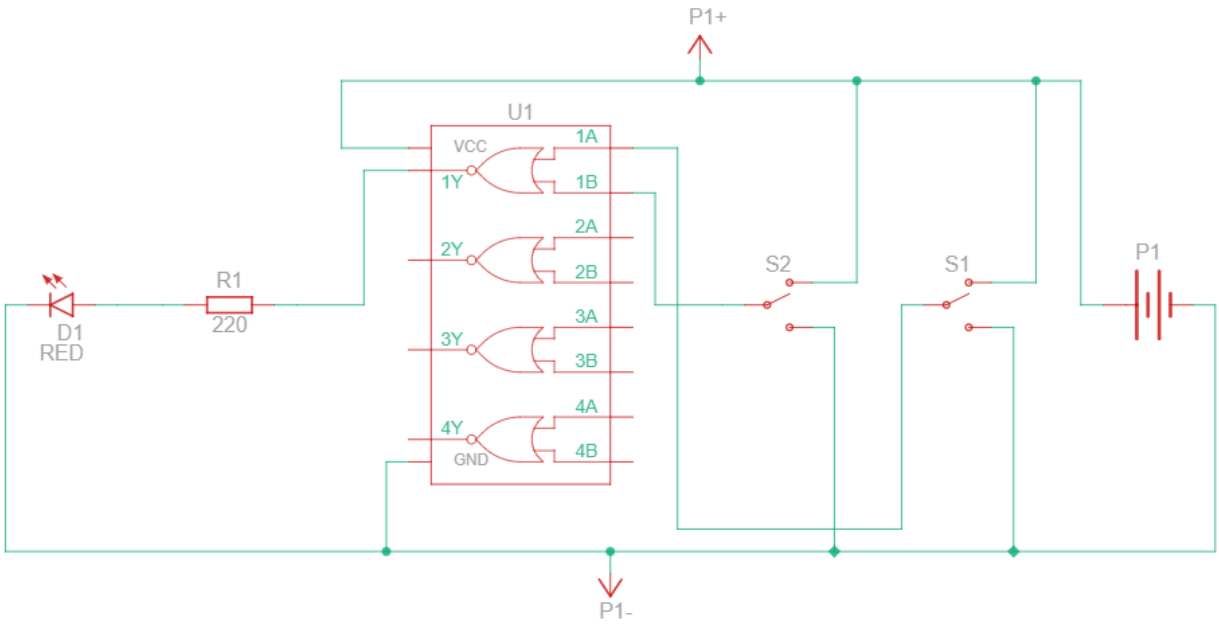
i. **Software :** TinkerCad
ii. **Hardware :** Breadboard, Connecting Wires, IC for 7402, 7486, Power Supply, 2 Slideswitch , 220 ohm resistor, LED.

3. Circuit Diagram:

(a) Schematic Diagram for XOR Gate :

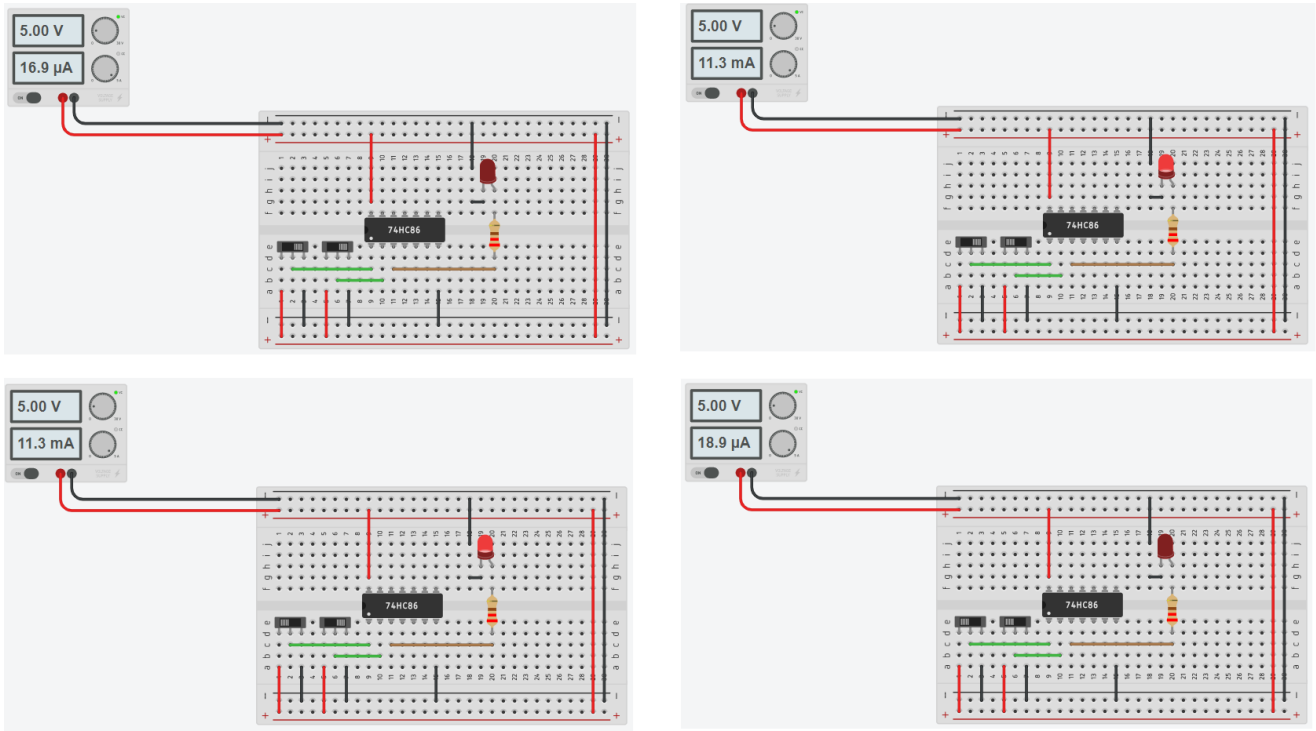


(b) Schematic Diagram for NOR Gate :

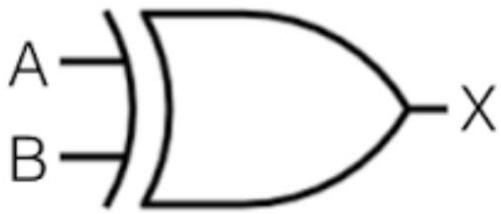


4. Simulation Results :

(a) XOR Gate



Concept Used : An XOR gate is a digital logic gate that performs a logical operation on two input signals. The output of an XOR gate is "true" or "1" only when exactly one of its inputs is "true" or "1". If both inputs are "true" or "false", the output is "false" or "0".
The symbol for XOR gate is shown below :



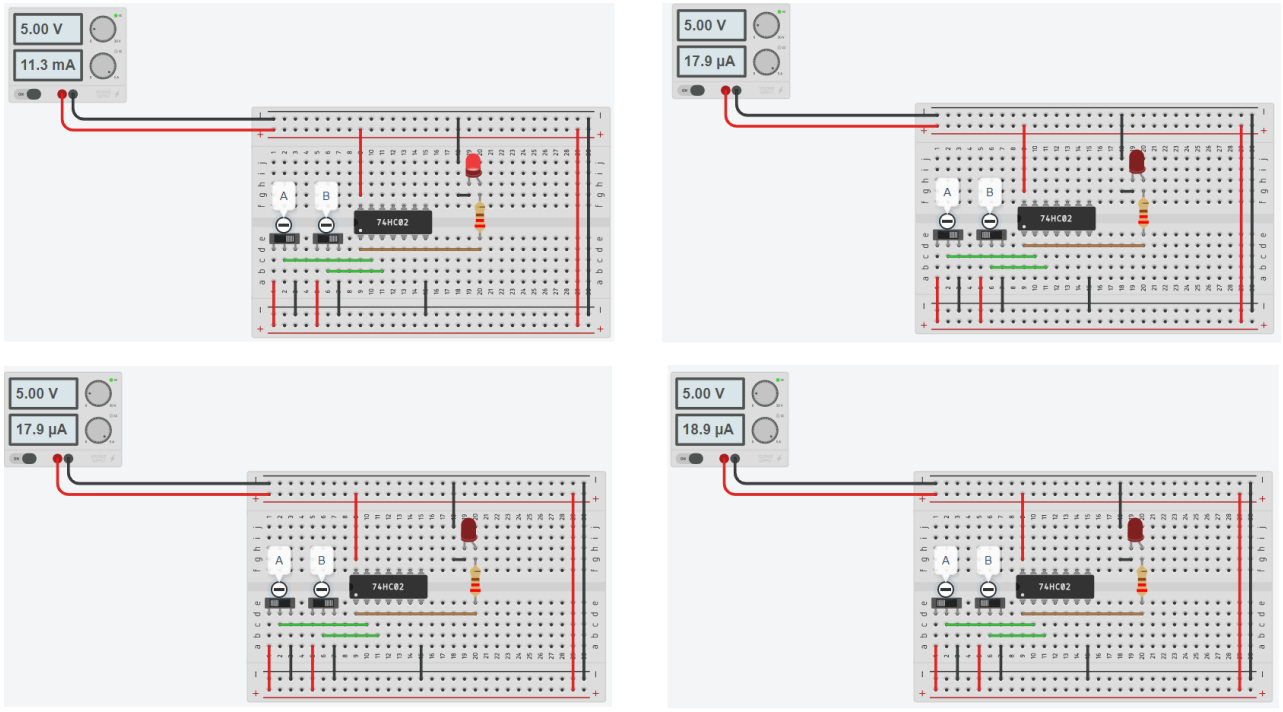
In simple terms, an XOR gate produces a "true" output if the input signals are different, and a "false" output if the input signals are the same.
The truth table for XOR gate is shown below :

Truth Table :

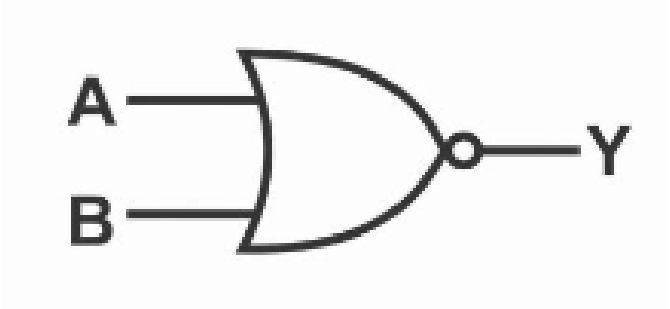
Inputs		Output
A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

This behaviour is useful in digital circuits for tasks such as error detection, data encryption, and switching between two inputs.

(b)NOR Gate



Concept Used : A NOR gate is a type of logic gate used in digital circuits. It takes in two inputs and produces a single output. The output of a NOR gate is "true" or "1" only when all of its inputs are "false" or "0".
The symbol for NOR gate is shown below :



A NOR gate is the opposite of an OR gate, where the output is “true” or “1” if any of the inputs are “true” or “1”.
The truth table for a NOR gate is as follows :

Truth Table :

Input		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

The output of a NOR gate is often used as an input to other logic gates in a digital circuit, and it is commonly used in circuits where it is necessary to determine if two or more conditions are false.

5. Observations : Here are some observations that can be made during this process:

1. **XOR gate:** The XOR gate produces an output of 1 only when its two inputs are different (i.e., one input is 1 and the other is 0). When both inputs are the same (i.e., both 0 or both 1), the output is 0. This behaviour is consistent with the XOR gate's truth table.
2. **NOR gate:** The NOR gate produces an output of 0 when one or both of its inputs are 1. It produces an output of 1 only when both inputs are 0. This behaviour is consistent with the NOR gate's truth table.

Observing and verifying the output behaviour of logic gates using their truth tables is an important step in digital electronics, as it helps ensure that the circuits are functioning as expected and that the logical operations are being carried out correctly.

6. Troubleshooting:

1. Messy Circuit Connection & loose connection.

2. **Incorrect gate implementation:** Another error that can occur is when the gate is not implemented correctly. For example, if you are testing an AND gate and accidentally implement an OR gate instead, you will get incorrect results. Double-check your gate implementation to make sure it matches the logic symbol for the gate you are testing.

3. **Faulty equipment:** Finally, it's possible that the error is not related to the gate or the truth table, but rather to faulty equipment. Make sure that your testing equipment is working properly and is calibrated correctly.

7. Result: The Practical application of XOR and NOR Gate were studied and implemented.

Learning outcomes (What I have learnt):

1. Understanding the concept of logic gates.

2. Identifying the logical function of a gate.

3. Evaluating the performance of a circuit.

4. Verifying the correctness of a gate.

Evaluation Grid:

Sr. No.	Parameters	Marks Obtained	Maximum Marks
1.	Worksheet completion including writing learning objectives/Outcomes.(To be submitted at the end of the day).		12
2.	Viva		8
3.	Student Engagement in Simulation/Demonstration/Performance and Controls/Pre-Lab Questions.		10
	Signature of Faculty (with Date):	Total Marks Obtained:	