Experiment No. 6

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Branch: CSE-AI/ML **Section/Group: 109-A**
Semester: II **Date of Performance: April 8, 2023**
Subject Name: Digital Electronics **Subject Code: 22ECH-101**

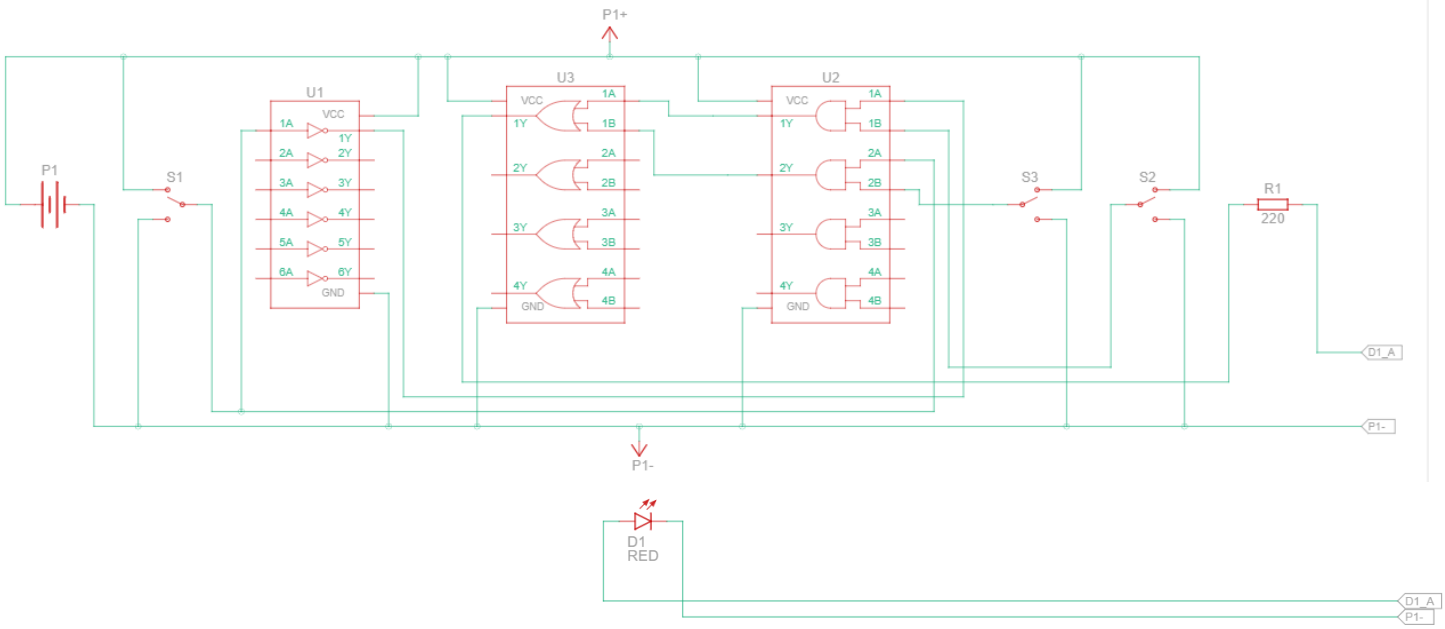
1. Aim: Design a data acquisition system using multiplexer.

2. Requirements :

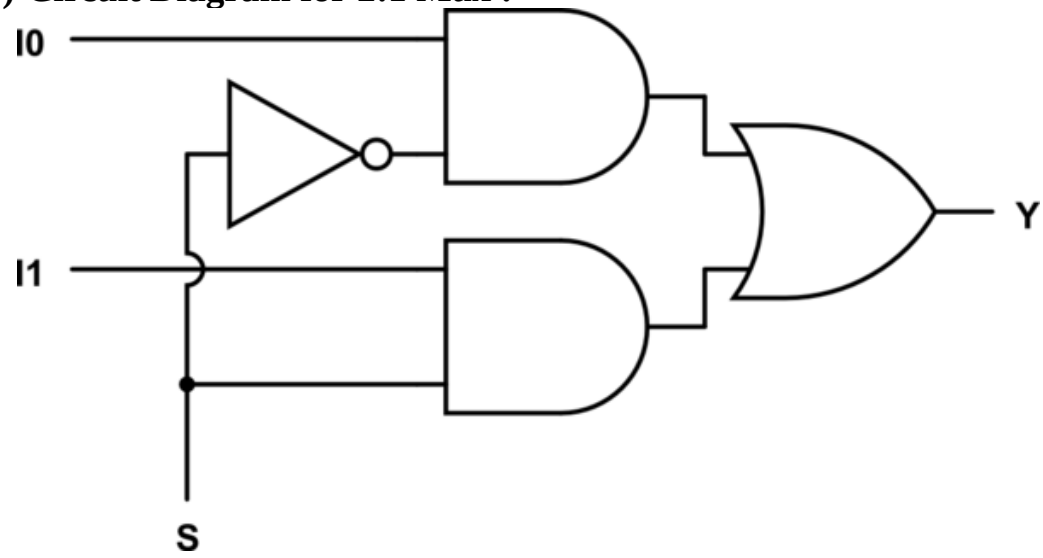
i. **Software :** TinkerCad
ii. **Hardware :** Breadboard, Connecting Wires, IC for 7404, 7408, 7432, Power Supply, Slideswitches , 220 ohm resistor, LED's.

3. Circuit Diagram:

(a) Schematic Diagram for 2:1 Mux :



(b) Circuit Diagram for 2:1 Mux :



4. Simulation Results

Multiplexer : It is a combinational circuit in which no. of input and outputs are not same. However, there is a relationship between input and output followed by:-

n : 2^n

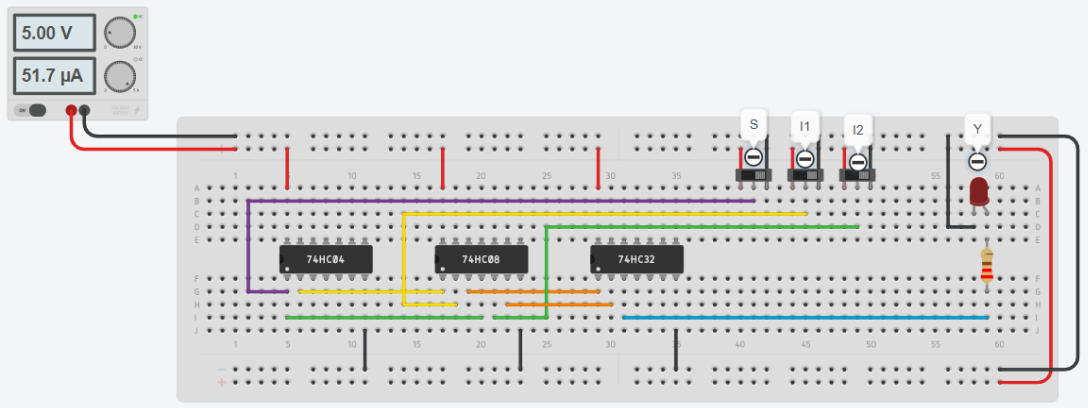
where n is the input variable.

In a Multiplexer the no. of input can be 2 and a multiple of 2 and the output will depend upon no. of select lines and input relationship.

In case of 2:1 mux, no. of input is 2 but no. of select lines is 1. The Output is also 1.

Boolean Expression : S'I1 + SI2

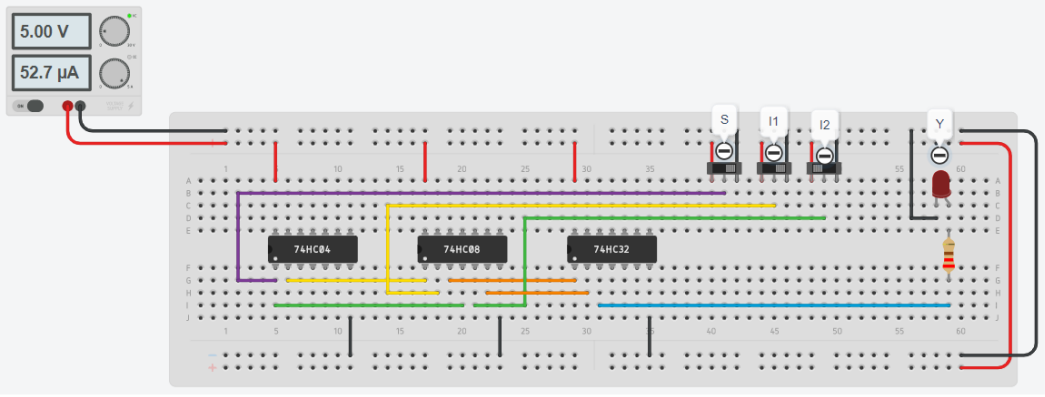
(i.) When S,I1,I2 = 0



Truth Table :-

S	I1	I2	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

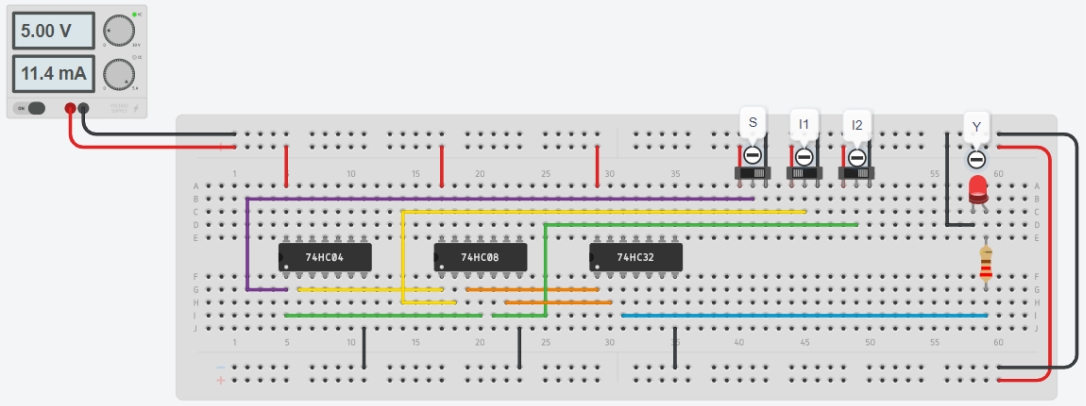
(ii.) When S,I1 = 0 & I2 = 1



Truth Table :-

S	I1	I2	Y
0	0	0	0
0	0	**1**	0
0	1	0	1
0	1	**1**	1
1	0	0	0
1	0	**1**	1
1	1	0	0
1	1	**1**	1

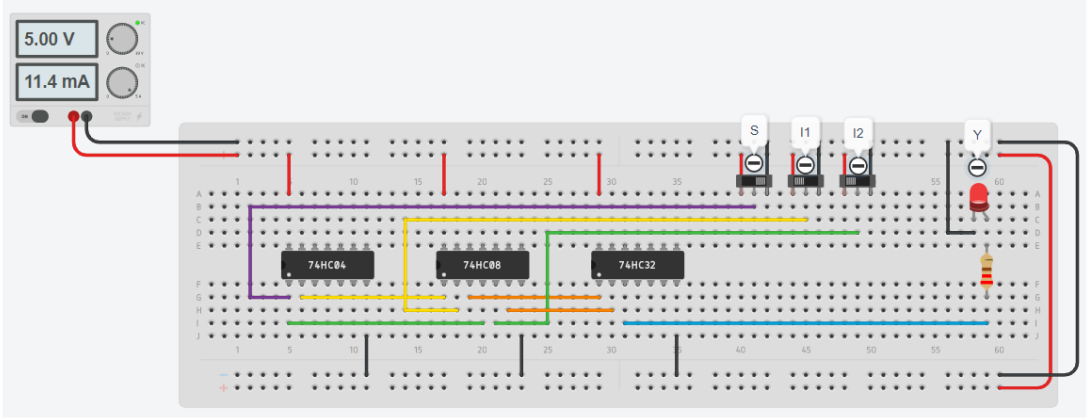
(iii.) When S,I2 = 0 & I1 = 1



Truth Table :-

S	I1	I2	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

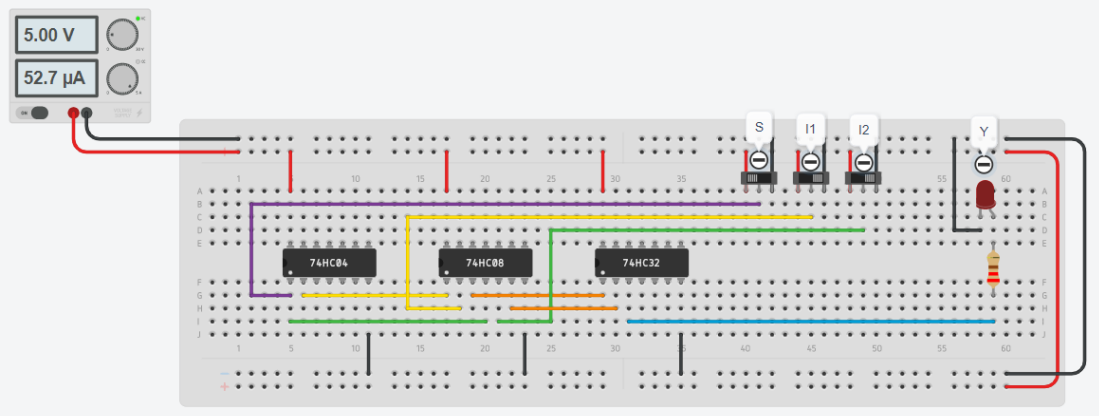
(iv.) When S = 0 & I1,I2 = 1



Truth Table :-

S	I1	I2	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

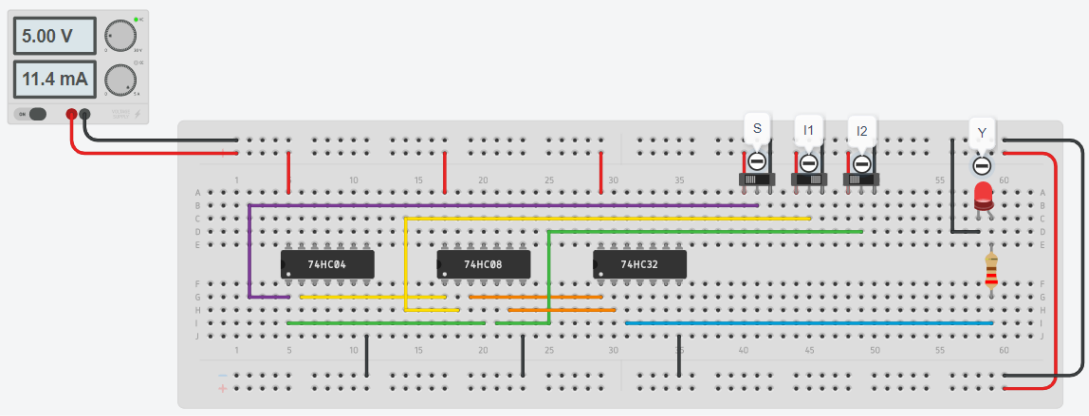
(v.) When S = 1 & I1,I2 = 0



Truth Table :-

S	I1	I2	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

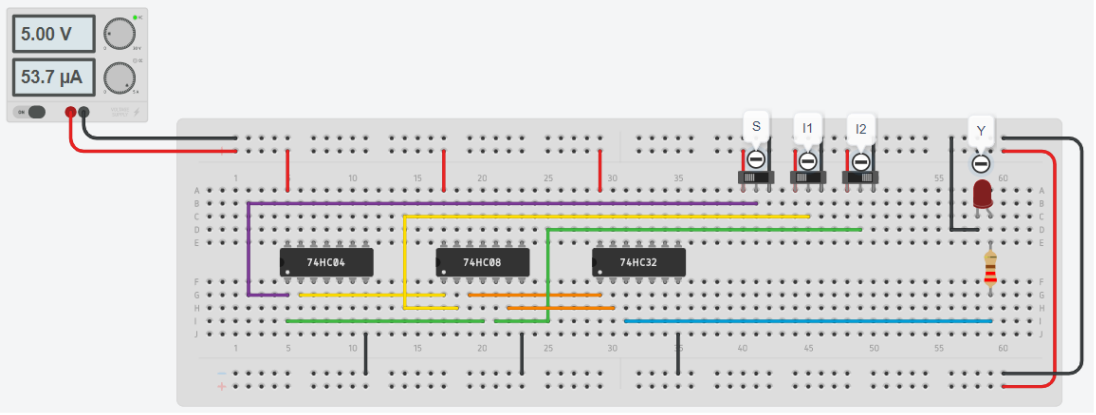
(vi.) When S,I2 = 1 & I1 = 0



Truth Table :-

S	I1	I2	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

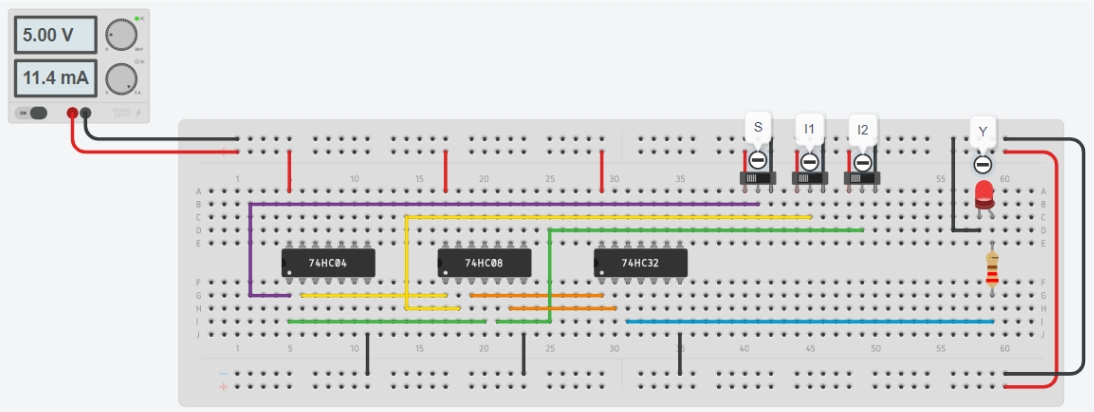
(vii.)When S,I1 = 1 & I2 = 0



Truth Table :-

S	I1	I2	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

(viii.) When S,I1,I2 = 1



Truth Table :-

S	I1	I2	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Truth Table :-

S	I1	I2	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

5. Observations : Here are some observations for a 2:1 mux:

1. **Input and output signals:** A 2:1 mux has two input signals and one output signal. The output signal is selected from one of the two input signals based on the Select Line input.
2. **Select Line:** The select line is the input line that determines which input signal is passed through to the output. The select line is a digital signal that is used to select one of several input signals and direct it to the output. The number of select lines in a mux depends on the number of input signals it can select from.
3. **Logic gates:** A 2:1 mux can be implemented using logic gates such as AND, OR, and NOT gates. The logic gates are used to switch between the two input signals based on the select line input.
4. **Applications:** 2:1 muxes are commonly used in digital systems for signal processing, data acquisition, and communications applications. They are often used in combination with other digital circuits, such as logic gates and flip-flops, to perform more complex operations.

6. Troubleshooting:

1. Messy Circuit Connection & loose connection.

2. **Incorrect gate implementation:** Another error that can occur is when the gate is not implemented correctly. For example, if you are testing an AND gate and accidentally implement an OR gate instead, you will get incorrect results. Double-check your gate implementation to make sure it matches the logic symbol for the gate you are testing.

3. **Faulty equipment:** Finally, it's possible that the error is not related to the gate or the truth table, but rather to faulty equipment. Make sure that your testing equipment is working properly and is calibrated correctly.

7. Result: We have successfully Designed a data acquisition system using multiplexer.

Learning outcomes (What I have learnt):

1. Understanding of how a mux operates to select one of two input signals based on a select line input.
2. Gaining knowledge about the design and operation of 2:1 mux.
3. Learning how to use logic gates to implement 2:1 mux.
4. Developing skills in verifying the functionality of 2:1 mux through TinkerCad.

Evaluation Grid:

Sr. No.	Parameters	Marks Obtained	Maximum Marks
1.	Worksheet completion including writing learning objectives/Outcomes.(To be submitted at the end of the day).		12
2.	Viva		8
3.	Student Engagement in Simulation/Demonstration/Performance and Controls/Pre-Lab Questions.		10
	Signature of Faculty (with Date):	Total Marks Obtained:	