# Experiment Title. 1.4

**Student Name: Chinmay Jain** **UID: 22BAI71094**
**Branch: CSE-AI/ML** **Section/Group: 109-B**
**Semester: II** **Date of Performance: Mar 11, 2023**
**Subject Name: Digital Electronics** **Subject Code: 22ECH-101**

**1. Aim:** Design a given function using K-maps and make a Gate of the Expression.

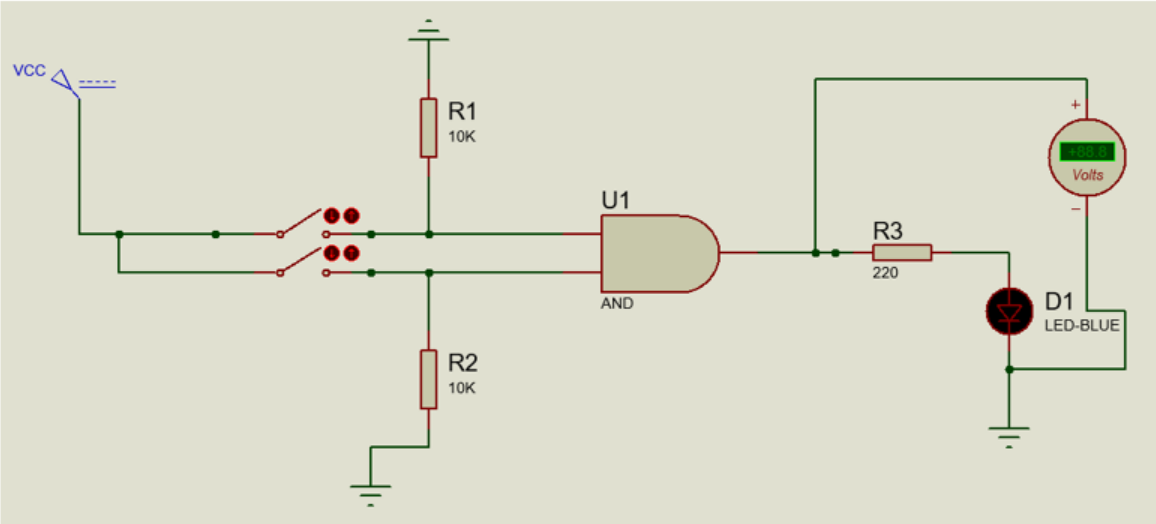
**2. Requirements :**

i. **Software :** TinkerCad
ii. **Hardware :** Breadboard, Connecting Wires, IC 7408, Power Supply, 2 Slideswitch, 220 ohm resistor.

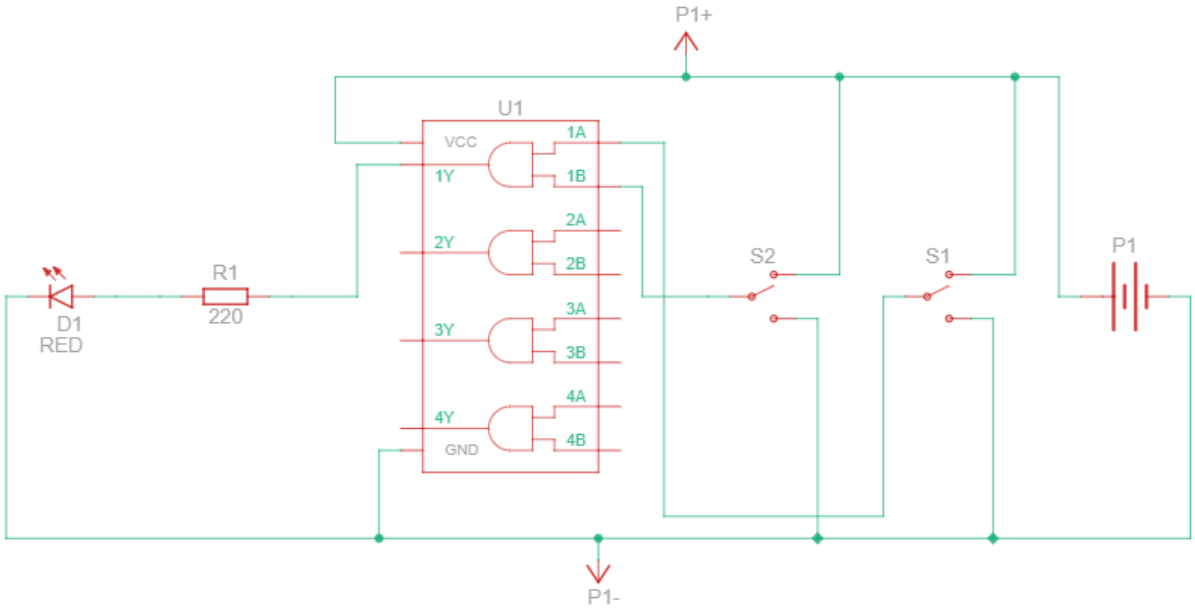
**3. Design :** Canonical Forms (Normal Forms): Any Boolean function can be written in disjunctive normal form (sum of min-terms) or conjunctive normal form (product of max-terms). A Boolean function can be represented by a Karnaugh map in which each cell corresponds to a minterm. The cells are arranged in such a way that any two immediately adjacent cells correspond to two minterms of distance 1. There is more than one way to construct a map with this property.

## 3. Circuit Diagram:

### (a) Circuit Diagram for AND Gate :

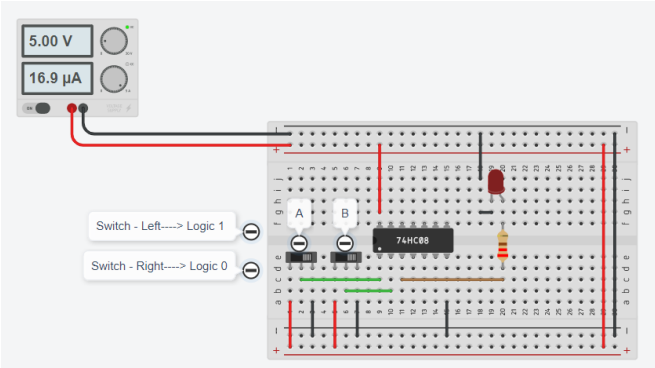


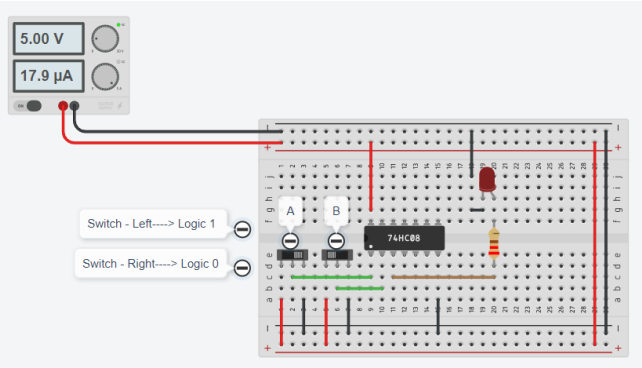

### (b) Schematic Diagram for AND Gate :

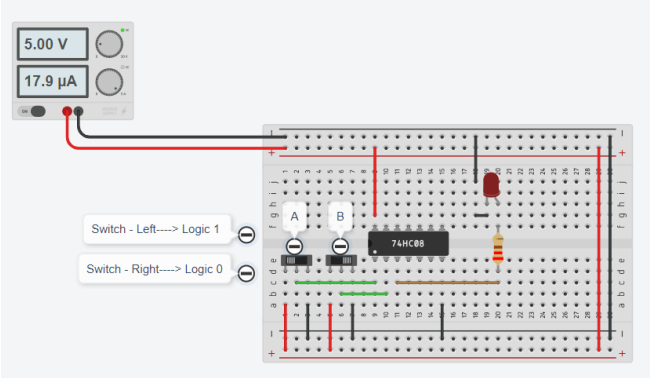


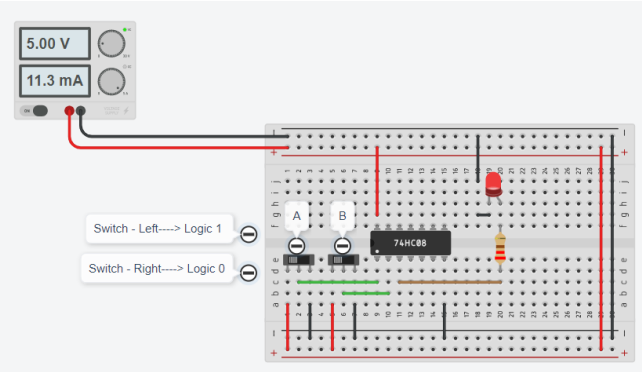
## 4. Simulation Results :

### (a) AND Gate

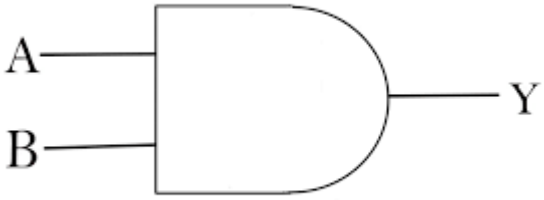



**Concept Used :** An AND gate is a fundamental logic gate in digital electronics that take in two or more binary inputs and produces a single binary output, which is high (1) only if all of the inputs are high (1).
The AND gate is represented by the symbol shown below, which has two inputs (A and B) and one output (Y).



The output of AND gate is determined by the logical operation of multiplication. If both inputs are 1, the output is 1. Otherwise, the output is 0.
The truth table for an AND gate is as follows :

**Truth Table :**

| Input | | Output |
|---|---|---|
| A | B | Y |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

For example, if input A is 1 and input B is 1, the output Y is 1. However, if either input A or input B is 0, the output Y is 0.
The AND gate is a fundamental building block of digital logic circuit and is used in many applications, such as in design of the microphones, memory units and control units.

5. **Observations :** Some observations that can be made while designing and realizing a function using K-maps include:

- The number of variables in the function determines the size of the K-map.
- The larger the group of adjacent 1s, the simpler the resulting Boolean expression will be.
- Prime implicants that are essential must be included in the final simplified expression.

**6. Troubleshooting:** When designing and realizing a given function using K-maps and verifying its performance, some common troubleshooting or errors that one might encounter include:

1. Incorrectly plotting minterms on the K-map: Make sure to correctly identify the minterms and plot them on the K-map according to their binary representation.
2. **Not grouping all adjacent 1s**: Make sure to group all adjacent 1s on the K-map to form implicants. This includes groups that wrap around the edges of the K-map.
3. **Not selecting all essential prime implicants**: Make sure to identify and select all essential prime implicants when simplifying the Boolean expression.
4. **Errors in converting the simplified Boolean expression into a circuit**: Make sure to correctly translate the simplified Boolean expression into a circuit using logic gates**.**

**7. Result:** We have successfully designed the K-map and made the desired gate.

**Learning outcomes (What I have learnt):**

**1.** Understanding the concept of K-map.

**2.** Understanding the concept of Boolean Algebra.

**3.** Developing the Logic Gates.

**4.** Verifying the correctness of a gate.

**Evaluation Grid:**

| Sr. No. | Parameters | Marks Obtained | Maximum Marks |
|---|---|---|---|
| 1. | Worksheet completion including writing learning objectives/Outcomes.(To be submitted at the end of the day). | | 12 |
| 2. | Viva | | 8 |
| 3. | Student Engagement in Simulation/Demonstration/Performance and Controls/Pre-Lab Questions. | | 10 |
| | Signature of Faculty (with Date): | Total Marks Obtained: | |