VLSI Design Flows

The Custom IC Design Flow

```
                    Conception of the idea
                              │
                              ▼
                     Definition of the Design
                              │
                              ▼
  Comparison with   →     Implementation    ←   Comparison with
  design specs                 │                 design specs
                              ▼
                         Simulation
                              │
                              ▼
                     Physical Definition
                              │
                              ▼
                     Physical Verification
                              │
                              ▼
                     Parasitic Extraction
                              │
                              ▼
                         Fabrication
                              │
                              ▼
                   Testing and Verification
                              │
                              ▼
                          Product
```

Cadence Tools

Schematic Entry → **Composer**

Simulation → **Virtuoso Analog Design Environment**

OK?
No / Yes

Layout Design → **Virtuoso**

Layout Verification → **Virtuoso LVS**

OK?
No / Yes

Post-Layout Simulation → **Virtuoso RCX + ADE**

OK?
No / Yes

Format conversion (GDSII, CIF, CALMA, etc.)