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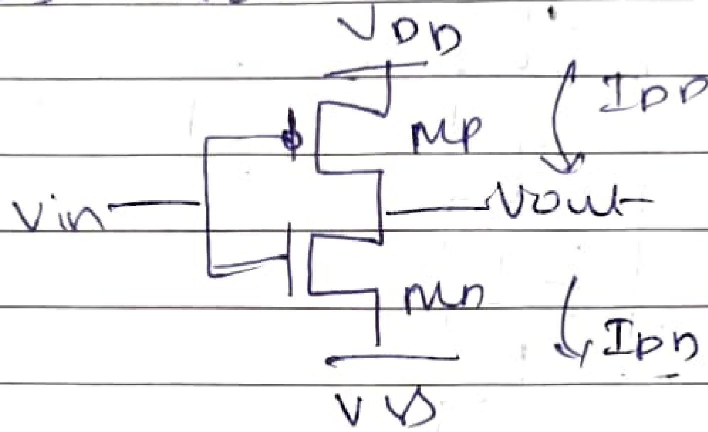
3) * Variations in switching point of a CMOS inverter with changes in β_p/β_n ratio

→ CMOS inverter



W.K.T

$$V_m = \frac{\sqrt{\frac{\beta_n}{\beta_p}}\, V_{tn} + V_{DD} - |V_{tp}|}{1 + \sqrt{\frac{\beta_n}{\beta_p}}} \longrightarrow (1)$$

here

$$\beta_n = \mu_n C_{ox} \left(\frac{W}{L}\right)_n$$

$$\beta_p = \mu_p C_{ox} \left(\frac{W}{L}\right)_p$$

So, $\frac{K_n'}{K_p'} = 2 \text{ to } 3 \longrightarrow (2)$

Let

$\frac{\mu_n}{\mu_p} = r$ (mobility ratio)

- A symmetrical inverter has V.T.C equal to i/p voltage range

$V_{in} = \frac{1}{2} V_{DD} \longrightarrow (3)$

rearranging the equation

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$$I_{dn} = I_{dp}$$

$$\frac{\beta_n}{2}\left[\frac{1}{2}V_{DD} - V_{tn}\right]^2 = \frac{\beta_p}{2}\left[V_{DD} - \frac{V_{DD}}{2} - |V_{tp}|\right)^2$$

$$\frac{\beta_n}{\beta_p} = \left(\frac{\frac{V_{DD}}{2} - |V_{tp}|}{\frac{V_{DD}}{2} - V_{tn}}\right)^2$$

$$V_{tn} = V_{tp}$$

$$\beta_n = \beta_p$$

widths of fpets changes the switching point of inverter.

4) given,

$V_{DD} = 3.3V - V_{OH}$

$V_{tn} = 0.7V$

$V_{tp} = -0.7V$

$\beta_p = \beta_n$

ideally $V_{OH} = V_{DD} = 3.3V$.

$V_{OL} = 0V$

here

$$V_{IL} = \frac{1}{8}(3V_{DD} + 2V_{tn})$$

$$= \frac{1}{8}(3 \times 3.3 + 2 \times 0.7)$$

$$= 1.4125 V$$

$$V_{IH} = \frac{1}{8}(5V_{DD} + 2V_{tp})$$

$$= \frac{1}{8}(5 \times 3.3 + 2(-0.7))$$

$$= 1.8875\text{ V}$$

So, $N_{MH} = V_{OH} - V_{IH}$

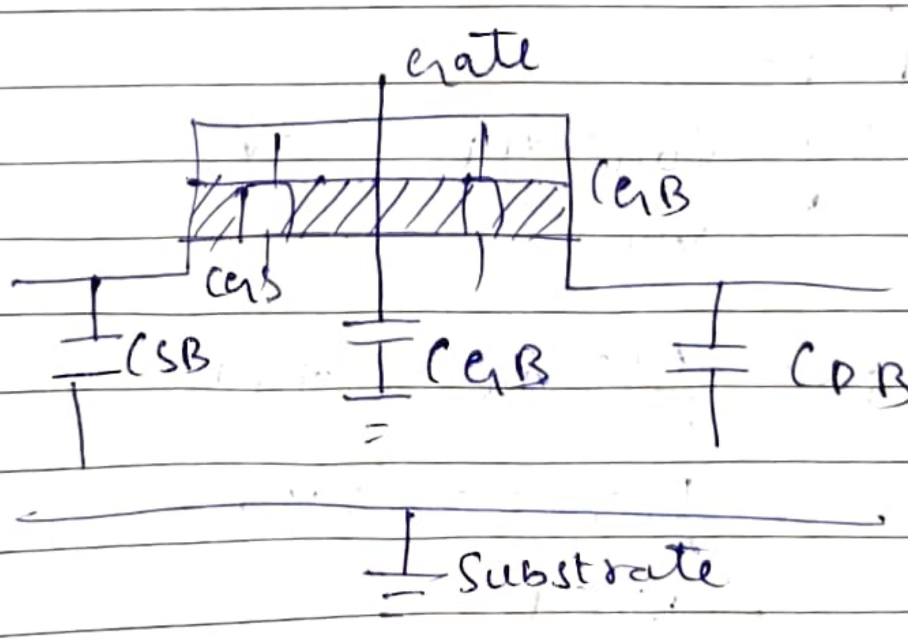
$$= 3.3 - 1.8875$$

$$= 1.4125$$

$$\boxed{NM_H = NM_L}$$

So, for any given threshold voltage V_t, the noise margin can always be increased & improved by increasing supply voltage.

5) <u>Capacitance modeling</u>



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* gate to channel capacitance
  C_{GS}, C_{GD}
* source to drain diff to Bulk
  C_{sb}, C_{dB}
* gate to Bulk
  C_{gb}

so $C_g = C_{gb} + C_{gd} + C_{gs}$

① Cutoff mode

$$C_{gb} = \frac{\varepsilon_{ox}}{t_{ox}} A$$

since no channel is formed, $C_{gs} = 0$

$C_{gd} = 0$

So. $\boxed{C_g = \frac{\varepsilon_{ox}}{t_{ox}} A} \rightarrow ①$.

② linear

$C_{gb} = 0$ (channel is formed but there is no polarity)

$C_{gs} = \frac{\varepsilon_{ox}}{2t_{ox}} A$ (2 tox caz of source & drain)

$C_{gd} = \frac{\varepsilon_{ox}}{2t_{ox}} \cdot A$

$$C_g = \frac{\varepsilon_{ox}}{t_{ox}} A \longrightarrow (2)$$

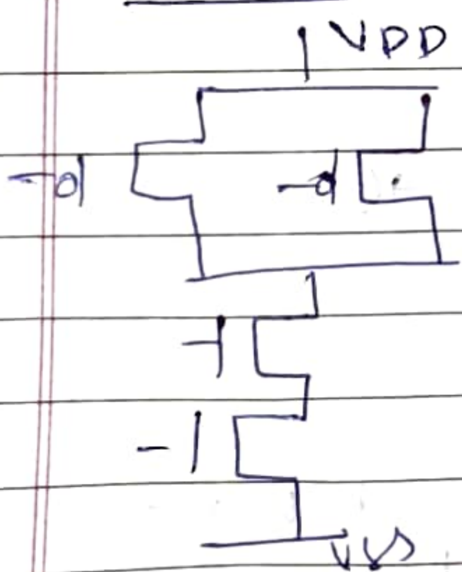
(3) Saturation region
- channel gets pinched off

$$C_{gb} = 0, \quad C_{gd} = 0$$

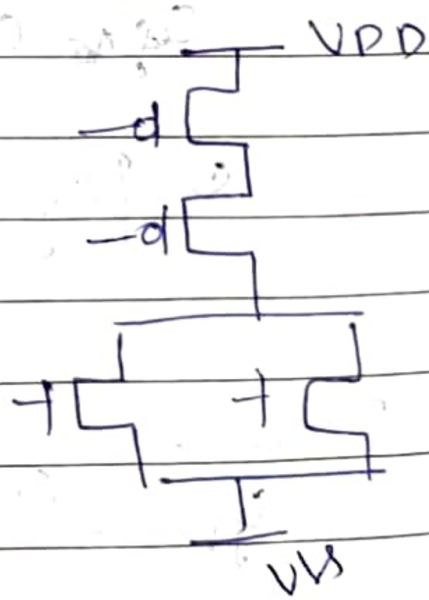
$$C_{gs} = (66\%) \left(\frac{\varepsilon_{ox}}{t_{ox}} A\right).$$

8) Nand based design is better than NOR based design

NAND



NOR



* In NAND pmos are in ||el & in NOR they are in series

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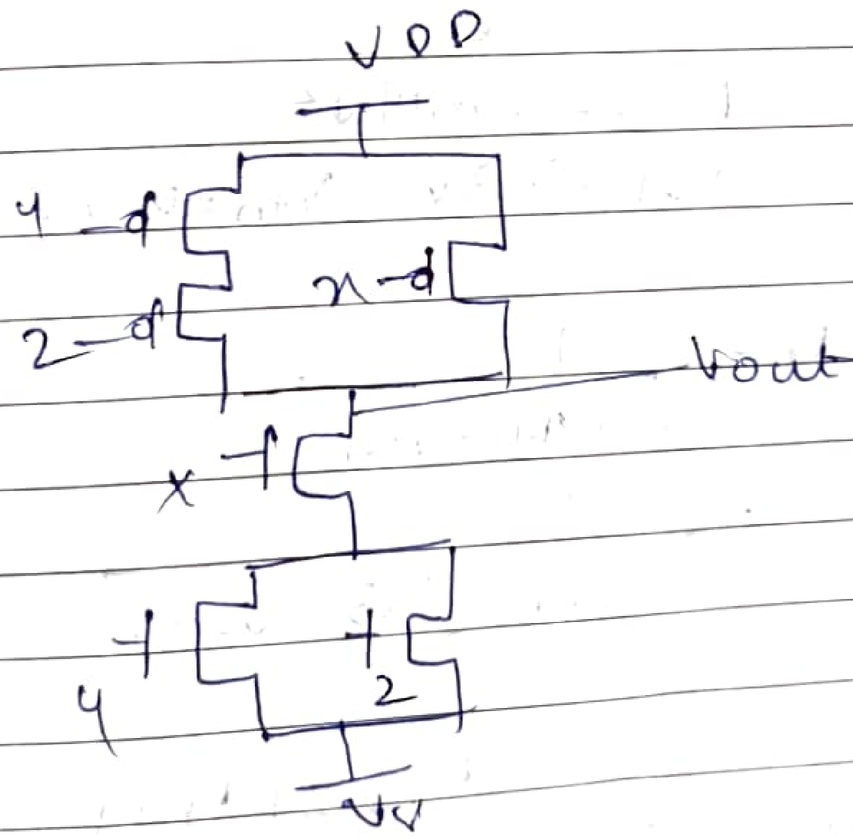
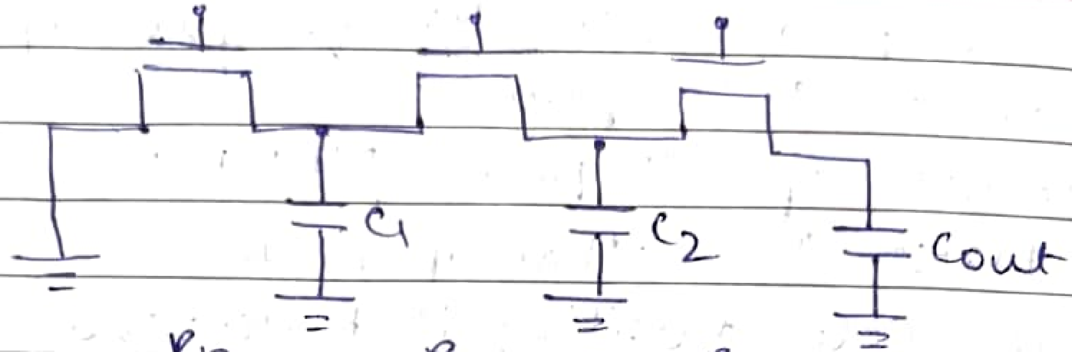
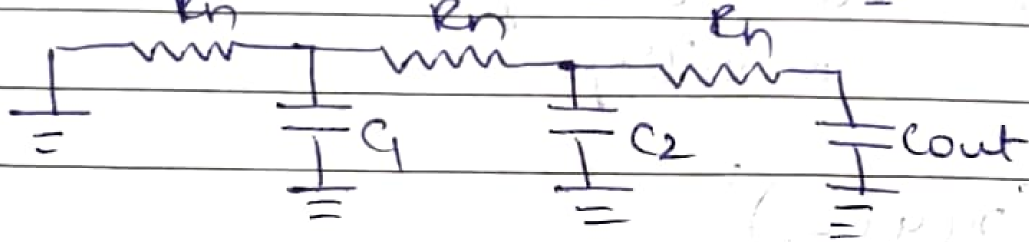
* parallel pmos makes stronger pull-up network than a series pmos
, Because of ||el pmos NAND based design is faster than that of NOR
, Since hole mobility is faster than electron mobility.

9) $(x(y+z))'$



11)





given, $C_{out} = 130fF$

$C_1 = C_2 = 36fF$

$\beta_n = 2.0 mA/V^2$

$V_{DD} = 3.3V$, $V_{tn} = 0.7V$.

here,

$$R_n = \frac{1}{\beta_n(V_{DD} - V_{tn})}$$

$$= \frac{1}{2.0\times10^{-3}(3.3 - 0.7)} = 192.30\Omega$$

$$T_n = 3R_n C_{out} + 2R_n C_2 + R_n C_1$$

$$= R_n[3C_{out} + 2C_2 + C_1]$$

$$= 192.30[3\times130 + 2\times36 + 36]\times10^{-15}$$

$$= 9.577\times10^{-11} \text{ or } 95.77 \text{ ps}$$

if we ignore C_1 & C_2

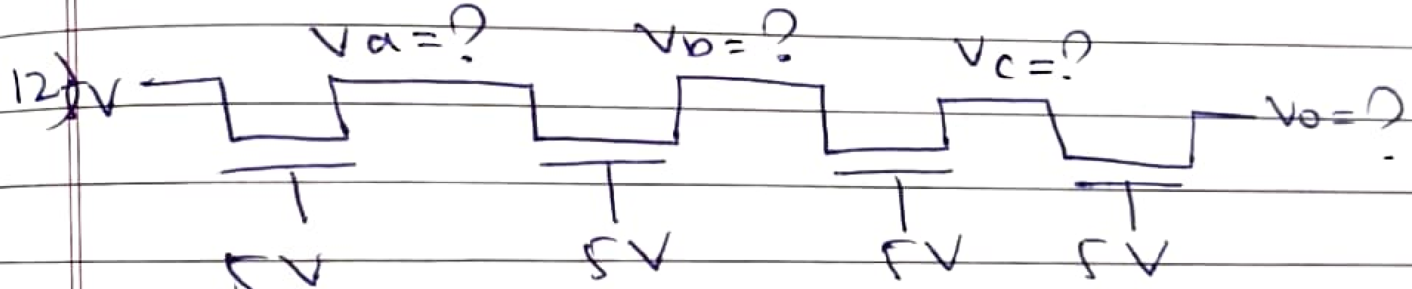
$\tau_n = 3 R_n C_{out}$

$= 3 \times 192.31 \times 130 \times 10^{-15}$

$= 75$ ps

$\%\ error = \frac{95.77 - 75}{95.77} \times 100$

$= 21.6\%$



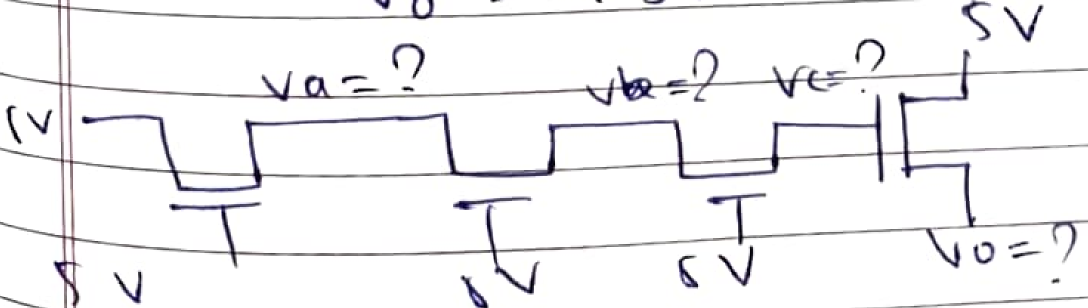
here $V_a = 5 - 0.7$

$= 4.3V$

$V_b = 5 - 0.7 = 4.3V$

$V_c = 4.3V$

$V_o = 4.3V$



$V_a = 5 - 0.7 = 4.3V$

$V_b = 4.3V$

$V_c = 5 - 0.7 = 4.3$

$V_o = 4.3 - 0.7$

$= \cancel{0.}\ 3.6V$