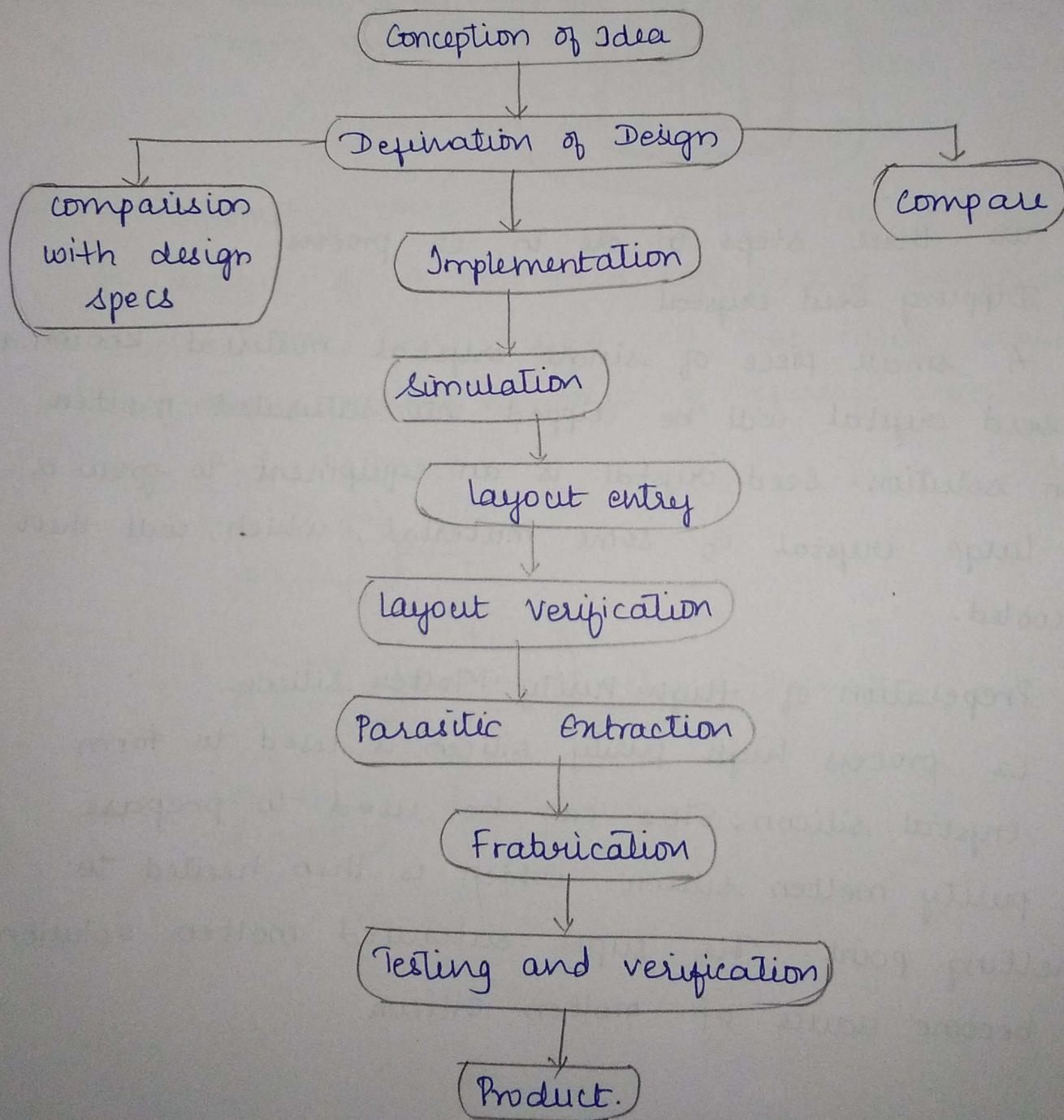


Q.No.	Questions	Marks	CO	BL	PO	PI Code	Gate QP
1a	Illustrate the full custom design flow in VLSI.	6	CO1	L2	1	1.4.2	
1b	Explain Czochralski method of growing silicon ingots with a neat figure.	6	CO1	L2	1	1.2.1	
1c	A symmetric CMOS inverter is used as a reference in design of a standard cell library. Design a complex CMOS logic AOI23 cell that meets same performance criteria as that of reference inverter.	8	CO2	L3	2	2.1.2	
2a	Estimate the charging and discharging time constants for the OAI321 gate implemented using fully CMOS logic. Also annotate the diffusion capacitances at all the nodes for the same.	6	CO2	L3	14	14.2.2	Gate
2b	Solve the node voltages in the arrangements given below if $V_m = 0.7V$. (Ignore the back-gate effect)	6	CO2	L3	1	1.4.2	Gate
2c	Explain the different process steps involved in fabrication of CMOS inverter in Pwell process, with neat diagrams.	8	CO1	L2	1	1.2.1	
3a	Calculate the diffusion parasitic C_{db} of the drain of a unit-sized contacted nMOS transistor in a 90 nm process when the drain is at 0 and at $V_{DD} = 1.8$ V. Assume the substrate is grounded. The transistor characteristics are $C_J = 0.98 \text{ fF}/\mu\text{m}^2$, $M_J = 0.36$, $C_{JSW} = 0.22 \text{ fF}/\mu\text{m}$, $C_{JSWG} = 0.33 \text{ fF}/\mu\text{m}$, $M_{JSW} = M_{JSWG} = 0.10$, and $\Psi_0 = 0.75$ V at room temperature. Area ($5\lambda \times 4\lambda$)	10	CO2	L3	1	1.2.1	
3b	<p>An inverter uses FETs with $\beta_n=2.1 \text{ mA/V}^2$ and $\beta_p=1.8 \text{ mA/V}^2$. The threshold voltages are given as $V_{Th}=0.6V$ & $V_{Tp}=-0.7V$ & the power supply has a value of $V_{DD}=5V$. The parasitic FET Capacitance at the output node is estimated to be $C_{FET} = 74 \text{ fF}$.</p> <ul style="list-style-type: none"> (a) Find the mid-point voltage V_M. (b) Find the values of R_n & R_p. (c) Calculate the rise & fall times at the output when $C_L=0$, and when $C_L=115 \text{ fF}$. (d) Plot t_r & t_f as a function of C_L. 	10	CO2	L3	1	1.4.2	

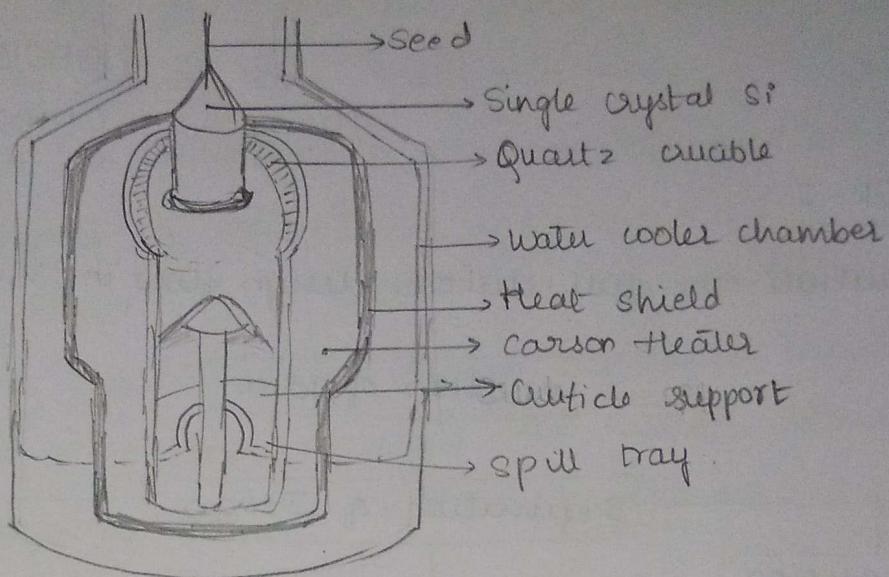
Sunidhi.V. Devadiga
237 'D'
DIFE16BEC434
CMOS

MINDR - I

1a. Illustrate the full custom design flow in VLSI



1b. Explain Czochralski method of growing silicon ingots with a neat figure.



There are three steps in one in Cz process

Step 2 Dipping Seed crystal

A small piece of single crystal material known as dip seed crystal will be dipped into saturated molten silicon solution. Seed crystal is an equipment to grow a large crystal of some material which will then be cooled.

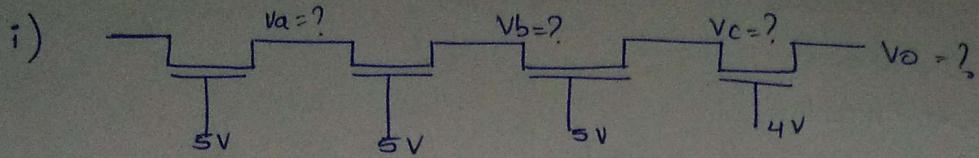
Step 1: Preparation of High Purity Molten Silicon.

In Cz process high purity silicon is used to form single crystal silicon. SiO_2 can be used to prepare high purity molten silicon which is then heated to its melting point. The super saturated molten solution will become source of molten silicon.

Step 3: Pulling the seed upward.

The seed crystal will be created from the molten silicon pool and the rod will be pulled upward and is rotated at the same time but this time rod and the crystal will be rotated in the opposite direction to minimize the effects of convection interrupts. In manufacturing single grade silicon the temperature gradient decides the simple crystal as seed crystal. As the seed is pulled upward the molten silicon helps in solidifying and so is called growing.

2b. Solve the node voltages in the arrangement given below if $V_{in} = 0.7V$ (Ignore the back gate effect)

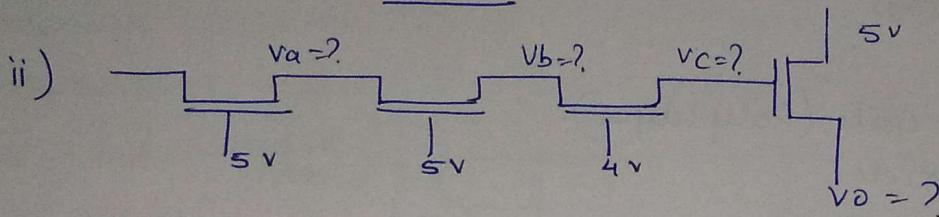


$$V_a = 5 - 0.7 = 4.3V$$

$$V_b = 5 - 0.7 = 4.3V$$

$$V_c = 5 - 0.7 = 4.3V$$

$$V_o = 4 - 0.7 = \underline{3.3V}$$



$$V_a = 5 - 0.7 = 4.3V$$

$$V_b = 5 - 0.7 = 4.3V$$

$$V_c = 4 - 0.7 = 3.3V$$

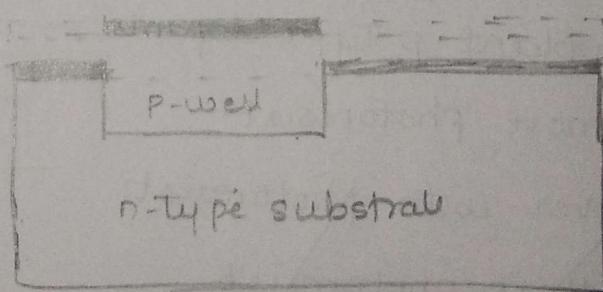
$$V_o = 3.3 - 0.7 = \underline{2.6V}$$

2c. Explain the different process steps involved in fabrication of CMOS inverter in PWEELL process with neat diagram

→ Step 1:

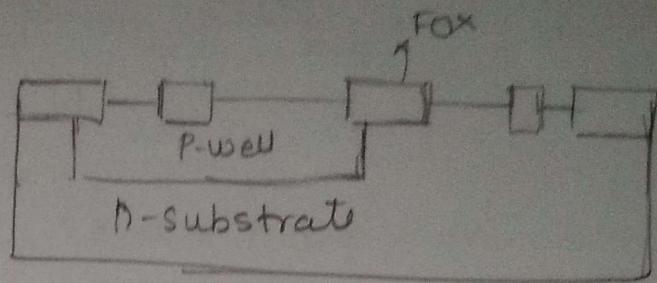
Form P-well regions

- grow oxide
- deposit photoresist
- pattern photoresist
 - N WELL mask
 - expose only n-well areas
- etch oxide
- remove photoresist
- diffuse n-type dopants through oxide mask layer



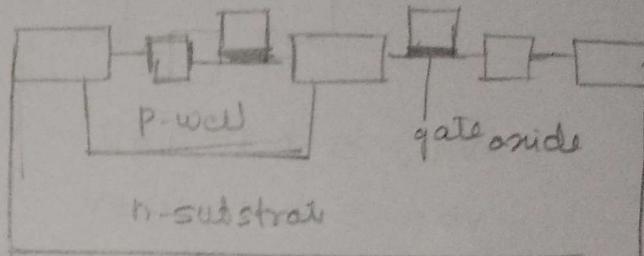
Step 2 : Form Active Regions

- Deposit SiN over wafer
- Deposit photoresist over SiN layer
- Pattern photoresist
 - Active mask
- Etch SiN in exposed areas
 - leaves SiN mask which blocks oxide growth
- Remove photoresist
- Grow Field oxide (FOX)
- Remove SiN



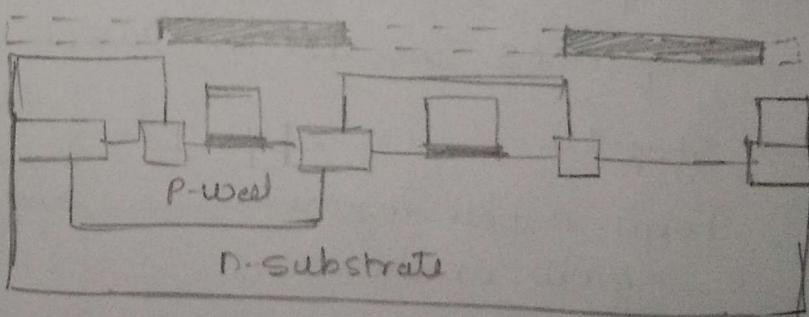
Step 3: Form Gate (Poly Layer)

- Grow Gate Oxide.
- Deposit polysilicon
- Deposit photoresist
- pattern photoresist
- Etch poly in exposed areas
- Etch/ remove oxide



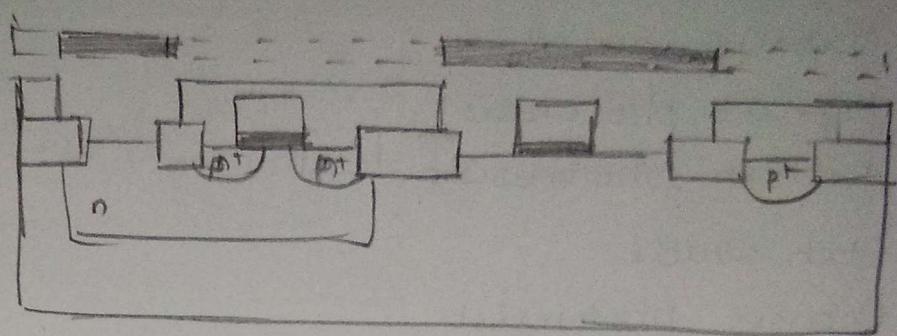
Step 4: Form PMOS S/D

- Cover with photoresist
- Pattern photoresist
- Implant p type dopants
- Remove photoresist
- Cover with photoresist
- Pattern photoresist
- Implant p-type dopants
- Remove photoresist.



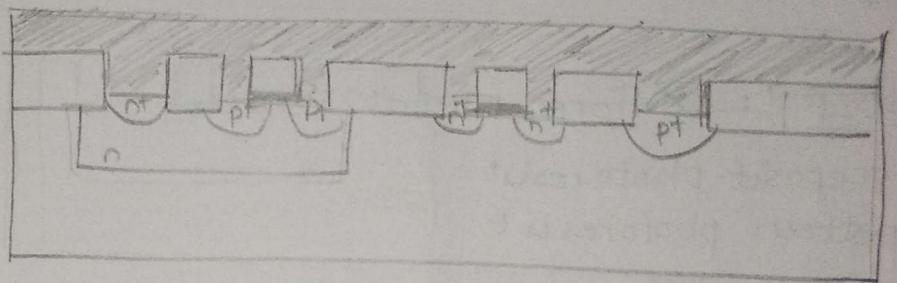
Step 5: Form nmos S/D

- Cover with photo resist
- Pattern photo resist
- Implant n-type dopants
- Remove photo resist
-



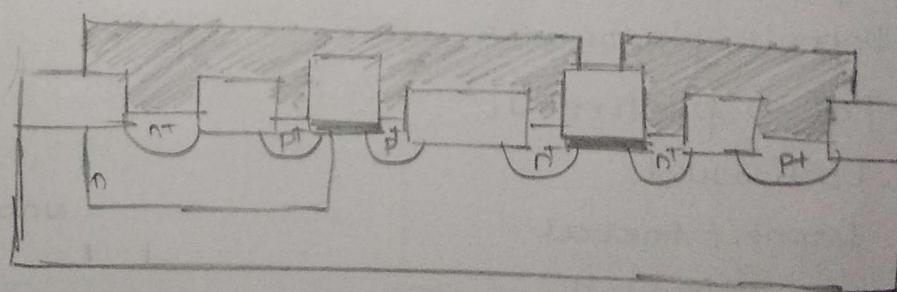
Step 6: Form Contacts

- Deposit oxide
- Deposit photo resist
- Pattern photo resist
- Contact mask
- Etch oxide
- Remove photo resist
- Deposit Metal 1
- Planarize.



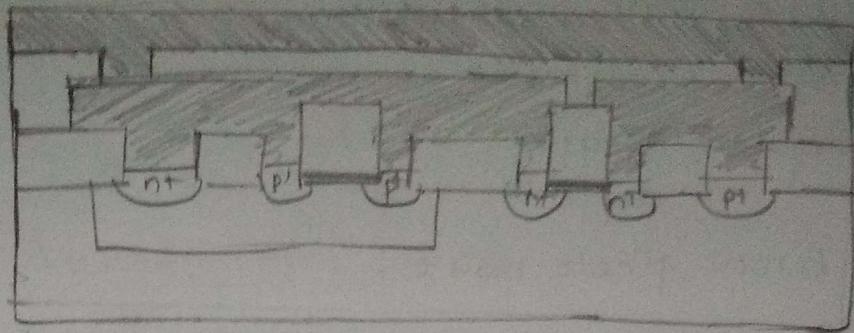
Step 7 - Form Metal1 traces.

- Deposit photoresist
- Pattern photoresist
- Metal1 Mask
- Etch Metal
- Remove photoresist



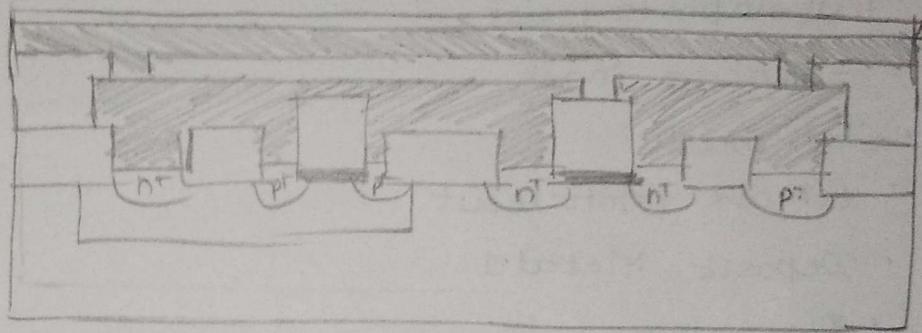
Step 8 : Form Vias to Metal1

- Deposit oxide
 - Planarize oxide
 - Deposit photoresist
 - Pattern photoresist
 - Etch oxide
 - Remove photoresist
 - Deposit Metal2
-



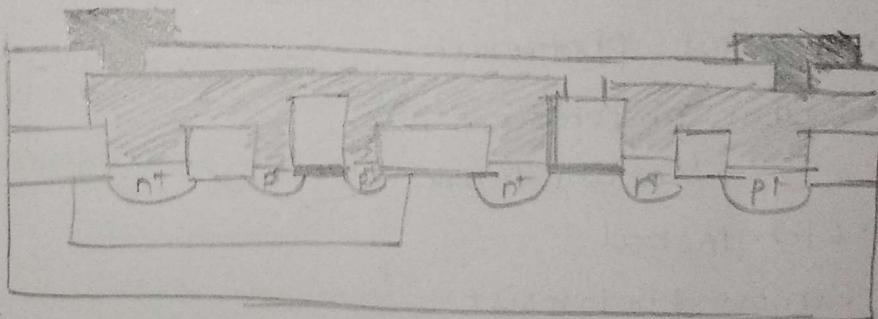
Step 9: Form Metal2 traces

- Deposit photoresist
- pattern photoresist
- etch metal
- remove photoresist



Step 10: Form Additional traces

- Deposit oxide
- Deposit photoresist
- Pattern photoresist
- Etch oxide
- Deposit metal
- Deposit photoresist
- Pattern photoresist
- Etch metal
- Repeat for each additional Metal.



3a. Calculate the diffusion parasitic Cdb of the drain of a unit sized contracted NMOS transistor in a 90nm process when the drain is at 0 and at VDD=1.8V. Assume the substrate is grounded the transistor characteristic. $C_J = 0.98 fF/\mu m^2$, $M_J = 0.36$, $C_{JSW} = 0.22 fF/\mu m$, $C_{JSWg} = 0.33 fF/\mu m$, $M_{JSW} = M_{JSWg} = 0.10$, $\psi = 0.75V$ at room temperature Area ($5\lambda \times 4\lambda$)

$$\rightarrow C_{db} = A_s + C_{jbd} + (L + 2w) (C_{jdssw} + L C_{jdsswg})$$

$$C_{jbd} = C_J \left(1 + \frac{V_{sb}}{\psi_0} \right)^{M_J}$$

$$C_{jdssw} = C_{JSW} \left(1 + \frac{V_{sb}}{\psi_0} \right)^{-M_{JSW}}$$

$$C_{jdsswg} = C_{JSWg} \left(1 + \frac{V_{sb}}{\psi_0} \right)^{-M_{JSWg}}$$

$$C_{jbd} = 0.98 f \left(1 + \frac{0}{0.75} \right)^{-0.36}$$

$$C_{jbd} = 0.98 f \left(1 + \frac{1.8}{0.75} \right)^{-0.36}$$

$$\underline{C_{jbd} = 0.98 f}$$

$$\underline{C_{jbd} = 0.63 f}$$

$$C_{jdssw} = 0.22 f \left(1 + \frac{0}{0.75} \right)^{-0.10}$$

$$C_{jdssw} = 0.22 f \left(1 + \frac{1.8}{0.75} \right)^{-0.10}$$

$$\underline{C_{jdssw} = 0.22 f}$$

$$\underline{C_{jdssw} = 0.194 f}$$

$$C_{jdsswg} = 0.33 f \left(1 + \frac{0}{0.75} \right)^{-0.10}$$

$$= \underline{0.33 f}$$

$$C_{jdsswg} = 0.33 f \left(1 + \frac{1.8}{0.75} \right)^{-0.10}$$

$$= \underline{0.29 f}$$

$$C_{db} = A_s C_j$$

$$\begin{aligned} C_{db} &= A_s C_{jbd} + (L+2w) C_{jdssw} + L C_{jdsswg} \\ @0 &= 0.55 \text{ fF} \end{aligned}$$

$$C_{db} @1.8 = 0.451 \text{ fF},$$

- 3b. An inverter uses FETs with $\beta_n = 2.1 \text{ mA/V}^2$ and $\beta_p = 1.8 \text{ mA/V}^2$. The threshold voltage are given as $V_{Tn} = 0.6 \text{ V}$ and $V_{Tp} = -0.7 \text{ V}$ and $V_{DD} = 5 \text{ V}$. The parasitic FET Capacitance at the output node is estimated to be $C_{FET} = 74 \text{ fF}$.
- find V_m
 - find R_n and R_p
 - Find t_r and t_f when $C_L = 0$ and $C_L = 115 \text{ fF}$
 - Plot t_r and t_f as function of C_L

$$\rightarrow R_p = \frac{1}{\beta_p (V_{DD} - V_{Tp})}$$

$$= \frac{1}{1.8 \text{ m} (5 - 0.7)}$$

$$= 129.19 \Omega$$

$$R_n = \frac{1}{\beta_n (V_{DD} - |V_{Tr}|)}$$

$$= \frac{1}{2.1 \text{ m} (5 - 0.6)}$$

$$= 108.225 \Omega$$

$$V_m = \frac{V_{DD} + \sqrt{\frac{\beta_n}{\beta_p}} V_{th} - (V_{LP})}{1 + \sqrt{\frac{\beta_n}{\beta_p}}} \\ = 5 + \frac{\sqrt{\frac{2.1m}{1.8m}} 0.6 - 0.7}{1 + \sqrt{\frac{2.1m}{1.8m}}}$$

$$V_m = 2.37V$$

t_r and t_f @ $CL = 0$

$$t_r = 2.2 R_p C_{FET} \\ = 2.2 (129.19) (74f) \\ = 0.021n$$

$$t_f = 2.2 R_n C_{FET} \\ = 2.2 (108.225) (74f) \\ = 0.0176n$$

t_r and t_f @ $CL = 150fF$

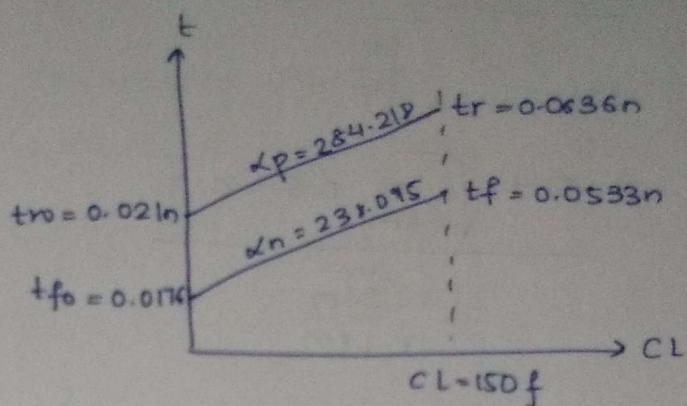
$$t_r = 2.2 R_p (C_{FET} + CL) \\ = 2.2 (129.19) (74f + 150f) \\ = 0.0636n$$

$$t_f = 2.2 R_n (C_{FET} + CL) \\ = 2.2 (108.225) (74f + 150f) \\ = 0.0533n$$

$$\alpha_p = 2.2 R_p$$
$$= 2.2 (129.19)$$
$$= 284.218$$

$$\alpha_n = 2.2 R_n$$
$$= 238.095$$

$$\alpha_{n0} = 10.0246$$



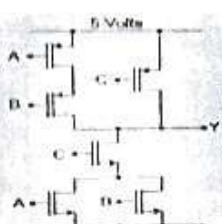
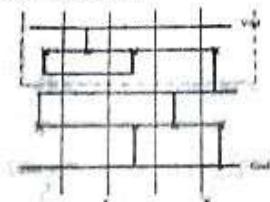
Minor Exam II, Nov 2017

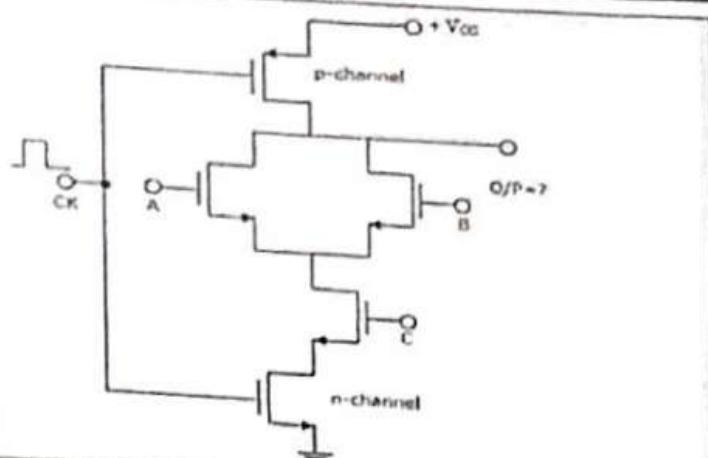
Total Duration (H:M):1:15

Course :CMOS VLSI Circuits
(15EECC301)

Maximum

Note :Answer any two full questions

Q.No.	Questions	Marks	CO	BL	PO
1a	For the circuit shown below, evaluate the output expression Y , and implement its CVSL equivalent. 	6	CO4	L3	1
1b	Examine the stick diagram shown below. Is this a functional logic gate? If so, determine the logic function it provides 	6	CO3	L3	1
1c	Ordering the poly gates of a CMOS gate expressed by AOI-23 using suitable optimizing technique and represent its equivalent stick diagram	8	CO3	L3	1
2a	Discuss the phenomenon of latch-up? Explain ways of dealing with latch-up in CMOS VLSI design	6	CO3	L2	1
2b	In the figure, the Boolean expression for the output in terms of inputs A, B and C when the clock CK is high, is given by _____. Also implement the clocked CMOS equivalent of the same	6	CO4	L3	1

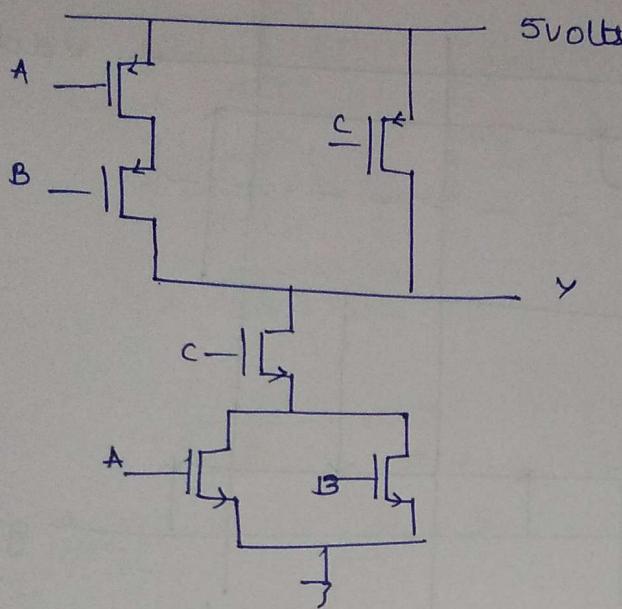


2c	<p>Consider the logic chain of a co-processor shown below. The input at A is switched from a 0 to 1. Estimate time taken for the given input to propagate through the chain using an appropriate procedure. Also choose appropriate inputs at other gates to ensure switching across the entire chain.</p>	8	CO4	L3	1	2.1.2
3a	<p>Consider the logic cascade shown in figure below. Use logical effort to find the relative size of each stage needed to minimize delay through the chain. Assume symmetric gates with $r = 2.5$.</p>	10	CO3	L3	1	1.4.2
3b	<p>Discuss the issues with Dynamic CMOS logic, and analyze how Domino logic can overcome these issues with an example.</p>	10	CO4	L3	3	14.2.2

MINOR - 2

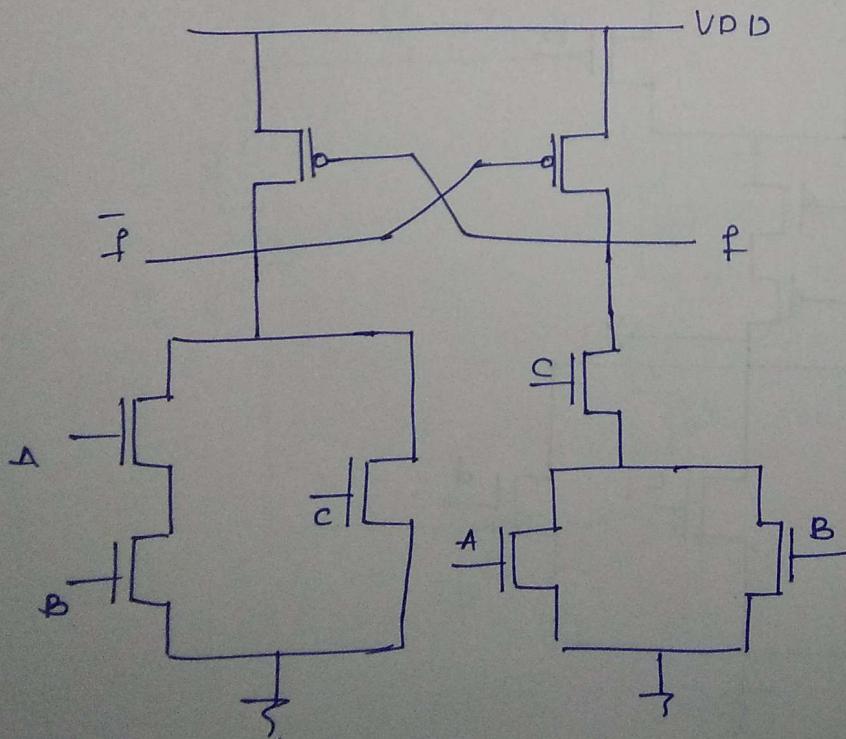
1a.

For the circuit shown below evaluate the output expression Y and implement its CVSL equivalent



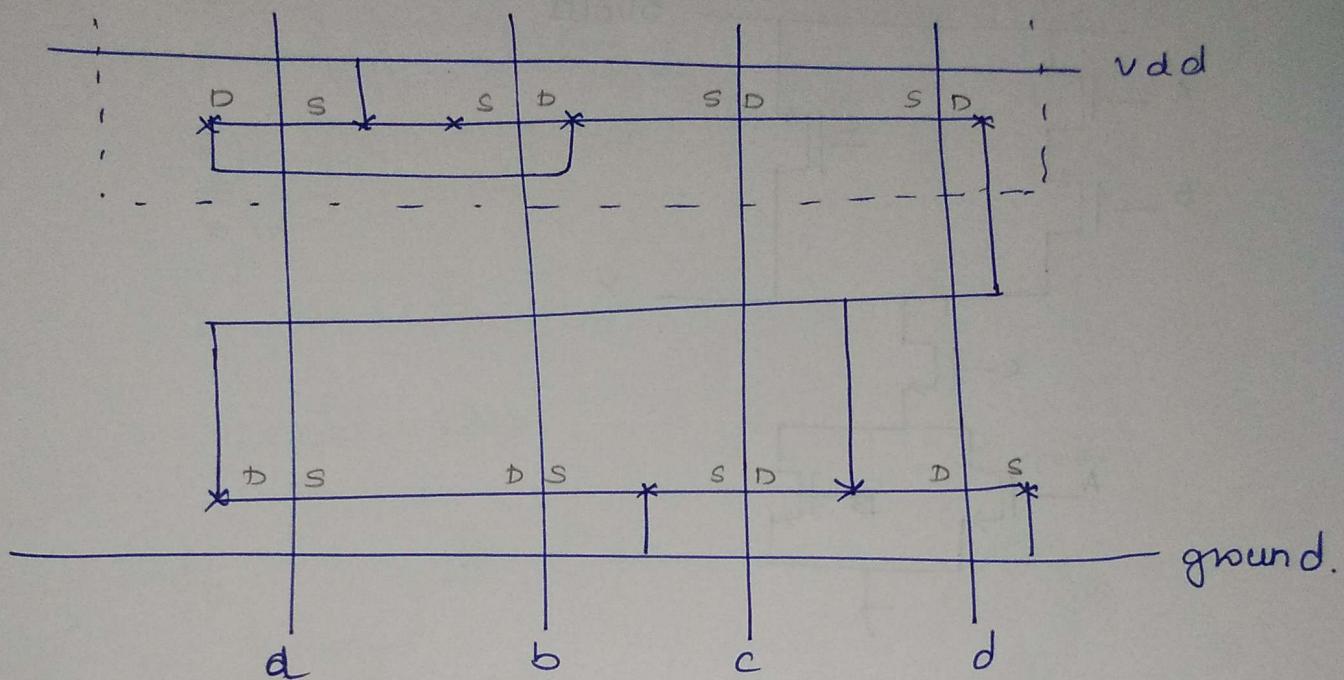
$$Y = (A + B) C$$

CVSL equivalent.

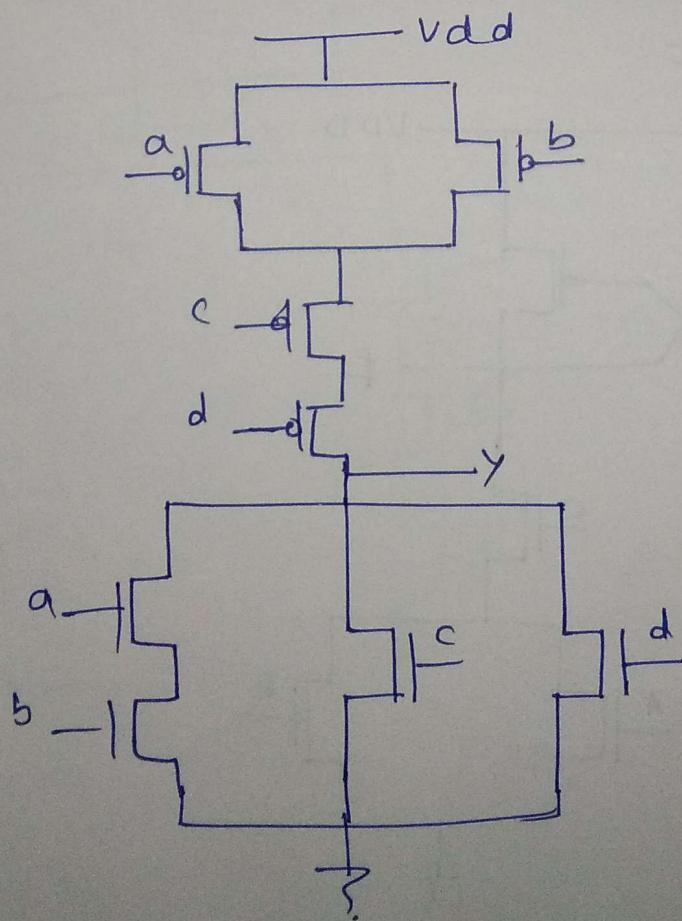


1 lb

Examine the stick diagram shown below. Is this a functional logic gate? If so determine the logic function it provides.



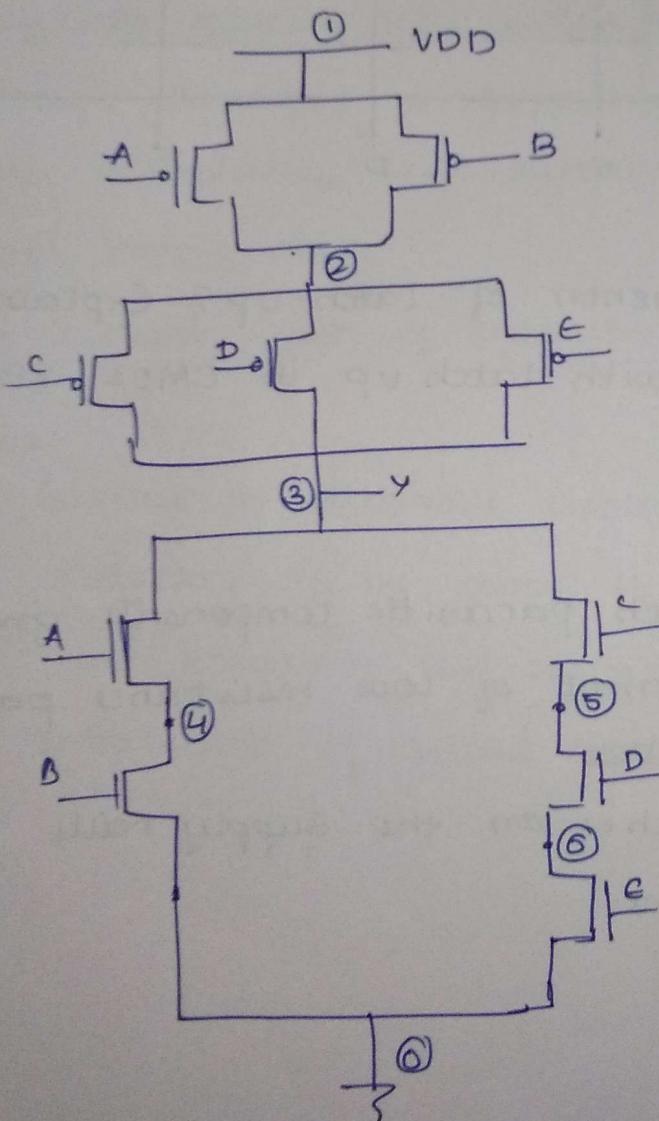
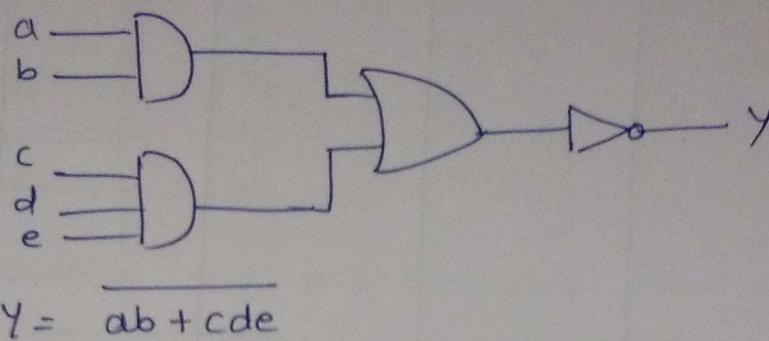
$$Y = \overline{ab + c + d}$$



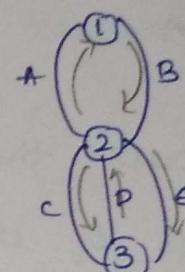
1c.

Ordering the poly gates of a CMOS gate expressed by AOI - 23 using suitable optimizing technique and represent its equivalent stick diagram

→

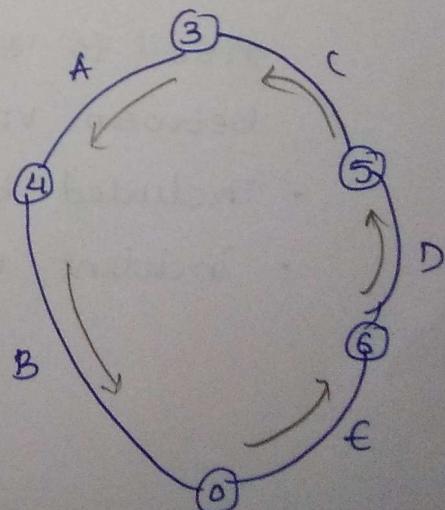


P-tree



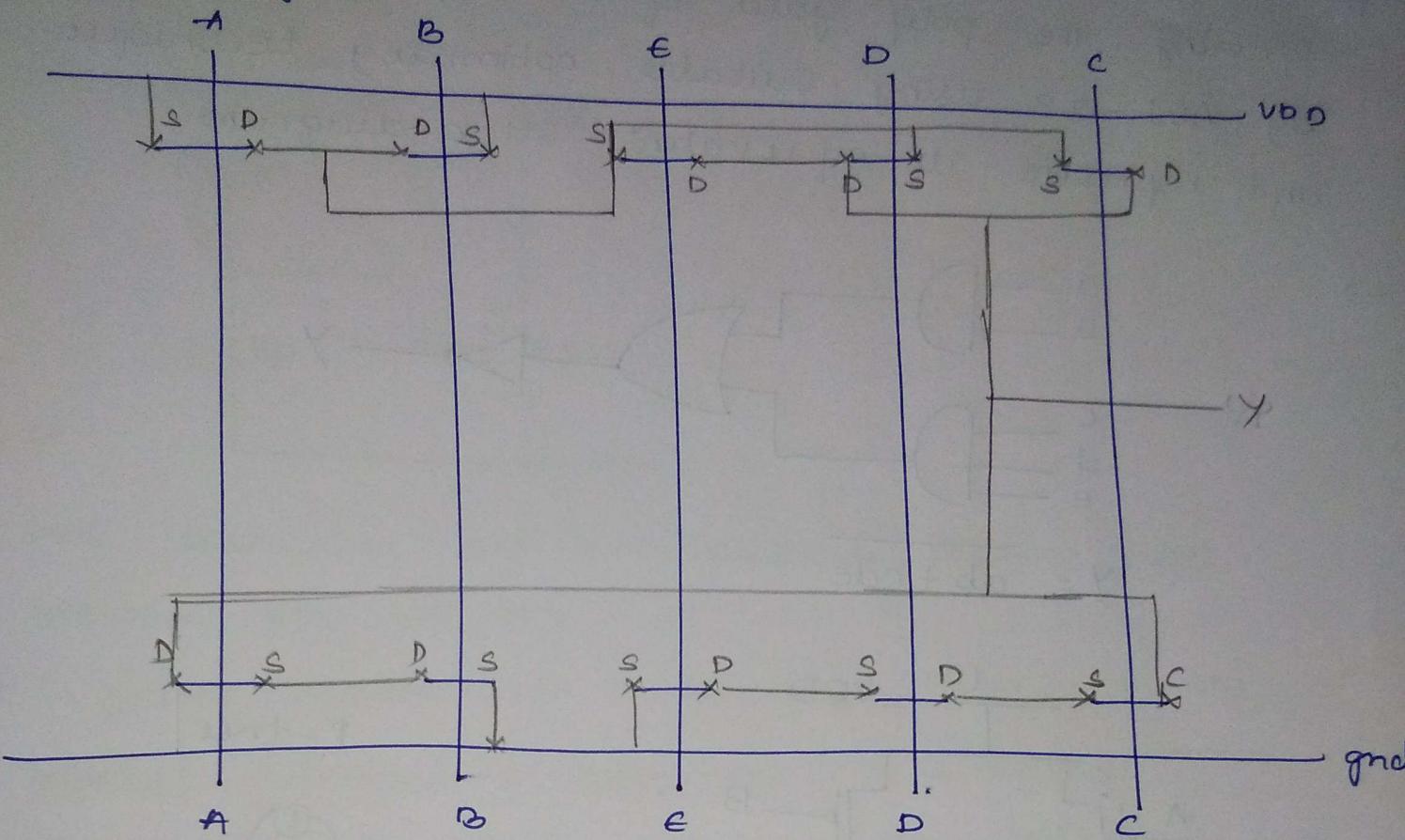
A - B - E - D - C

N-tree



A - B - E - D - C

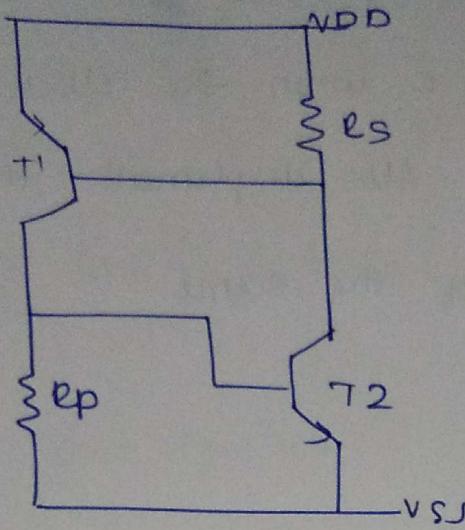
stick diagram



2a. Discuss the phenomenon of latch-up? Explain ways of dealing with latch up in CMOS VLSI design

→ causes of latch-up

- Condition in which parasitic components give rise to establishment of low resistance path between VDD and VSS
- induced by glitches on the supply rails
- incident radiations



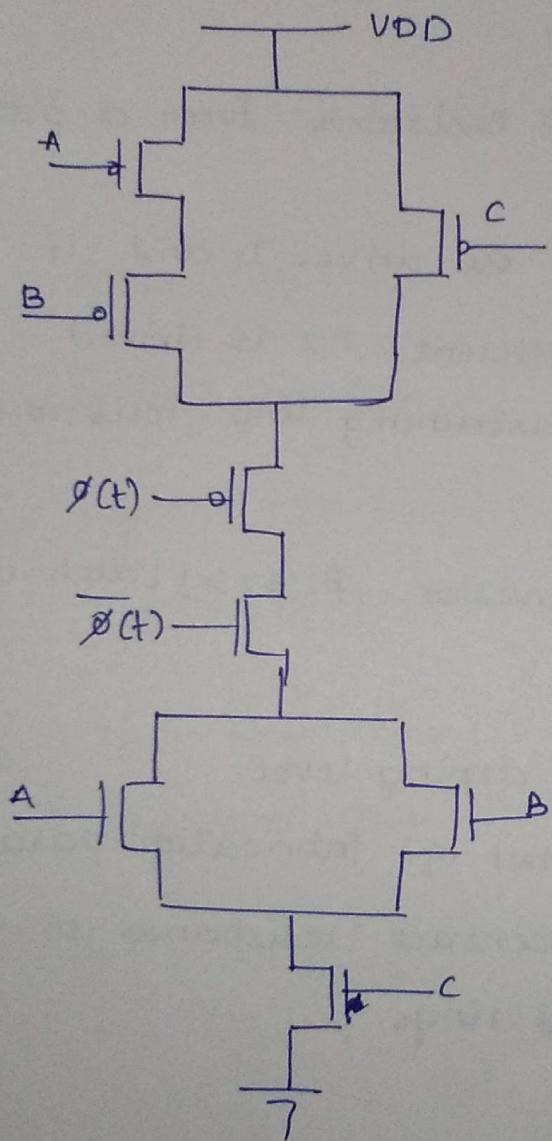
- two transistors and two resistors form a path between VDD and VSS
- sufficient current flow in r_S drives T_1 and if the voltage developed is sufficient T_2 is driven
- This establishes self-sustaining low resistance path bet' supply rails
- if current gain of transistor $\beta_1 \beta_2 > 1$ Latch up occurs

Remedies:

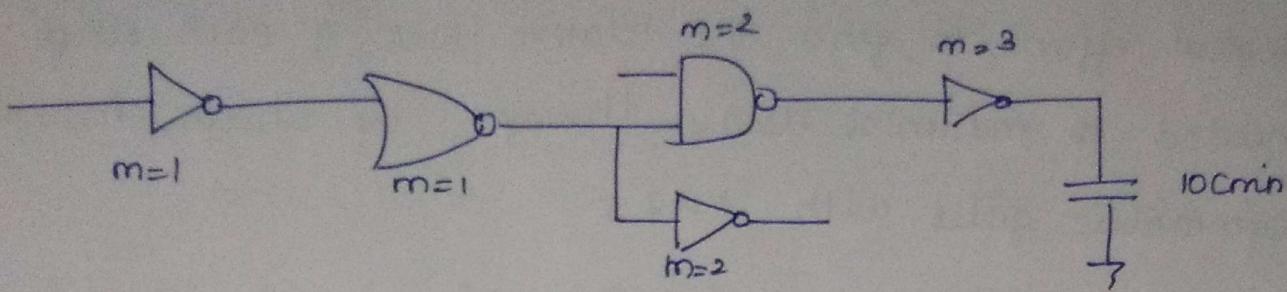
- Increase in substrate doping level
- Reducing r_P by control of fabrication parameter and ensuring low contact resistance to VSS
- Introduction of guard rings.

2 2b. In the figure the boolean expression for the op is terms of input A, B and C when the clock ck is high is given by _____. Also implement the clocked CMOS equivalent of the same.

$$\rightarrow Y = \overline{(a+b)} \cdot c$$



2c



$$\text{total delay} = t_{\text{inv}} \Big|_{m=1} + t_{\text{fnor2}} \Big|_{m=1} + t_{\text{rnand}} \Big|_{m=2} + t_{\text{finv}} \Big|_{m=3}$$

$$t_{\text{inv}} \Big|_{m=1} = t_{\text{fo}} + \alpha_{\text{pu}} \text{cm min}$$

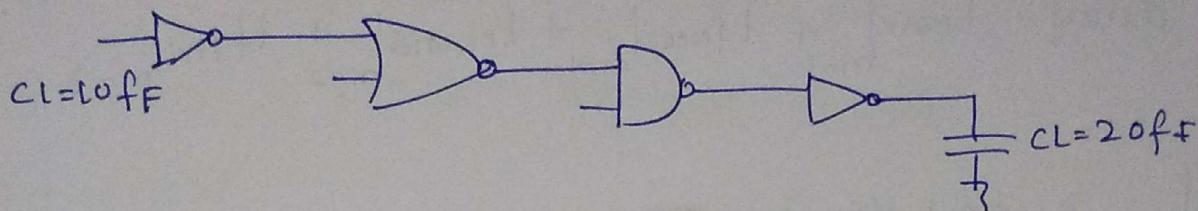
$$\begin{aligned} t_{\text{fnor2}} \Big|_{m=1} &= \frac{3}{2} t_{\text{fo}} + \alpha_{\text{nu}} \text{2cm min} \\ &= \frac{3}{2} t_{\text{fo}} + 2 \alpha_{\text{nu}} \text{cm min} \end{aligned}$$

$$\begin{aligned} t_{\text{rnand}} \Big|_{m=2} &= \frac{3}{2} t_{\text{fo}} + \frac{\alpha_{\text{pu}}}{2} \text{3cm min} \\ &= \frac{3}{2} t_{\text{fo}} + \frac{3}{2} \alpha_{\text{pu}} \text{cm min} \end{aligned}$$

$$\begin{aligned} t_{\text{finv}} \Big|_{m=2} &= t_{\text{fo}} + \alpha_{\text{nu}} (10 \text{min}) \\ &= t_{\text{fo}} + 10 \alpha_{\text{nu}} \text{cm min} \end{aligned}$$

$$\text{total delay} = \frac{7}{2} t_{\text{fo}} + \frac{5}{2} t_{\text{fo}} + 12 \alpha_{\text{nu}} \text{cm min} + \frac{11}{2} \alpha_{\text{pu}} \text{cm min}$$

3a. Consider the logic cascade shown in figure below. Use logical effort to find the relative size of each stage needed to minimize delay through the chain. Assume symmetric gates with $r = 2.5$



$$\hat{f} = p^N$$

$$N = 4$$

$$F = g \cdot H = \bar{g}_1 \cdot g_2 \cdot \bar{g}_3 \cdot g_4$$

$$g_{\text{NOT}} = g_1 = 1$$

$$g_{\text{NOR2}} = g_2 = \frac{2r+1}{r+1} = \frac{6}{3.5} = 1.71$$

$$g_{\text{NAND2}} = g_3 = \frac{r+2}{r+1} = \frac{4.5}{3.5} = 1.28$$

$$g_{\text{NOT}} = g_4 = 1$$

$$G = g_1 \cdot g_2 \cdot g_3 \cdot g_4 = 2.1888$$

$$H = \frac{C_{\text{out}}}{C_{\text{in}}} = \frac{20fF}{10fF} = 2F$$

$$F = g \cdot H = 3.6$$

$$\hat{f} = (F)^N = 1.377$$

$$\hat{f} = f_1 = f_2 = f_3 = f_4 = g_1 h_1 = g_2 h_2 = g_3 h_3 = g_4 h_4$$

$$h_1 = \hat{f}/g_1 = 1.377$$

$$h_2 = \hat{f}/g_2 = 0.805$$

$$h_3 = \hat{f}/g_3 = 1.075$$

$$h_4 = \hat{f}/g_4 = 1.377$$

$$h_4 = \frac{C_{out}}{C_{in3}} = \frac{C_5}{C_3} \quad C_{in4} = \frac{C_5}{h_4} = \frac{0.0f}{1.377} = 14.52f$$

$$h_{23} = \frac{C_{in}(NAND)}{C_{in2}} = \frac{C_5}{C_3}$$

$$C_{in}(NAND) = C_{in}(1+r) \cdot S_2 = 14.52f$$

$$C_{in}S_2 = 3.1226f \quad 4.14ef$$

$$h_3 = \frac{14.52f}{C_3} \Rightarrow C_3 = \frac{14.52f}{1.377} = 10.54f$$

$$\begin{aligned} C_{in}(NOR) &= C_{in}(1+r) \cdot S_2 = 10.54f \\ &= C_{in}S_2 = 2.124f \quad 1.756f \end{aligned}$$

$$h_2 = \frac{10.54f}{C_2} = C_2 = \frac{10.54f}{1.377} = 7.654f$$

$$C_{in}(NAND) = C_{in}(2+r) = 7.654f$$

$$C_{in} = 1.700$$

$$\begin{aligned} \$ & D = NF^{VN} + P \\ & = 4f + P \\ & = 4(1.377) + P \\ & = 5.508 + P \end{aligned}$$

3b. Discuss the issues with Dynamic CMOS logic, and analyze how Domino logic can overcome these issues with an example.

→ Charge sharing reduces the voltage on the O/P node. To keep this high the capacitors must satisfy $C_{out} = C_1 + C_2$. This may be difficult to achieve since the capacitance values are determined by the layout dimensions. After charge sharing takes place the node is still subject to charge leakage which continues to drop the voltage with time.

Domino logic is a CMOS logic style obtained by adding a static inverter to the outputs of the basic dynamic gate circuit. The precharge and evaluate events still occurs in this logic. and Domino logic gates are noninverting because the output is inverted.

