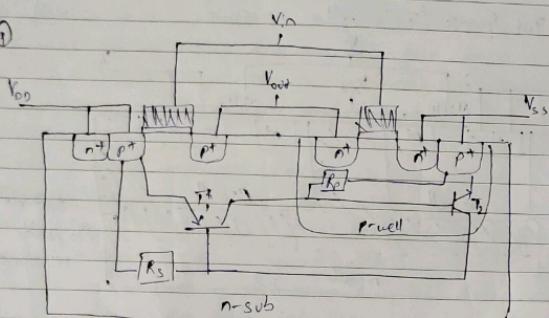
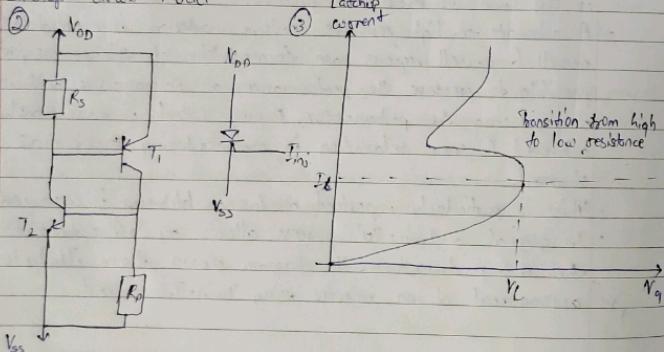


* Latch-Up in CMOS circuits.

①



* Latchup Circuit Model



- A problem which is inherent in the n-well & p-well process is due to the relatively large no. of j's which are formed in these structures as mentioned earlier, due subsequent presence of parasitic transistors & diodes.

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- Latch-Up is a condⁿ in which the parasitic components give rise to the establishment of low resistance conducting paths b/w V_{DD} & V_{SS} with disastrous results. Careful control during fabrication is necessary to avoid this problem.

- Latch-Up may be induced by glitches on the power supply rail or by incident radiation. The mechanism involved may be understood by referring diagram 1, which shows the key parasitic components associated with a p-well structure in which an inverter cell has been formed.

- It is observed that 2 transistors & 2 resistors (associated with the p-well & n-well region of the substrate) which form a path b/w V_{DD} & V_{SS} . If sufficient substrate current flows to generate enough voltage across ' R_s ' to turn ON transistor T_1 , this will then draw current through ' R_p ' & if voltage developed is sufficient ' T_2 ' transistor will also turn ON, establishing a self sustained low resistance path b/w the supply rails. If the current gains of the 2 transistors are such that $[B_1 \times B_2 > 1]$

latch-up may occur. Equivalent circuit is given in diagram 2.

- With no injected current the parasitic transistors will exhibit high resistance, but sufficient substrate current draw will cause switching to low resistance state. The switching characteristics of arrangement is outlined in diagram 3.

- Once latched up, this conⁿ will be maintained until the latch-up current drops below I_c , it is essential for CMOS process to ensure that V_c & I_c are not readily achieved in any normal mode of operation.

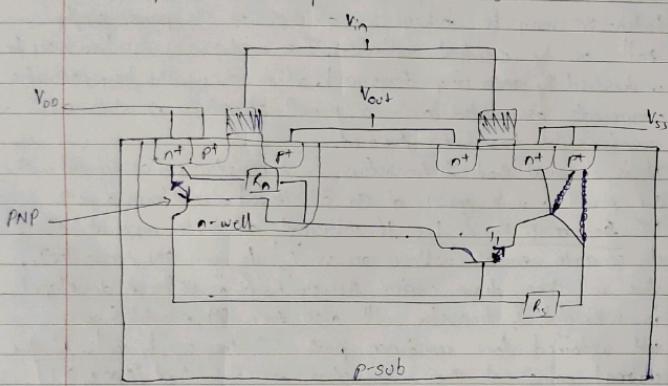
- Remedies for latch-up problem include

1. An increase in substrate doping levels with a consequent drop in the value of R_s

2. Reducing R_p by control of fabrication parameters & by ensuring
 a low contact resistance to V_{ss} .

3. 2nd Use of Guard ring may solve the issue.

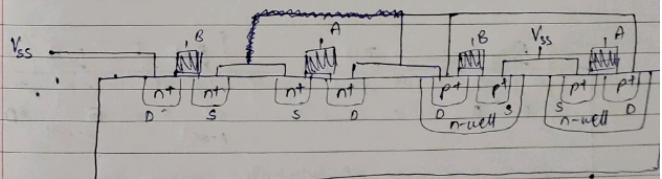
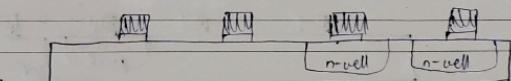
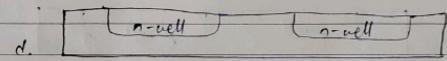
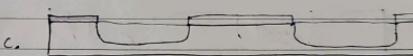
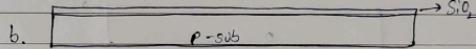
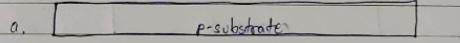
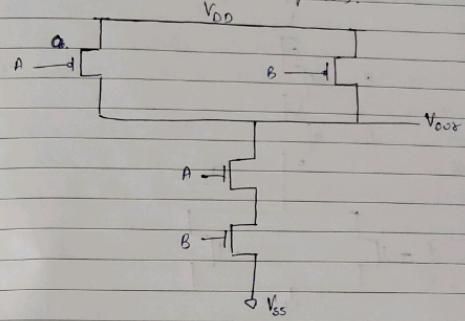
* n-well process Latch-up cell in CMOS ORS.



Q. NAND gate Layout with n-well process.

Q. NOR gate Layout with p-well process.

* NMOS gate Layout with n-well process.



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mos & BiCMOS Circuit Design Processes

- * MOS layers
 - MOS circuits are basically formed by 4 layers.
 - i. metal
 - ii. Polysilicon
 - iii. N diffusion
 - iv. P⁺
 - The thin oxide (SiO₂) layer includes n-diffusion, p-diffusion & transistor channel.
- * Stick diagram
 - " " are means of capturing topography & layer information using simple diagrams.
 - They convey layer info through color codes (or monochrome encoding).
 - Acts as an interface b/w symbolic & actual layout.
 - They show all comps/vias (contacts), relative placement of comps. & helps in planning & routing. It goes one step closer to layout.
 - They do not show exact placement of comps, transistor sizes, length & width of wires also the boundaries. We can say that it does not give any low level details.
- * Procedure to draw Stick Diagram.
 1. Draw 2 metal lines / power rails providing sufficient space to accommodate all transistors i.e. V_{DD} & V_{SS}.
 2. Draw demarcation line in the middle of 2 power lines.
 3. Draw P⁺ diff above N⁺ diffusion below demarcation.

metal M1 - Blue
" M2 - Grey
N⁺, P⁺ - green
Poly - Red

Dashed yellow - n well
Contact/via - 'X' mark.

4. Draw Polysilicon to represent PMOS & NMOS which represents gates of the transistors.

5. Connect source terminal of transistors to supply.

6. Drain terminals of transistors are connected using metal 1.

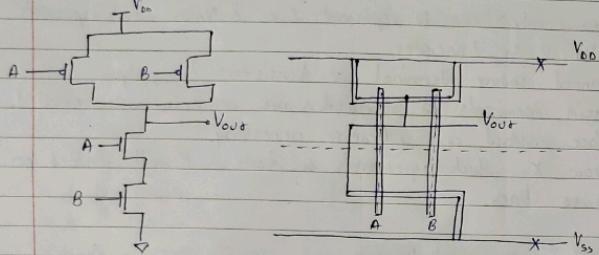
7. Place contact cuts wherever necessary.

8. Draw X which represents substrate & P-well contact on power lines.

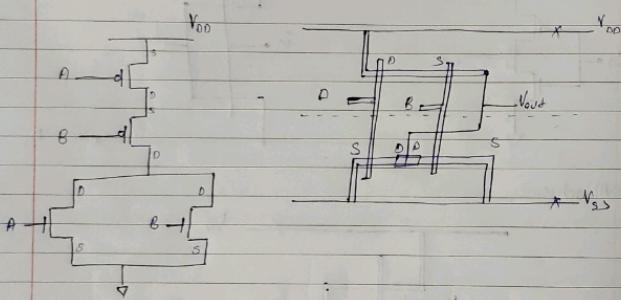
* CMOS Inverter Stick Diagram

Monochrome

* NAND Gate



* NOR Gate

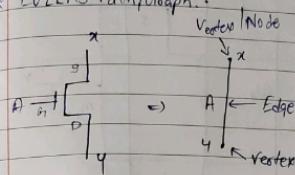


* Colour encoding, notation.

- Metal m_1 - Blue
- Metal m_2 - Grey
- n^+ - Green
- Poly - Red
- Dotted line - yellow ! n-well.
- Contact/Via - 'x' mark.

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* EULER'S Path/Graph..



FET

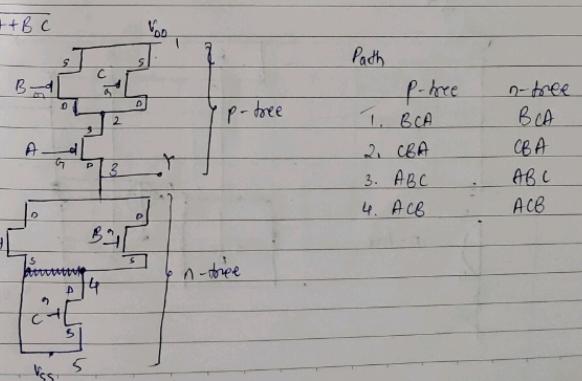
Graph Representation

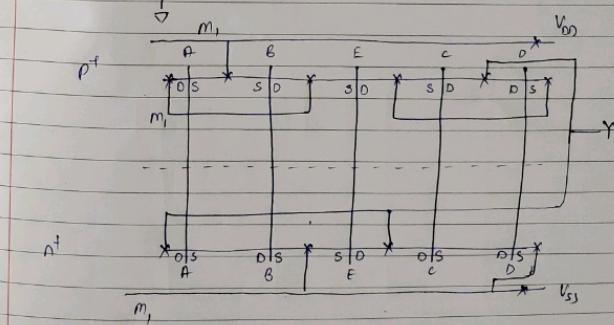
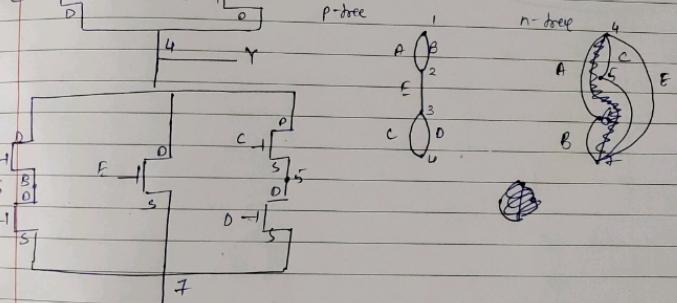
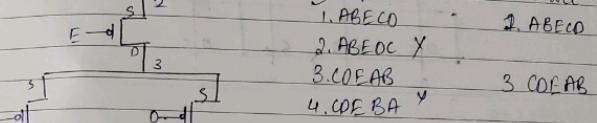
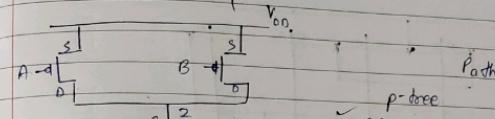
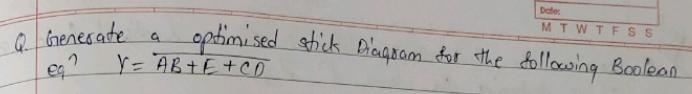
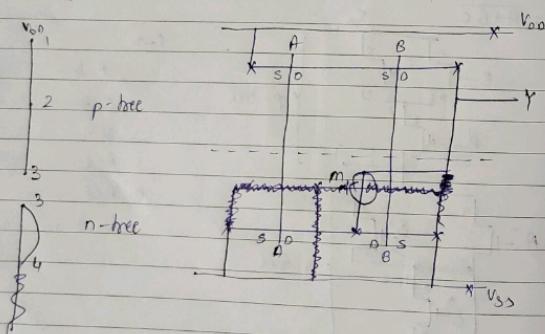
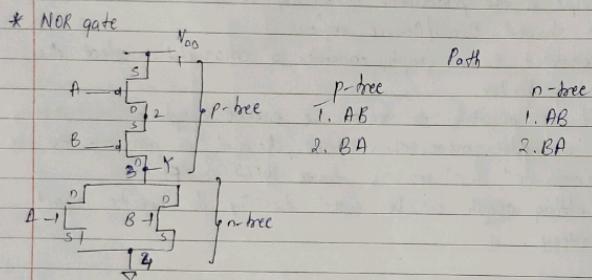
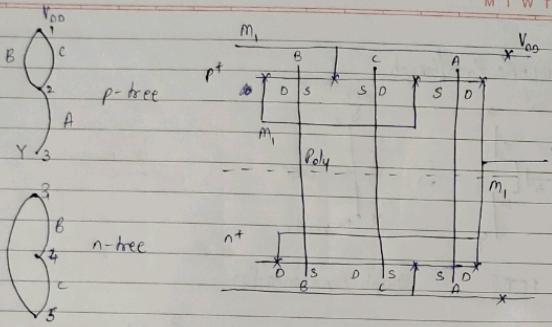
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- It helps in the placement & wiring of ckt's where the transistors have shared Drain/Source regions.
- To construct Euler graph, consider a CMOS ckt & select the starting vertex.
- If it is possible to trace the entire graph without passing over an edge more than once, then it is possible to use common n^+ & p^+ regions for NEET & PEET.
- Resulting graph can be used directly to create layout strategy.

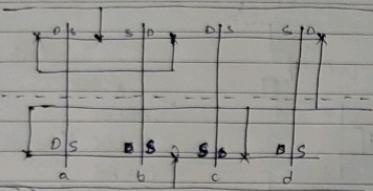
Ex:

$$Y = \overline{A} + BC$$





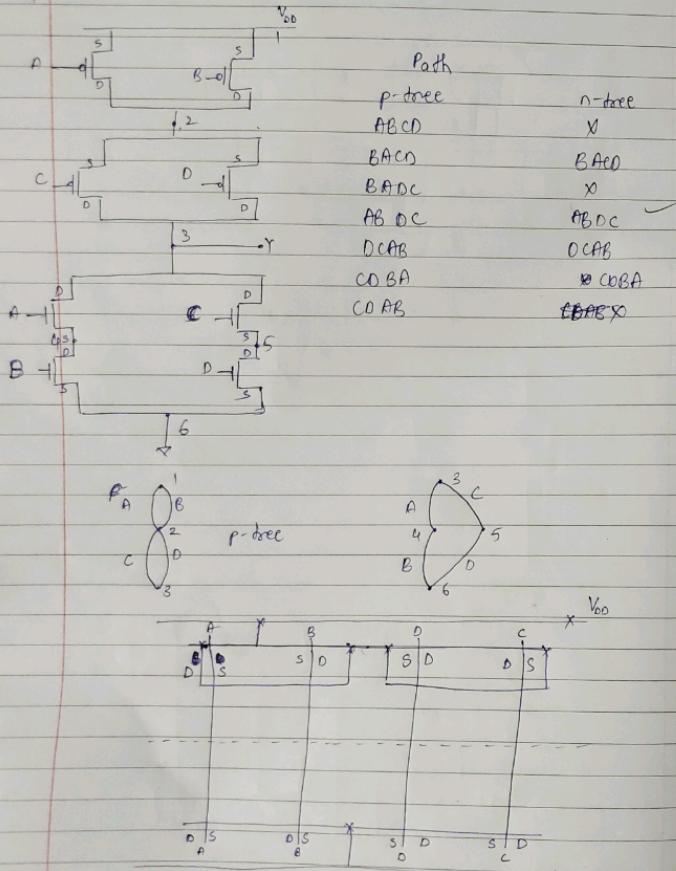
for Q
Q. Examine the stick diagram below. Is this a functional logic gate?
If so, determine the logic of it if possible.



$$\Rightarrow Y = AB + C + D$$

Q. $Y = \overline{AB} + CD$

\Rightarrow



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* Layout Design Rules

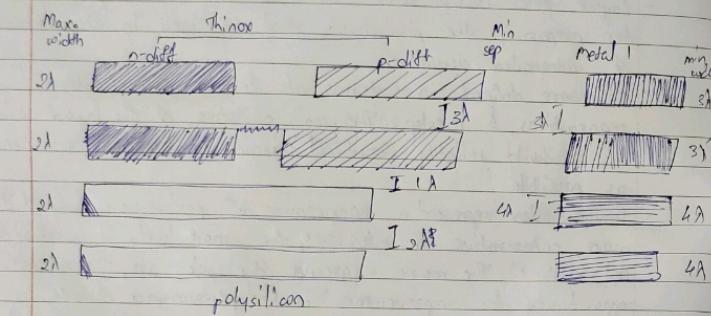
- Layout rules (design rules) can be considered a prescription for preparing the photomask that are used in the fabrication of integrated circuits.
- Rules are defined in terms of features sizes (widths), separations, & overlaps. The main objective of the layout rules is to build reliable functional circuits in as small an area as possible.
- Design rules represent a compromise b/w performance & yield. The more conservative the rules are, the more likely it is that the chip will fail. The more aggressive the rules are, the greater the opportunity for improvements in chip performance & size.
- They specify the designer certain ~~aggressive~~ geometric constraints on the layout artwork so that patterns on the processed wafer will preserve the topology & geometry of the designs.

* MOSIS (Metal Oxide Semiconductor Implementation Service)

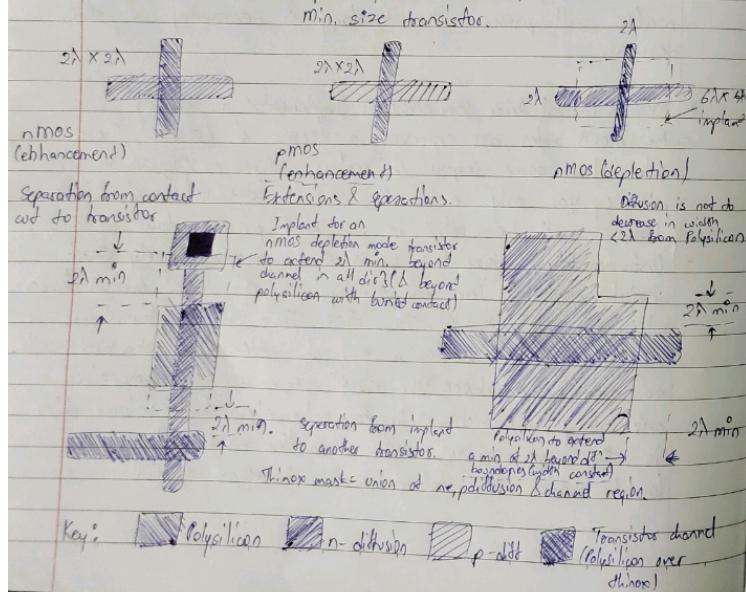
- The MOSIS rules are expressed in terms of 'Lambda'. These rules allow some degree of scaling for processes, as in principle, you only need to reduce the value of λ & the designs will be valid in the next process down in size.
- Unfortunately, history has shown that processes rarely shrink uniformly. Industry usually uses the actual micron design rules for layouts. At this time, custom layout is usually constrained to a no. of often-used standard cells. e.g. memories, where the effort expended is amortized over many instances. Only for extremely high-volume chips is the cost savings of a smaller ~~cost~~ custom layout worth the labour cost of that layout.

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* Design rules for wires (nmos & pmos)

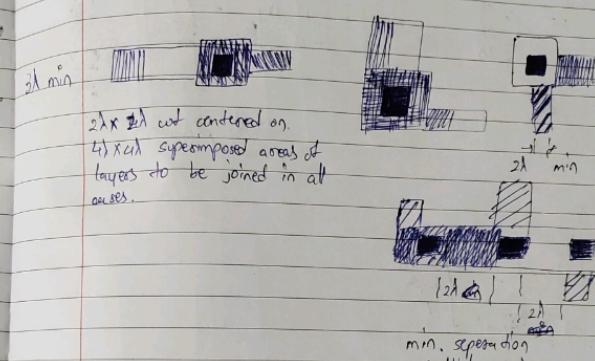


* Transistor Design rules (pmos, nmos & emos)

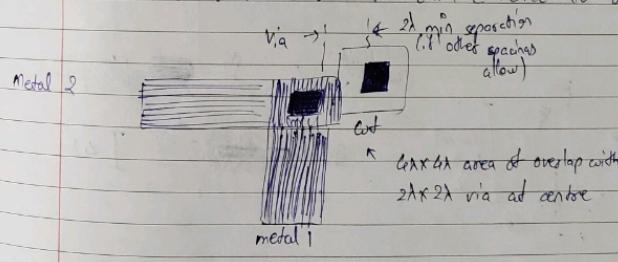


* Contacts (nmos & pmos)

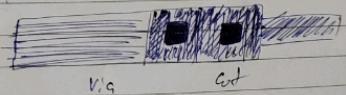
1. metal 1 to polysilicon or to diffusion.

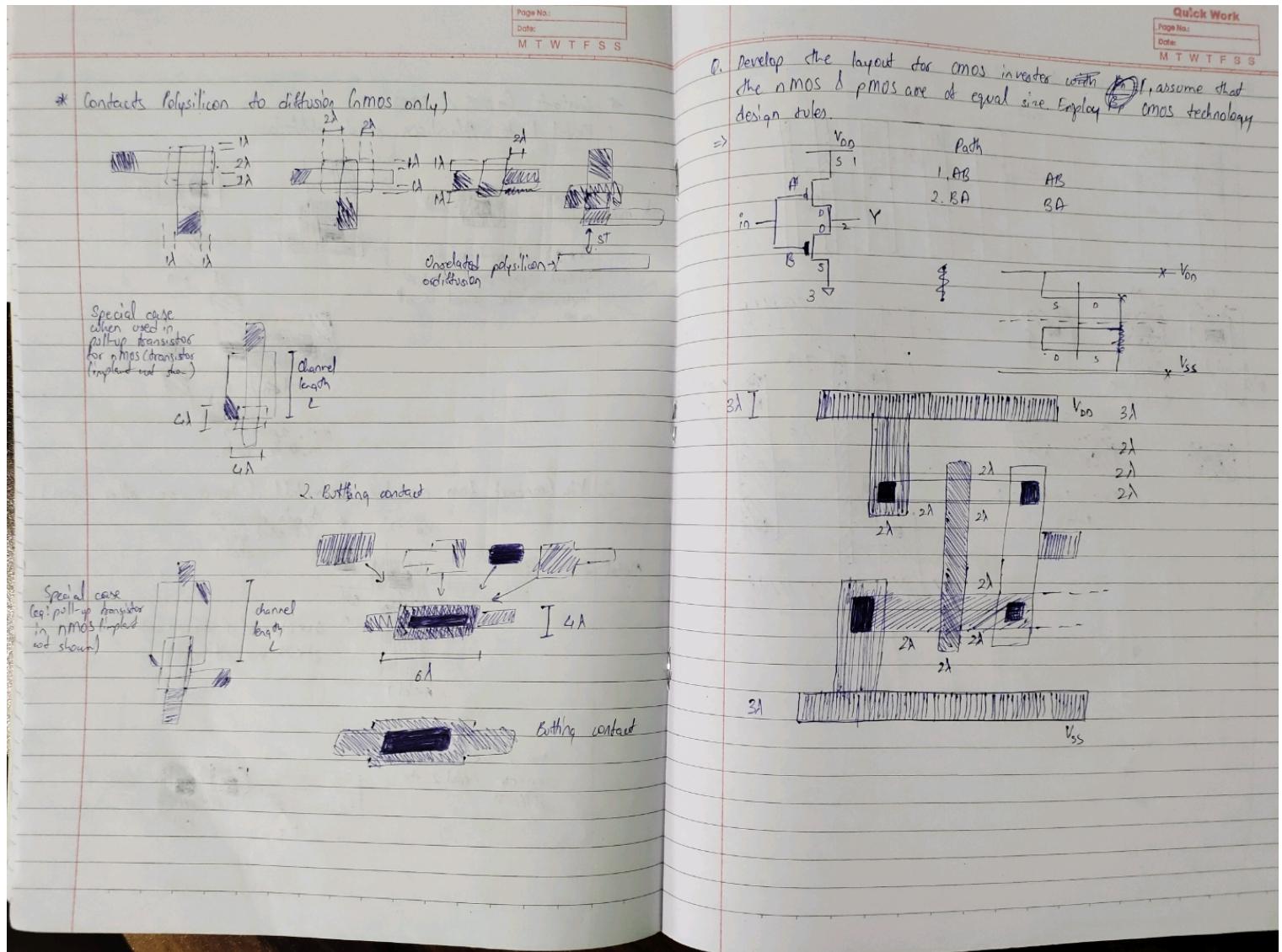


2. via (contact from metal 2 to metal 1 & hence to other layers)

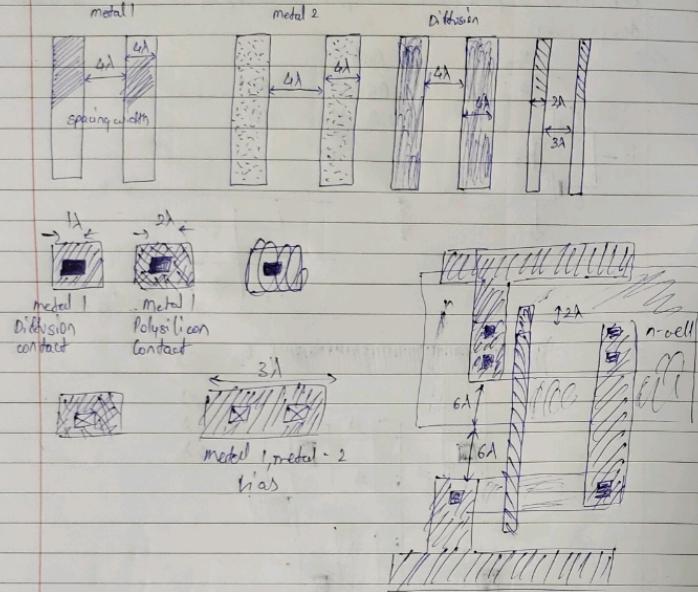


via & cut used to connect metal 2 to diffusion

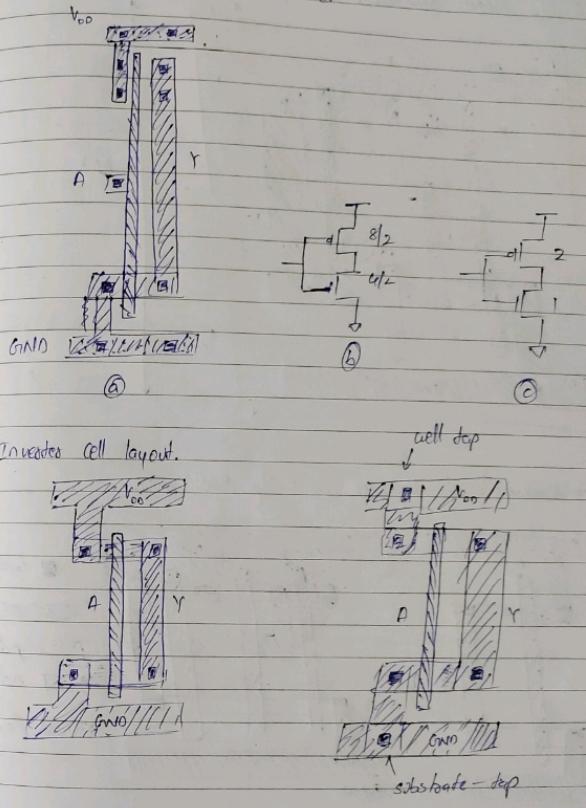




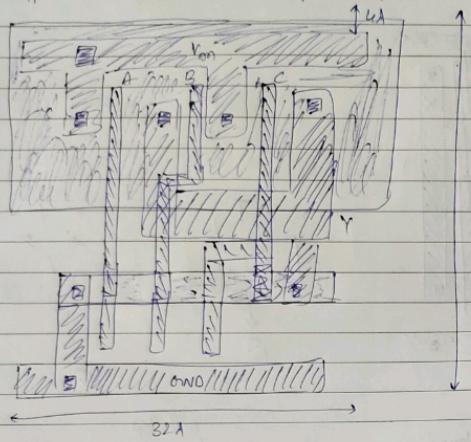
* Simplified λ -based design rules.



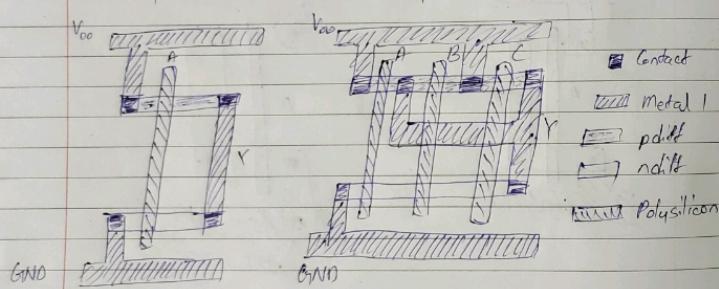
* Inverted with dimensions labelled.



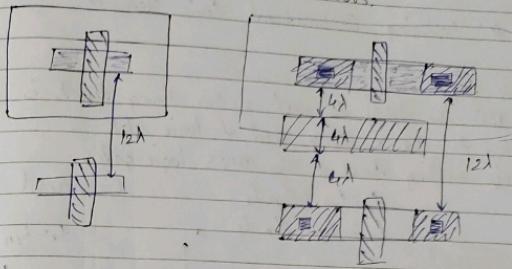
* 3 i/p NAND standard cell gate layouts.



* Stick diagrams of inverter & 3 i/p NAND gate

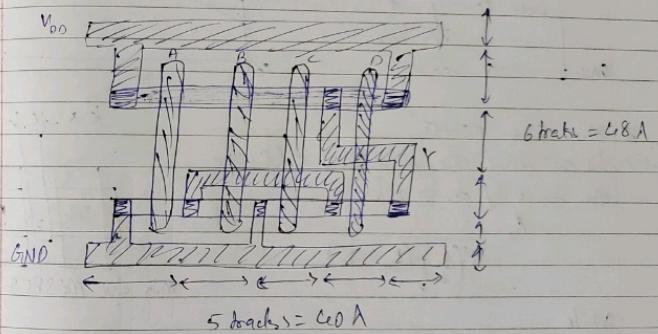


* Spacing b/w nMOS & pMOS transistors.



a. Sketch a stick diagram

$$Y = (A + B + C) \cdot D$$



Cell size 60λ by 68λ

Ch 4: Designing Combinational Logic Networks.

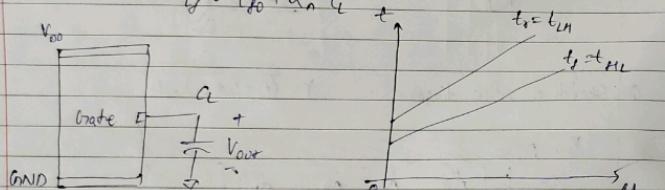
* Gate Delay

- In VLSI, the ability to meet system timing targets is intimately related to the switching speed of logic cells.

- off switching times of the CMOS logic gates.

$$t_{off} = t_{off} + \alpha_p C_L \quad C_L - \text{external load.}$$

$$t_{off} = t_{off} + \alpha_n C_L \quad t$$



* Min. size MOSFET

- We can define the parasitical R & C for the device by design rules

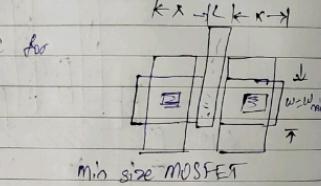
$$R_p = \frac{K' (w/L)}{I_{off}} (V_{DD} - V_0)$$

while

$$C_{ov} = C_{ox} (W/L)$$

$$C_{ov} = (C_{ox} + C_{obs})$$

$$C_{sv} = (C_{ox} + C_{sg})$$



To create a design methodology, we will specify that all transistors size are integer multiples of the min. width

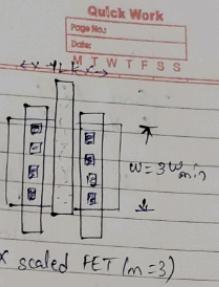
$$W_{min} = W_0$$

Unseen ch 8:

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$$\left(\frac{w}{L}\right)_m = m \left(\frac{w}{L}\right)_0$$

with $m = 1, 2, 3, \dots$ as the size specifier



* mX scaled FET

Resistance & gate cap. of the m-size FET are written in terms of the unit transistor ab.

$$R_m = \frac{R_0}{m} \quad C_{gm} = m C_{g0}$$

$$C_{ov} = m C_{ov0} \quad C_{sv} = m C_{sv0}$$

$$\Rightarrow [R_m C_m = R_0 C_0 = \text{constant}]$$

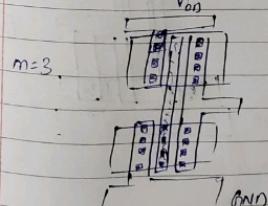
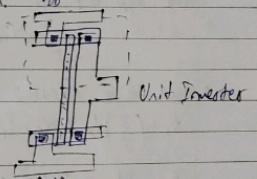
; True by Scaling Theorem.

* Inverter Using Scaled Transistor

- Rise time & Fall-time with scaled tech. V_{DD}

$$t_{ov} = t_{off} + \alpha_p C_L$$

$$t_{af} = t_{off} + \alpha_n C_L$$



- Since $R_p > R_n$, $t_{ro} > t_{fo}$ & $\alpha_{pu} > \alpha_{nv}$ for a given load G ,
for V_{DD} : The midpt voltage

$$V_m = \frac{V_{DD} - |V_{DD}| + \alpha_{pu} G}{1 + \sqrt{s}}$$

where $s = \left(\frac{Nn}{Mp}\right)$ is the mobility ratio

- The i/p cap. is a min. value for a complementary pair.
 $C_{in} = 2C_0 = C_{min}$

- However, this does not change midpt voltage, but does affect switching time.

- Response time for new ckt ($m=3$)

- The zero-load times t_{ro} & t_{fo} are ($\alpha_{pu} G$) constants & the slope parameter will decrease as $(1/m)$ because of the decrease in resistance by some factor

$$t_{ro} = t_{ro} + \frac{\alpha_{pu} G}{3}$$

(order $s=3$)

$$t_{fo} = t_{fo} + \frac{\alpha_{pu} G}{3}$$

The i/p cap. for this gate is:

$$\therefore C_{in} = 3C_{min} \quad (\text{order } s=3)$$

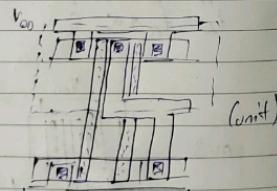
- Min. size NAND2

$$t_{ro} = \left(\frac{3}{2}\right) t_{ro} + \alpha_{pu} G$$

$$t_{fo} = 3t_{fo} + 2\alpha_{pu} G$$

Since an nFET/pFET pair consists
of min. size devices, i/p cap. is

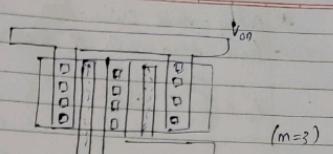
$$C_{in} = C_{min}$$



- NAND2 with ($m=3$)

$$t_{ro} = \left(\frac{3}{2}\right) t_{ro} + \frac{\alpha_{pu}}{3} G$$

$$t_{fo} = 3t_{fo} + \frac{2\alpha_{nv}}{3} G$$



The i/p cap. is

$$C_{in} = 3C_{min}$$

$$t_{ro} = \left(\frac{N+1}{2}\right) t_{ro} + \frac{\alpha_{pu}}{m} G$$

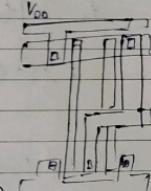
$$t_{fo} = (N+1)t_{fo} + \frac{N\alpha_{nv}}{m} G$$

$$C_{in} = mC_{in} \quad \boxed{\text{For N-i/p NAND gate, m-sized FET}}$$

- m/iN size NOR2

$$t_{ro} = 3t_{ro} + 2\alpha_{pu} G$$

$$t_{fo} = \left(\frac{3}{2}\right) t_{fo} + \alpha_{nv} G$$



for ($m=3$)

$$t_{ro} = 3t_{ro} + \frac{2\alpha_{pu}}{3} G$$

$$t_{fo} = \left(\frac{3}{2}\right) t_{fo} + \frac{\alpha_{nv}}{3} G$$

$\ddot{\text{f}}_{DOS}$ N-i/pS

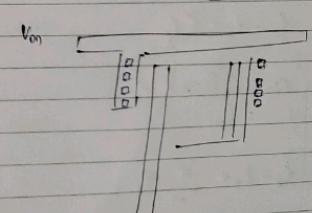
$$t_{ro} = (N+1)t_{ro} + \frac{N\alpha_{pu}}{m} G$$

$$t_{fo} = \left(\frac{N+1}{2}\right) t_{fo} + \frac{\alpha_{nv}}{m} G$$

$$C_{in} = mC_{in}$$

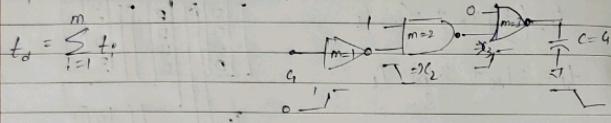
$N \rightarrow$ fan in (i/pS)

$m \rightarrow$ Transistor scaling factor



* Delay-time estimation

logic chain with m stages,



$$t_d = t_{NOT} I_{m=1} + t_{NOT} I_{m=2} + \dots + t_{NOT} I_{m=m}$$

$$t_{NOT} I_{m=1} = t_{d0} + \alpha v_{min}$$

$$t_{NOT} I_{m=2} = \left(\frac{3}{2}\right) t_{d0} + \alpha v_{min}$$

$$t_{NOT} I_{m=3} = \left(\frac{5}{2}\right) t_{d0} + \alpha v_{min}$$

$$t_d = \left(\frac{5}{2}\right) t_{d0} + \left(\frac{10}{3}\right) \alpha v_{min} + \left(\frac{3}{2}\right) t_{d0} + \left(\frac{3}{2}\right) \alpha v_{min}$$

$$= \frac{1}{2} (5t_{d0} + 3t_{d0}) + \left[\left(\frac{10}{3}\right) \alpha v_{min} + \left(\frac{3}{2}\right) \alpha v_{min}\right] v_{min}$$

→ General Equations

$$t_d = t_{d0} + \alpha' C_L$$

$$C_{in} = C_p(1+\delta)$$

$$= C_p$$

$$t_d = t_{d0} + \frac{\alpha'}{m} C_L$$

$$\beta_n = \beta_p, w_n = w_{min} \quad \& \quad w_p = \beta_p + w_{min}$$

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* Driving Large Capacitive Loads

High speed design can be obtained from studying the characteristic delay through inverter.

$$\left(\frac{V_o}{I}\right)_p = \sigma \left(\frac{V_o}{I}\right)_n$$

$$T = R C_{out} = R (C_{FFL} + C_L)$$

$$\delta = \frac{M_p}{M_n} = \frac{k_n}{k_p} > 1$$



$$R_n = R_p = R = \frac{1}{\beta(V_{DD} - V_T)}$$

$$\alpha \times R = \frac{1}{\beta(V_{DD} - V_T)}$$

$$R_{FFL} V_m = V_{DD}/2$$

$$V_{out}(t) = V_{DD} [1 - e^{-t/\tau}]$$

$$C_{in} = C_{out} + C_{dp}$$

$$= C_{ox} (A_{on} + A_{dp})$$

(p-n/w precharge δ^n) /

$$C_n = C_{ox} L [w_n + w_p]$$

$$= (1+\delta) (C_{ox} L w_p)$$

$$= (1+\delta) C_{on}$$

$$V_{out}(t) = V_{DD} e^{-t/\tau_n}$$

(n-p/w discharge δ^n) /

* Unit load

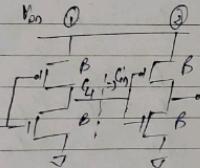
load cap same as gate's own cap

i.e. unit load value.

$$C_{ut} = C_{in} \quad (\text{unit load})$$

$$t_{sr} = t_d + \alpha' C_{in} \quad (\text{switching time})$$

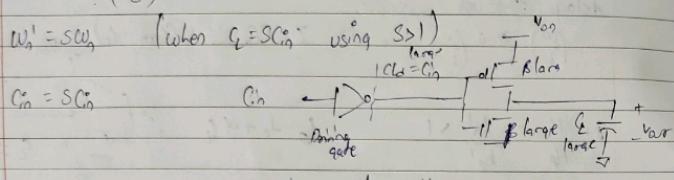
$$\beta' = SB \quad (\text{when } C_L \gg C_{in} \text{ using } s \gg 1)$$



$$\beta' = \frac{R}{S} \quad \alpha' = \frac{\alpha}{S}$$

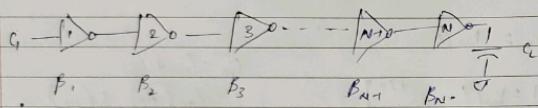
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$$t_o = t_o + \left(\frac{d}{s}\right) C \quad (\text{new switching time})$$



Driving a large i/p cap gate.

* Delay minimization of Inverter cascade, ideal case



C_i - i/p cap R_i - FET res. β_i - device transconductance.
 $\beta_1 < \beta_2 < \beta_3 < \dots < \beta_{N-1} < \beta_N$ $\beta_j = S^{(j-1)} \beta_1$

$$\beta_2 = S\beta_1$$

$$\beta_j = S^{(j-1)} \beta_1$$

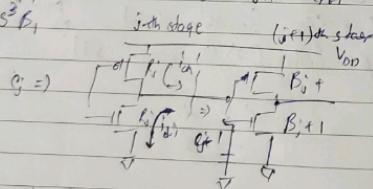
$$\beta_{j+1} = S\beta_j$$

$$R_j = \frac{R}{S^{(j-1)}}$$

$$\beta_2 = S\beta_1$$

$$\beta_3 = S\beta_2 = S^2\beta_1$$

$$\beta_4 = \beta_3 = S^3\beta_1$$



$T_d = T_1 + T_2 + T_3 + \dots + T_{N-1} + T_N$
 $= R_1 C_1 + R_2 C_2 + R_3 C_3 + \dots + R_{N-1} C_{N-1} + R_N C_N$

$$C_i = C_{in} +$$

$$= S^n C_1$$

$$T_d = R_1 S C_1 + \frac{R_1 S^2 C_1}{S^2} + \frac{R_1 S^3 C_1}{S^3} + \dots + \frac{R_1 S^{N-1} C_1}{S^{N-1}} + \frac{R_1 S^N C_1}{S^N}$$

$$T_d = S R_1 C_1 + S R_2 C_2 + S R_3 C_3 + \dots + S R_{N-1} C_{N-1} + S R_N C_N$$

$$T_d = N S T_o \quad \text{where } T_o = R_1 C_1$$

$$C_i = S^n C_1$$

$$\ln(S^n) = \ln\left(\frac{C_i}{C_1}\right) = N \ln(s)$$

$$\Rightarrow N = \frac{\ln\left(\frac{C_i}{C_1}\right)}{\ln(s)}$$

$$T_d = T_o \ln\left(\frac{C_i}{C_1}\right) \left[\frac{S}{\ln(s)} \right]$$

$$\frac{\partial T_d}{\partial S} = \frac{\partial}{\partial S} \left[\frac{S}{\ln(s)} \right] = 0$$

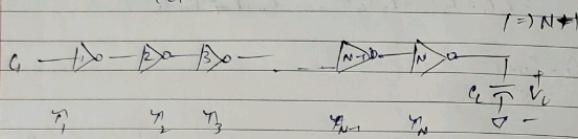
$$\frac{1}{\ln(s)} - \frac{S}{S[\ln(s)]^2} = 0$$

$$\text{or } \ln(s) = 1$$

$$S = e$$

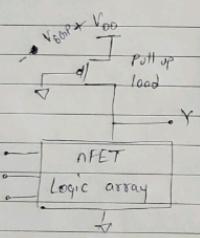
$$N = \frac{\ln\left(\frac{C_i}{C_1}\right)}{\ln(s)} = \ln\left(\frac{C_i}{C_1}\right)$$

$$T_d = e \ln \left(\frac{I_o}{I_s} \right) t_0$$

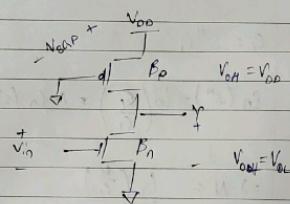


Time-constants in Cascade

* Pseudo nMOS



Pseudo-nMOS Inverter :



Radiced logic

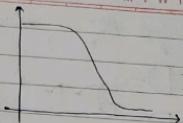
non - satⁿ $i_{DN} = i_{DN}$ \rightarrow satⁿ

$$\frac{\beta_n}{2} [2(V_{DD} - V_{TN}) V_{OL} - V_{OL}^2] = \frac{\beta_P}{2} (V_{DD} - |V_{TP}|)^2 - \text{Quadratic eq for } V_{OL}$$

$$V_{OL} = (V_{DD} - V_{TN}) - \sqrt{(V_{DD} - V_{TN})^2 - \frac{\beta_P}{\beta_n} (V_{DD} - |V_{TP}|)^2}$$

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V_{OL} : V_{OL} depends on $\frac{\beta_P}{\beta_n} > 1$ V_{OL}



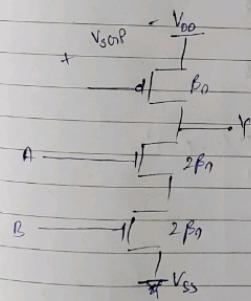
Advantages of Pseudo nMOS

- Uses few transistors because only NFET logic block is required to create the logic.
- Total no. of transistors required in pseudo nMOS logic is $n+1$ FET's, where n is no. of ilps in a logic blk.
- Used to reduce FET count & area.

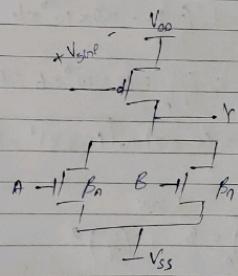
Disadvantages

- Pseudo nMOS logic family is more complicated because of sizing of transistors set, the numerical value of V_{OL} & proper care must be taken to ensure that V_{OL} is small.
- Pseudo nMOS logic is passived logic.

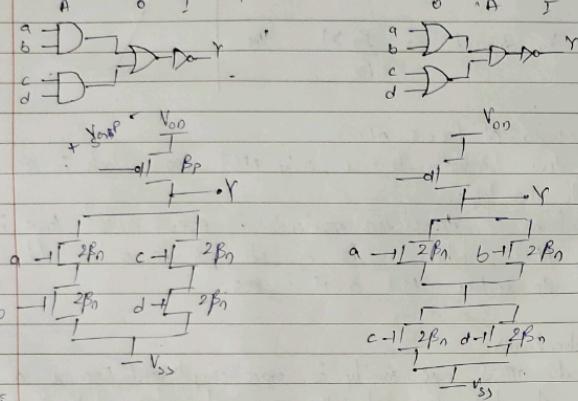
NAND2



NOR2



Q. Develop AOI 22 using Pseudo nmos logic.



Q Consider a CMOS process with $V_{DD} = 5V$, $V_{TN} = 0.7V$, $V_{TP} = -0.8V$, $k_n' = 150 \text{ MA/V}^2$, $k_p' = 68 \text{ MA/V}^2$. A pseudo nMOS inv sized with $(W/L)_n = 4$, $(W/L)_p = 6$ estimate V_{OL} & V_{OH} .

$$\Rightarrow V_{OH} = 5V$$

$$P_n = k_0' \left(\frac{w}{\Sigma} \right)_n = 150 \times 10^{-6} \times 4 = 6 \times 10^{-4}$$

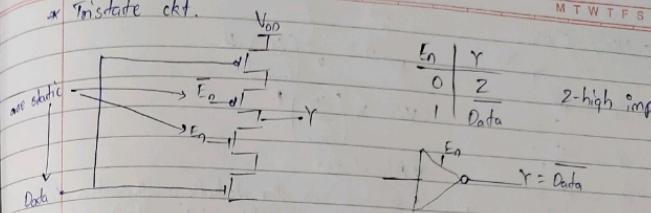
$$V_0 = (15 - 0.7) - \frac{\sqrt{(15 - 0.7)^2 - 4 \cdot 0.08 \times 10^4 \cdot (15 - 0.81)^2}}{6 \times 10^4}$$

$$V_{o_2} = 1.25V$$

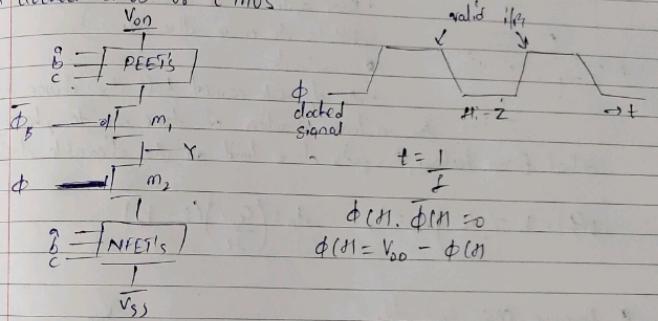
$$V_{21} = 0.239 \sqrt{}$$

Quick Work

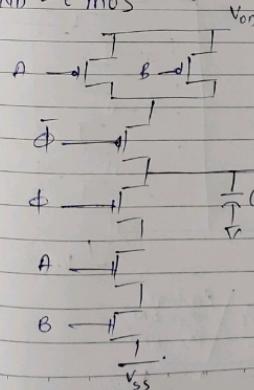
* Tristate ckt.



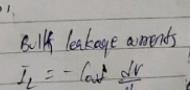
* Clocked CMOS or C²MOS



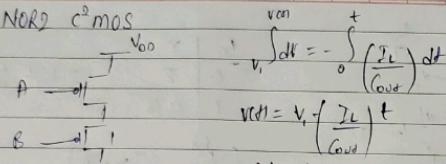
NAND - c²mos



$$\begin{aligned}
 & \text{charge leakage} \\
 & \text{off } I_{\text{on}} \quad i_{\text{out}} = i_{\text{in}} - i_p \\
 & \text{on } I_{\text{on}} \quad i_{\text{out}} = i_{\text{in}} + i_p \\
 & \text{off } I_{\text{off}} \quad i_{\text{out}} = i_{\text{in}} + i_p \\
 & \text{on } I_{\text{off}} \quad i_{\text{out}} = i_{\text{in}} - i_p
 \end{aligned}$$



* NOR2 CMOS



• Advantages

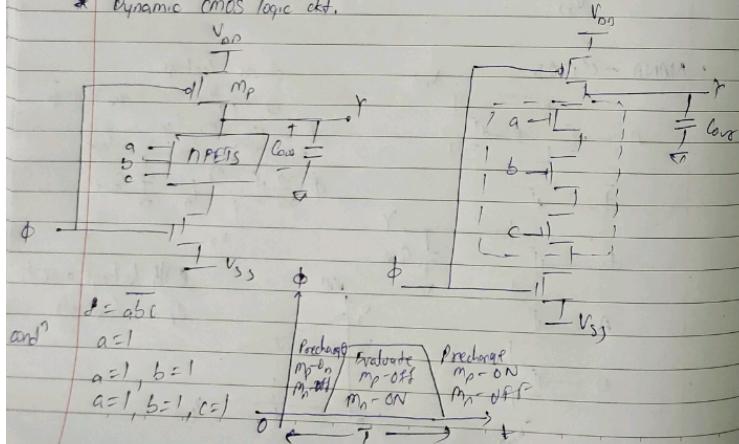
- synchronizes the dataflow through a logic cascade by controlling int. op² of gate
- every cycle of φ allows a new group of bits to enter the n/w

• Drawbacks

- the d/p node cannot hold the charge on VDD for a longer duration of time due to phenomena called charge leakage, this puts alone limit on the allowable clock freq.

$$V(t_h) = V_i - \left(\frac{I_L}{V_{DD2}} \right) t_h = V_x \quad t_h = \left(\frac{C_{out}}{I_L} \right) (V_i - V_x)$$

* Dynamic CMOS logic dft.



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* Logical Effort

- logical effort characterizes gate & how they interact in logic cascades, & provides techniques to minimize the delay
- Basic dft starts with an inverter & uses a symmetric NOT gate, where $F_n = F_p$

$$\left(\frac{W}{L} \right)_p = \delta \left(\frac{W}{L} \right)_n$$

- logical effort q of a gate is defined by the ratio of capacitance to that at the reference gate.

$$q = \frac{C_n}{C_{ref}}$$

Ref. inverter for logic gate

- For the IX inv., since $C_n = C_{ox}(A_{in} + A_{op})$, $A_{in} = W_p L$ & $A_{op} = W_p L$

Since $W_p = \delta W_n$

$$\begin{aligned} C_n &= (C_{ox} L W_n) (1+\delta) \\ &= C_{in} (1+\delta) \\ &= C_{ref} \end{aligned}$$

$$q_{NOT} = \frac{C_{ref}}{C_{in}} = 1$$

* Electrical Effort

- h is defined by the capacitance ratio

$$h = \frac{C_{out}}{C_{in}}$$

- It is the ratio of electric drive strength that is required to drive C_{out} relative to that needed to drive its own i/p capacitance C_{in} .

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Absolute delay time through inverter.

$$d_{abs} = k R_{ref} (C_{p,ref} + C_{out})$$

$$R = \frac{R_{ref}}{S}$$

$$C_p = S C_{p,ref}$$

$$d_{abs} = k R (C_p + C_{out})$$

$$= k \frac{R_{ref}}{S} (S C_{p,ref} + C_{out})$$

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$$k = \ln(2) \approx 2.2$$

$$C_n = S C_{out}$$

$$d_{abs} = k \frac{R_{ref}}{S} S C_{p,ref} + k \frac{R_{ref}}{S} C_{out}$$

$$= k R_{ref} C_{p,ref} + k \frac{R_{ref}}{S} \left(\frac{C_{out}}{C_{out}} \right) C_{out}$$

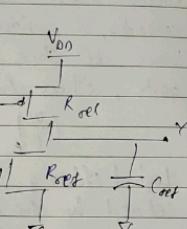
$$= k R_{ref} C_{p,ref} + k R_{ref} C_{out} \left(\frac{C_{out}}{C_{in}} \right)$$

$$\bar{T} = k R_{ref} C_{out}$$

$$d_{abs} = T / (k + p)$$

$$P = \frac{\bar{T}_{par}}{T} = \frac{R_{ref} C_{p,ref}}{R_{ref} C_{out}}$$

$$d = \frac{d_{abs}}{T} = h + p$$



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• 2 stage inverter chain

Total path delay ΔD is sum of individual delays

$$D = d_1 + d_2 = (h_1 + p_1) + (h_2 + p_2)$$

$$h_1 = \frac{C_2}{C_1}, \quad h_2 = \frac{C_3}{C_2} \quad \Rightarrow \quad \frac{1}{C_1} \rightarrow \frac{1}{C_2} \rightarrow \frac{1}{C_3}$$

$$H = \frac{C_{out}}{C_{in,ref}} \quad (\text{path electrical effort})$$

$$H = h_1 h_2$$

$$H = \left(\frac{C_2}{C_1} \right) \left(\frac{C_3}{C_2} \right) = \frac{C_3}{C_1}$$

$$h_2 = \frac{H}{h_1}$$

$$D = (h_1 + p_1) + \left(\frac{H + p_2}{h_1} \right)$$

$$\frac{\partial D}{\partial h_1} = \frac{1}{h_1} \left[(h_1 + p_1) + \left(\frac{H + p_2}{h_1} \right) \right]$$

$$\frac{\partial D}{\partial h_1} = 1 - H = 0 \quad \text{since } H = h_1 h_2$$

$$h_1 = h_2$$

The primary goal of logical effort is to minimize the delay time. The condition can be found by derivative

Path delay will be minimized if $h_1 = h_2$

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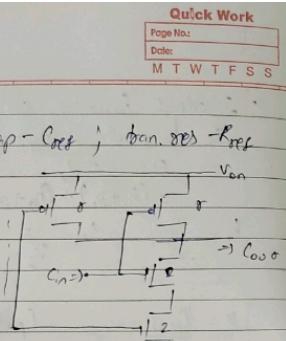
* Logical Effort Generalization

- IX Factorance inverter ; i/p cap - C_{ref} ; o/p res - R_{ref}

1. NAND2

$$C_{in} = C_{in}(2+s)$$

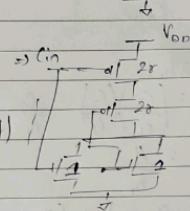
$$q_{NAND2} = \frac{C_{in}(2+s)}{C_{ref}} = \frac{2+s}{1+s} \text{ (logical effort)}$$



2. NOR2

$$C_{in} = C_{in}(1+2s)$$

$$q_{NOR2} = \frac{C_{in}(1+2s)}{C_{ref}} = \frac{1+2s}{1+s} \text{ (logical effort)}$$



General eq' for n i/p NAND & NOR gate.

$$C_{in} = C_{in}(n+s) \text{ (NAND2)}$$

$$q_{NAND} = \frac{n+s}{1+s} \text{ (logical of NAND2)} \quad q_{NOR} = \frac{1+n s}{1+s} \text{ (logical of NOR2)}$$

Delay through general gate is expressed as

$$d = q \cdot h + p$$

$$d = qh + p$$

Primary effect of logical effort parameter q is to modify 1st term to account for the difference in drive characteristics

For a logic cascade with n stages, each gate will be characterized by a delay of

$$d_i = q_i h_i + p_i$$

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Total path delay D is summation of all individual delays

$$D = \sum_{i=1}^N d_i = \sum_{i=1}^N (q_i h_i + p_i)$$

$$G = \prod_{i=1}^N q_i = q_1 q_2 \dots q_N \quad (\text{path logical effort})$$

$$H = \prod_{i=1}^N h_i = h_1 h_2 \dots h_N \quad (\text{path electrical effort})$$

$$F = G H \quad (\text{path effort})$$

$$= (q_1 h_1) (q_2 h_2) \dots (q_N h_N)$$

$$q_i h_i = \text{constant} = d \quad (\text{min delay}).$$

The optimum path effort is

$$q_h = \hat{d} = \frac{F}{\prod_{i=1}^N h_i} \quad (\text{min path delay})$$

$$h_i = \frac{\hat{d}}{q_i} \quad (\text{design reference})$$

The optimized path delay is given

$$\hat{D} = N F^{\frac{1}{N}} + P \quad (\text{min. path delay})$$

Parasitic delay due to each gate

$$P = \sum_{i=1}^N p_i$$

$$P = n p_{ref} \quad (n - \text{stage parasitic})$$

Q. Analyse the logic cascade & using logical effort.

i. Path logical effort.

$C_4 = 500 \text{ fF}$ $C_1 = 20 \text{ fF}$

Path logical effort

 $G_1 = g_{\text{NOT}} g_{\text{NAND2}} g_{\text{NAND2}}$
 $G_1 = (1) \left(\frac{1+2s}{1+s} \right) \left(\frac{2+s}{1+s} \right) = 2.2$

Path electrical effort

 $H = \frac{C_{\text{load}}}{C_{\text{total}}} = \frac{C_4}{C_1} = \frac{500}{20} = 25$

Path effort

 $F = GH = 55$

Optimum stage effort

 $f = F^{\text{opt}} = (55)^{1/3} = 3.8$
 $D = NF^{\text{opt}} + P$
 $= 3(3.8) + P$
 $= 11.41 + P$

sizing eq's are obtained from the analysis using the optimized quantities, starting from NAND2 gate at the o/p where

 $g_{\text{NAND2}} = \frac{n+s}{1+s} = \frac{4.5}{3.5} = 1.29$

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$h_3 = \frac{3.8}{1.29} = \frac{3}{9.3} = 2.95 = \frac{C_4}{C_3}$

$C_3 = \frac{500}{2.95} = 169.5 \text{ fF}$

Since C_3 is i/p cap. into NAND2 gate, we may use the eq?

$C_{\text{in}} = C_{\text{out}} (2+s)$ → write scaled gate as

$C_3 = S_2 C_{\text{in}} (2+s)$

$C_3 = S_2 (4.5 C_{\text{in}})$ NAND2

$g_{\text{NOR2}} = \frac{1+n+s}{1+s} = \frac{1+2(3.8)}{1+3.8} = 1.71$

$h_2 = \frac{3.8}{1.71} = 2.22 = \frac{C_3}{C_2}$

$C_2 = \frac{169.5}{2.22} = 76.35 \text{ fF}$

$C_2 = S_2 C_{\text{in}} (1+2s)$ NOR2

$C_2 = S_2 (6 C_{\text{in}})$

The i/p NOT gate is defined to have logical effort of 1

$h_1 = \frac{3.8}{1} = \frac{C_2}{C_1}$

$C_1 = 20 \text{ fF}$

The ref. NOT gate had $G = G_{\text{ref}} = C_{\text{in}}(1+s) = 3.5 C_{\text{in}}$

Q. The odd NOT gate had

$$S_2 = \frac{G_2}{G_{\text{path}}} = \frac{76.35}{67.35 \text{ C}_{\text{in}}} = \frac{3.64}{\text{C}_{\text{in}}}$$

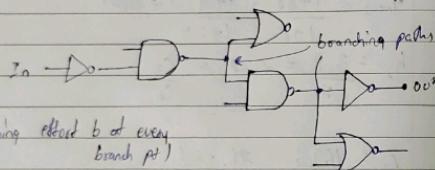
$$S_2 = \frac{169.35}{4.5 \times 3.5 \text{ C}_{\text{in}}} = \frac{10.76}{\text{C}_{\text{in}}}$$

These scaling values are referenced to a value of,

$$\text{C}_{\text{out}} = \frac{20}{35} = 5.71 \text{ fN}$$

$$\text{C}_{\text{out}} = \text{C}_{\text{in}} \times b_1$$

* Branching



$$b = \frac{C_t}{C_{\text{path}}} \quad (\text{branching effect } b \text{ at every branch pt})$$

$C_{\text{path}} = \text{Cap. in main logic path}$

$$G = C_{\text{path}} + C_{\text{off}} \quad (\text{total capacitance seen at every branch node})$$

$\text{C}_{\text{off}} - \text{includes all cap. contrib. that are off the main path}$

$$B = \prod b_i \quad (\text{path branching effect when } b > 1)$$

$$F = G \cdot B \quad (\text{new path effect including branching effect})$$

HW
Q. Problem 8.4 from

(Q. 8.4)
Umera

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At 1st branch pt a NMOS drives another on path NMOS 2 a odd path NOR2 gate, assuming equal gate sizes, the branching effect b_1

$$b_1 = \frac{C_t}{C_{\text{path}}} = \frac{C_{\text{NMOS}} + C_{\text{NOR2}}}{C_{\text{NMOS}}} \\ = \frac{(2+s) + (1+2s)}{(2+s)}$$

The 2nd branch pt is described by

$$b_2 = \frac{C_{\text{NOR2}}}{C_{\text{NOT}}} = \frac{(1+s) + (1+2s)}{(1+s)} = 2 + 3s$$

$$B = b_1 b_2 =$$

Recall $b_1 = \frac{C_t}{C_{\text{path}}} = \frac{C_{\text{NMOS}} + C_{\text{NOR2}}}{C_{\text{NMOS}}} = \frac{(2+s) + (1+2s)}{(2+s)}$