15/11/23

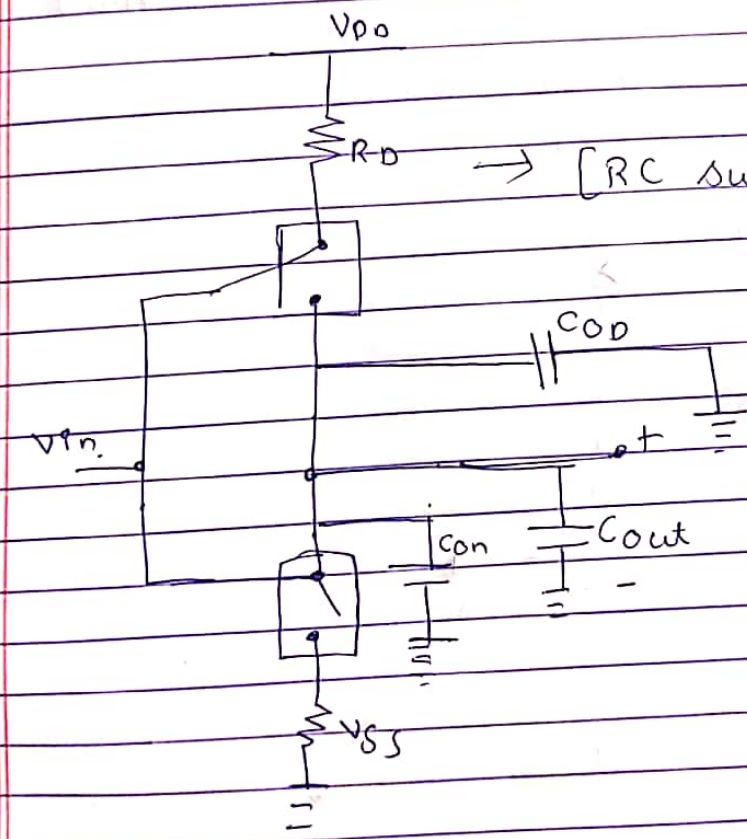
Assignment - 1

1] Estimate the rise & fall time delay of a CMOS inverter through a simple analysis.

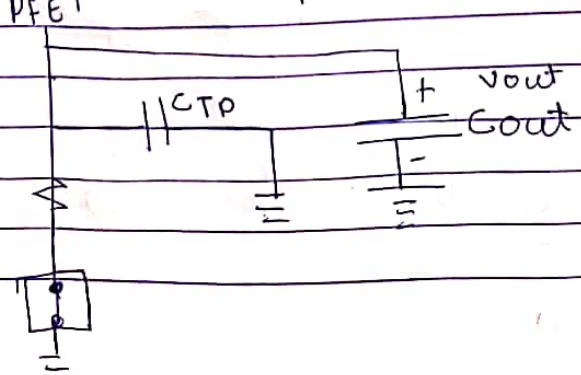
→ **Fall time delay :-**

The input signal Vin changes from 0 to V_{DD} at time $t=0$, the initial condn of o/p is given as $V_{out(0)} = V_{DD}$ when i/p is switched the nfet is acting in linear region & pfet is in cut-off

- In term of switch model nFET is closed & pfet is open as shown in fig below



Since the pfet is ON.



- Capacitor Cout is initially charged to V_{DD} & is allowed to discharge to a nFET resistance R_n leaving the current output of capacitor as

$$I = -C_{out}\frac{dv_{out}}{dt} = \frac{v_o}{R}$$

$$v_{out} = V_{DD}\, e^{-t/\tau_n}$$

where

$$\tau_n = R_n C_{out}$$

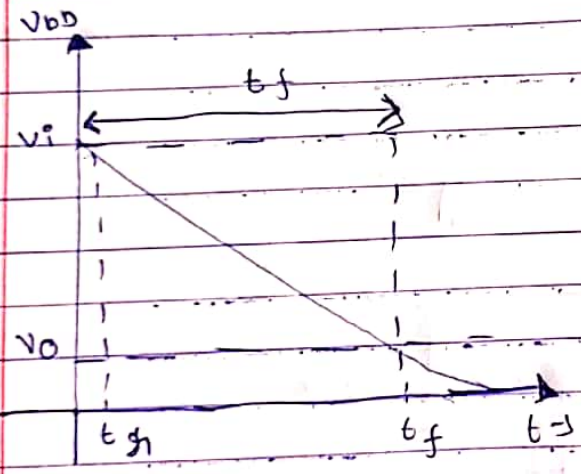
$$t = \tau_n \ln\left(\frac{V_{DD}}{v_{out}}\right)$$

$$t_f = t_y - t_x$$

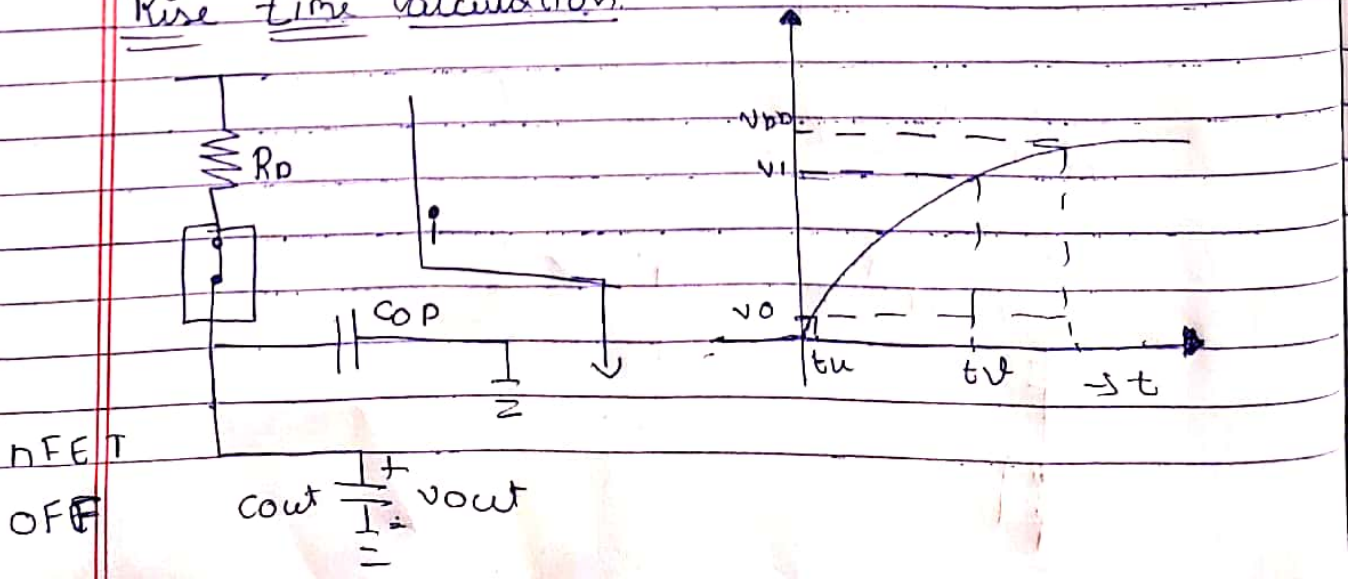
$$= \tau_n \ln\left(\frac{V_{DD}}{0.1V_{DD}}\right) - \tau_n \ln\left(\frac{V_{DD}}{0.9V_{DD}}\right)$$

$$t_f = \tau_n \ln|9| \approx 2.2\tau_n$$

$$t_{HL} = \tau_f$$



Rise time Calculation



E.
tance
as

$V_{out}(0) = ON \quad i = I_{out} = C_{out}\frac{dV_{out}}{dt} = \frac{V_{DD} - V_{out}}{R_p}$

$V_{out}(t) = V_{DD}\left[1 - e^{t/T_p}\right]$

$T_p = R_p C_{out} \qquad t_{pr} = t_v - t_u$

$t_{pr} = t_r(a) T_p = 2.2 T_p$

$t_{LH} = t_{pr}$

- Max freq is given by

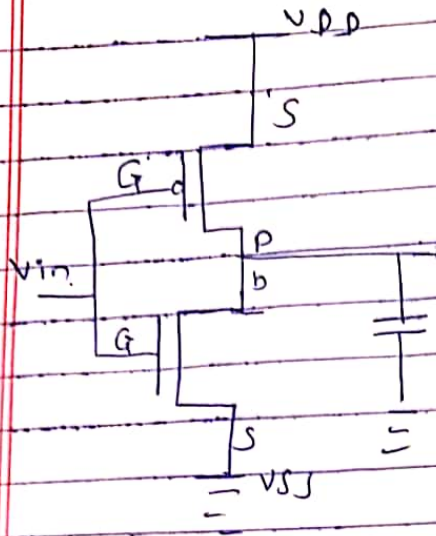
$$f_{max} = \frac{1}{t_{HL} + T_{LH}}$$

$$\boxed{f_{max} = \frac{1}{t_f + t_r}}$$

2. Discuss the power dissipation components of a CMOS inverter.

→

(4) Derive the equation for switching point of CMOS inverter



$\therefore I_{DN} = I_{DP}$

nFET

$V_{Sat} > V_{GSn} - V_{th}$

$V_{Sat} > V_{in} - V_{SS} - V_{th}$

$V_{GS} = V_o - V_{SS}$

$V_{GS} = V_m$

$= V_m$

PFET: $V_{Sat} > V_{GSP} - |V_{tn}|$

$V_{DD} - V_m > V_{DD} - V_m - |V_{tp}|$

Both nMOS & PMOS are in saturation at V_{in}

$\therefore I_{DSn} = I_{DPn}$

$$\frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right) (V_{gs} - V_t)^2 = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{gsp} - |V_{tp}|)^2$$

$$= \frac{\beta_n}{2} (V_{gsn} - V_{tn})^2 = \frac{\beta_p}{2} (V_{SGp} - |V_{tp}|)^2$$

$$= \frac{\beta_n}{2} (V_m - V_{th})^2 = \frac{\beta_p}{2} (V_{DD} - V_m - |V_{tp}|)^2$$

$$\frac{\beta_n}{\beta_p} = \frac{(V_{DD} - V_m - |V_{tp}|)^2}{(V_m - V_{th})^2}$$

$$\sqrt{\frac{\beta_n}{\beta_p}} = \frac{V_{DD} - V_m - |V_{tp}|}{V_m - V_{th}}$$

$$\sqrt{\frac{\beta_n}{\beta_p}} (V_m - V_{th}) = (V_{DD} - V_m - |V_{tp}|)$$

$$\sqrt{\frac{\beta_n}{\beta_p}} (V_m) - \sqrt{\frac{\beta_n}{\beta_p}} (V_{th}) = V_{DD} - V_m - |V_{tp}|$$

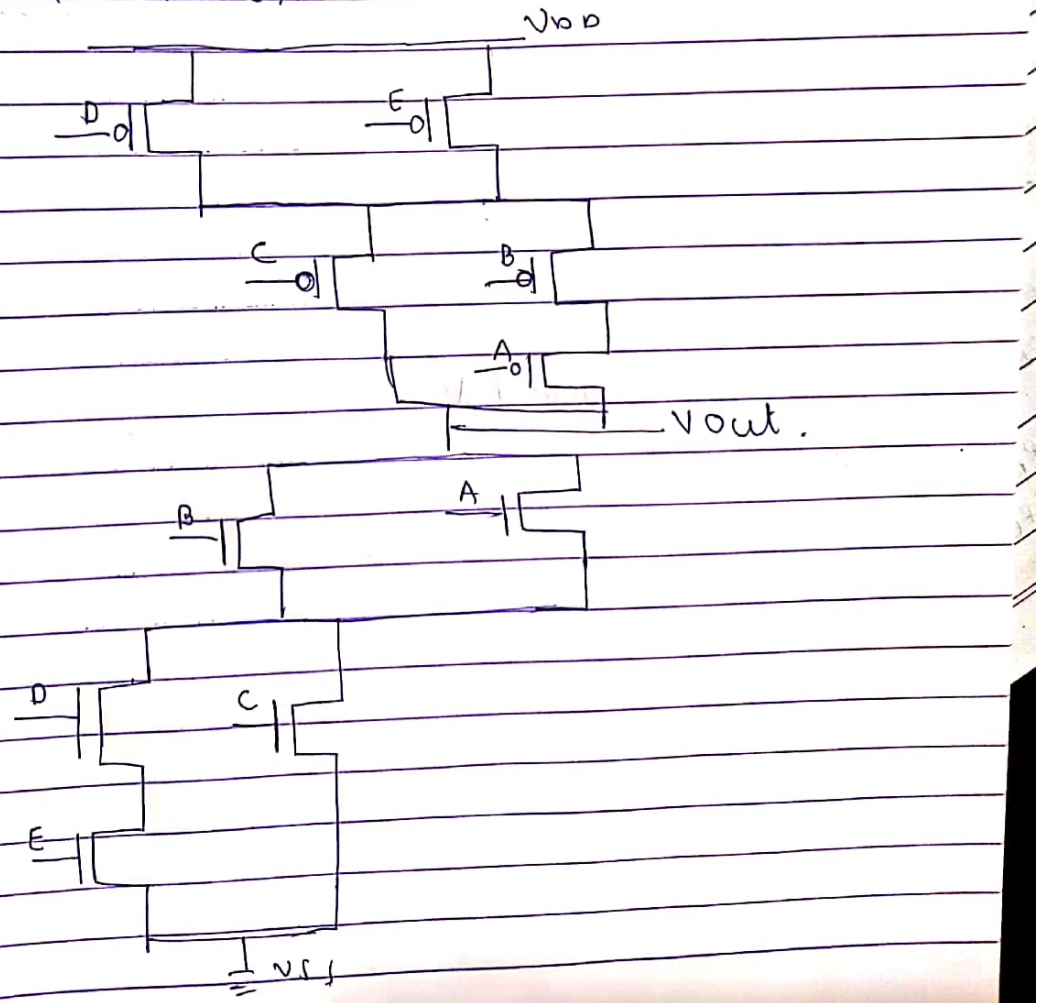
$$\sqrt{\frac{\beta_n}{\beta_p}}\,V_m + V_m = V_{DD} - |V_{tp}| + \sqrt{\frac{\beta_n}{\beta_p}}\,V_{th}$$

$$V_m = \frac{V_{DD} - |V_{tp}| + \sqrt{\frac{\beta_n}{\beta_p}}\,V_{th}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$ → mid point voltage

Symmetrical inverter $= \beta_n = \beta_p = \& \; V_{tn} = |V_{tp}|$.

Hence $V_M = \frac{V_{DD}}{2}$

5. The designer has a goal to achieve same transient performance as that of a reference CMOS inverter. Accordingly, design a combinational circuit using fully CMOS logic for function $F = \{A + B(C + DE)\}'$.



6. Consider a process that has an oxide of $t_{ox} = 9.5nm$. The particle mobility are given by $\mu_n = 540 cm^2/V\text{-}sec$, $\mu_p = 220 cm^2/V\text{-}sec$. An nfet & pfet are made both with $W = 12\mu m$, $L = 0.35\mu m$. Both have gate voltage of $V_g = 3.3\ V$ while threshold voltage $V_{tn} = 0.65\ V$ & $V_{tp} = -0.74\ V$

i) Find R_p & R_n of 2 transistors

ii) Suppose that we keep nFet of same size, but ↑ width of pFET to point where $R_p = 0.8R_n$. Find required width of pFET?

⇒ $\mu_n = 540 cm^2/VS$ $\mu_p = 220 cm^2/V\text{-}sec$ $W = 12\mu m$ $L = 0.35\mu$

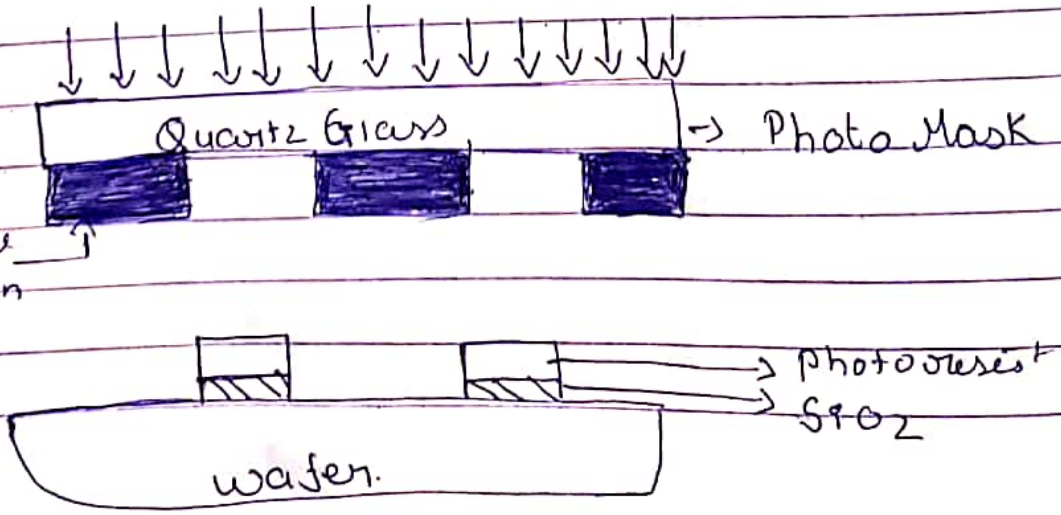
$V_g = 3.3$ $V_{tn} = 0.65V$ $V_{tp} = -0.74V$

i) $R_n = \dfrac{1}{\beta_n (V_{DD} - V_{tn})}$

$R_p = \dfrac{1}{\beta_n (V_{DD} - |V_{tp}|)}$

8 Explain procedural steps in photo lithography for forming diffusion with neat diagram & what is differences b/w +ve & -ve photo resist

→ Lithography is a technique used to transfer a geometric pattern (circuit) from a photo mask to a light sensitive chemical (photoresist) on a substrate



1) In this process 1st a layer of Silicon di-oxide is applied over a wafer or Substrate.

2) Then over the silicon wafer a light sensitive liquid (photoresist) is applied on it. Photo resist of is of 2 types +ve resist & -ve resist.

3) The

3) Then once the photoresist is applied then the excess solvent is removed & the photoresist layer is made hard by prebake process which is done by different technique most common is hotplate technique which where temp is upto 1000 degree

4) After the Prebake process the Masking process takes which is used to print a certain diagram of a circuit on to the photoresist layer. This mask layer is placed on a flat quartz glass to ensure proper impression

5) Once the mask is aligned properly on wafer surface with the help of optical instruments then it is exposed under UV radiation

6) ~~Once~~ After they are exposed to UV rays they are again baked to ensure structure change. Then they are dipped into mild alkaline soln to dissolves the regions of photoresist which was not not exposed to UV rays.

7) Then wafer is treated with etchant which only dissolves exposed wafer surface.

8) Then the photo resist layer is removed.