

## Assignment - 1

- 1) Estimate the rise & fall time delays of a CMOS inverter through a simple analysis

We know that,

$$C_{out} = C_{FET} + C_L$$

$$t_r = 2 \cdot 2 T_p \quad \& \quad t_f = 2 \cdot 2 T_n$$

$$\begin{aligned} T_p &= R_p \cdot C_{out} \\ &= R_p \cdot [C_{FET} + C_L] \end{aligned}$$

$$\begin{aligned} T_n &= R_n \cdot C_{out} \\ &= R_n [C_{FET} + C_L]. \end{aligned}$$

$$\Rightarrow t_r = 2 \cdot 2 R_p C_{FET} + 2 \cdot 2 R_p C_L$$

and

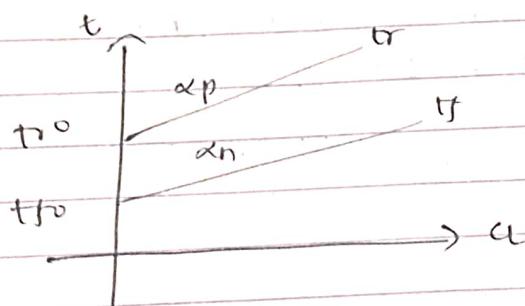
$$t_f = 2 \cdot 2 R_n C_{FET} + 2 \cdot 2 R_n C_L$$

$$\Rightarrow t_{r0} = 2 \cdot 2 R_p C_{FET}$$

$$\& \alpha_p = 2 \cdot 2 R_p$$

$$t_{f0} = 2 \cdot 2 R_n C_{FET}$$

$$\alpha_n = 2 \cdot 2 R_n$$



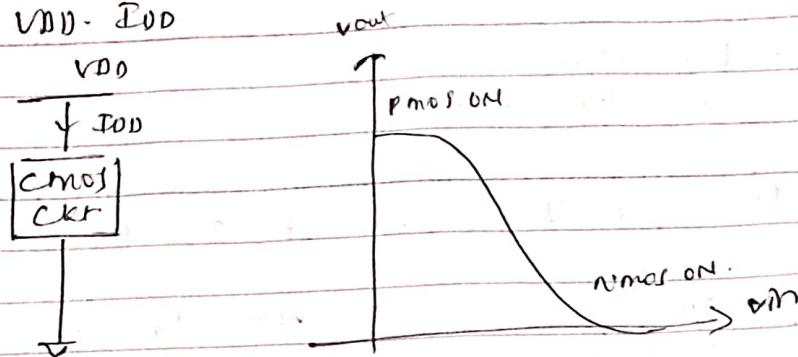
$$\Rightarrow \alpha_p = 2 \cdot 2 R_p = \frac{2 \cdot 2 (1)}{R_p (V_{DD} - V_{tp})}$$

$$\alpha_n = 2 \cdot 2 R_n = \frac{2 \cdot 2 (1)}{R_n (V_{DD} - V_{tn})}$$

- 2) Discuss the power dissipation component of a CMOS inverter.

→ The current and constitutes power given by:

$$P = V_{DD} \cdot I_{DD}$$

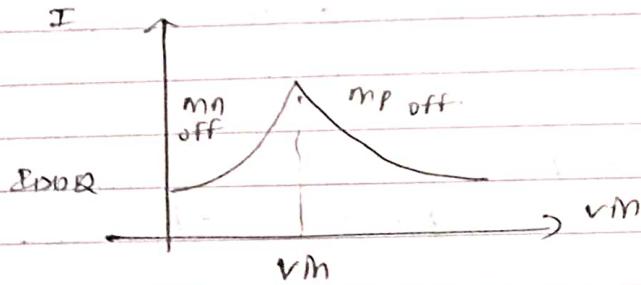


$$\therefore I_{TOTAL} = I_{DC} + I_{DYN}$$

(i) When  $v_{IN} = 0$  or logic 0, nFET is off & there is no direct path from  $V_{DD}$  to GND. ∴ Ideally  $I_{DD} = 0$ . But small amount of current, known as quiescent leakage current flows & hence power is constituted due to this.

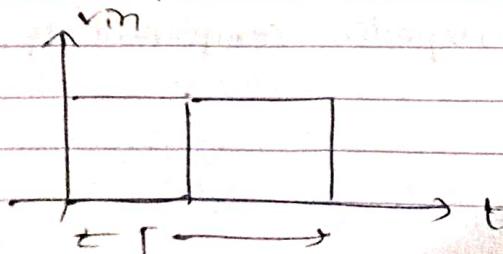
(ii) When  $v_{IN} = \text{switched}$ , current flows upto "peak" & at  $v_{IN} = \text{logic 1}$ , mp turns off & only mn is ON.  
→ Again no direct path between  $V_{DD}$  to GND

$$\therefore P_{DC} = I_{DDQ} \cdot V_{DD}$$



For dynamic power dissipation:

— We use square wave inputs with  $f = \frac{1}{T}$



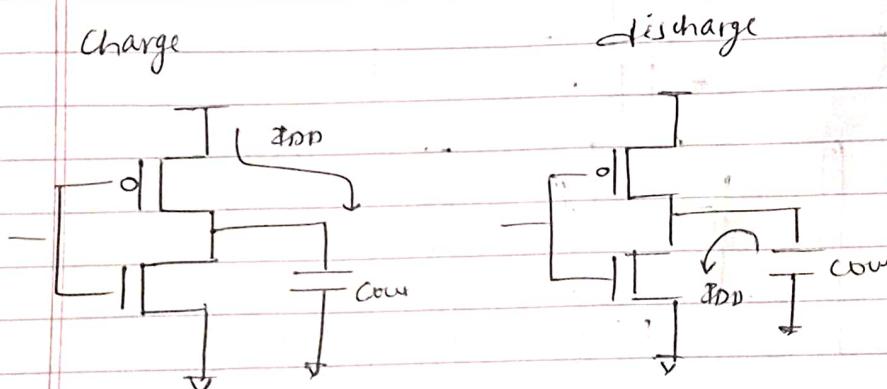
- During 1st half cycle,  $V_m = 0 \rightarrow$  The pFET is only ON & nFET is OFF.  $\therefore$  the current through pFET charges capacitor to  $V_{out} = V_{DD}$
- During 2nd half cycle,  $V_m = \text{high}$ ,  $\therefore$  the nFET turns ON. This causes discharge events.

$$\Delta e = C_{out} \times V_{DD}$$

$$P_{SCW} = C_{out} V_{DD}^2 \cdot f$$

$\hookrightarrow$  Total power dissipation:

$$\begin{aligned} P_{TOTAL} &= P_{DC} + P_{DYN} \\ &= V_{DD} \cdot I_{DDA} + C_{out} \cdot V_{DD}^2 \cdot f \end{aligned}$$



- 3) Explain (Z method of growing Si ingots with a neat figure



- \* (Z) method is used to obtain single crystal Si ingots
- \* It is most widely used method for production of Si ingots in semiconductor industry.
- \* It is also known as pulling technique.

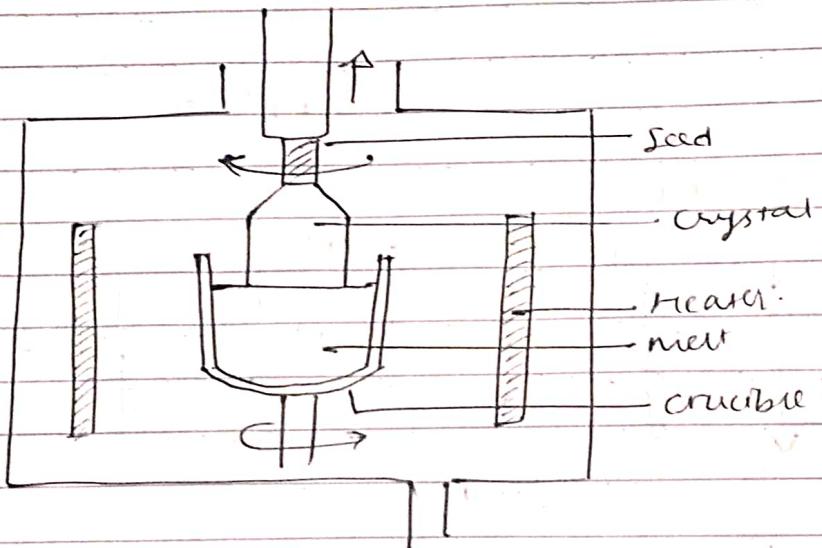
Procedure :

- A piece of seed crystal is attached to a rod & lowered into molten Si.

- The crystal seed is slowly pulled upwards & rotated while temperature being controlled.
- As crystal seed is pulled upwards it solidifies & it forms to crystal ingot.
- The pulling process is continued until the desired ingot diameter is reached.

Factors:

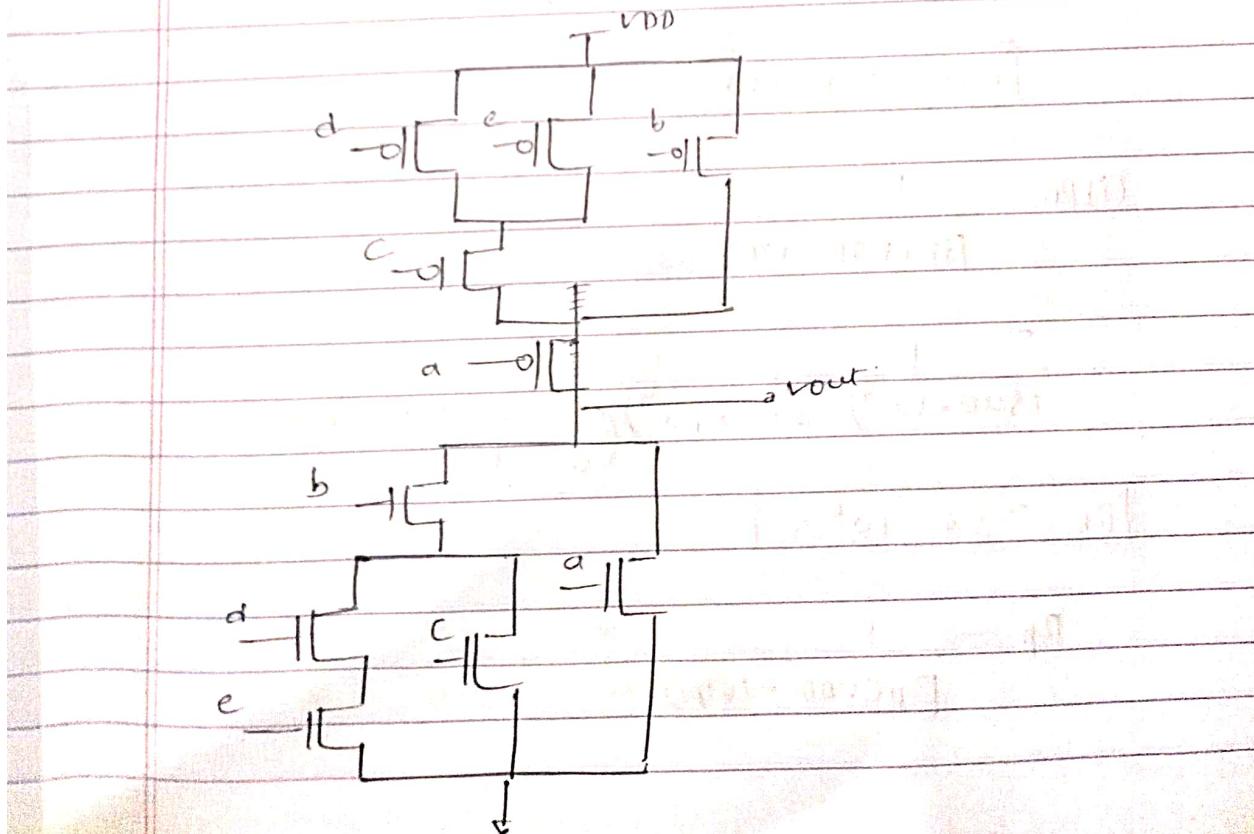
- Temperature - To ensure uniform crystal growth.
- Pulling rate - to avoid formation of dislocations.
- Doping - To control Electrical conductivity.



Q) Derive the equation for switching pt. of CMOS inverter.

→

- 5) The designer has a goal to achieve same transient performance as that of the reference CMOS inverter. Accordingly, design a combinational circuit using fully CMOS logic for the function  $F = \overline{(A+B(C+DE))}$ .



6) Consider a process that has an oxide thickness of  $t_{ox} = 9.5 \text{ nm}$ . The carrier mobilities are given by  $\mu_n = 540 \text{ cm}^2/\text{Vs}$ ,  $\mu_p = 220 \text{ cm}^2/\text{Vs}$ . An nFET & pFET are both with  $w = 12 \mu\text{m}$ ,  $L = 0.35 \mu\text{m}$ . Both have voltages of  $V_g = 3.3 \text{ V}$ . Since the threshold voltages are  $V_{th} = 0.65 \text{ V}$  &  $V_{tp} = -0.7 \text{ V}$ .

- a) Find the voltage values of  $R_p$  &  $R_n$  for the 2 transistors.  
 b) Suppose that we want to keep nFET of same size, but increase width of pFET to the point where  $R_p = 0.8 R_n$ . Find the required width of the pFET.

$$\rightarrow t_{ox} = 9.5 \text{ nm}$$

$$\mu_n = 540 \times 10^{-4}$$

$$\mu_p = 220 \times 10^{-4}$$

$$w = 12 \mu\text{m}$$

$$L = 0.35 \mu\text{m}$$

$$V_g = 3.3 \text{ V}$$

$$V_{th} = 0.65 \text{ V}$$

$$V_{tp} = 0.7 \text{ V}$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{8.854 \times 10^{-12} \times 3.9}{9.5 \times 10^{-3}}$$

$$\boxed{C_{ox} = 3.63 \times 10^{-9}}$$

$$(i) R_n = \frac{1}{B_n(V_{DD} - V_{th})}$$

$$= \frac{1}{(540 \times 10^{-4})(3.63 \times 10^{-9}) \left(\frac{12}{0.35}\right) (3.3 - 0.65)}$$

$$\boxed{R_n = 56 \times 10^6 \Omega}$$

$$R_p = \frac{1}{B_p(V_{DD} - V_{tp})} =$$

$$\frac{1}{(220 \times 10^{-4})(3.63 \times 10^{-9}) \left(\frac{12}{0.35}\right) (3.3 - 0.74)}$$

$$I_{Pp} = 142 \times 10^6 n$$

$$(IV) P_p = 0.8 P_n$$

$$\frac{1}{\mu_n C_o x w L (V_{DD} - V_{Tp})} = 0.8 \times 1 \times 56 \times 10^6$$

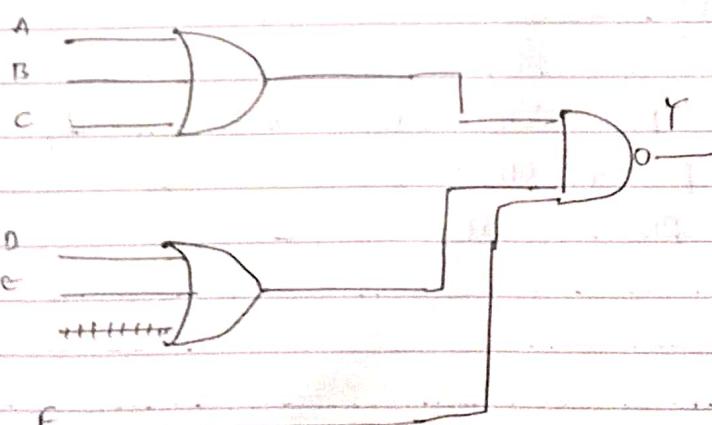
$$\Rightarrow w = 0.35 \times 10^{-6}$$

$$220 \times 10^{-4} \times 3.63 \times 10^{-9} \times (0.8 \times 56 \times 10^6) (3.3 - 0.74)$$

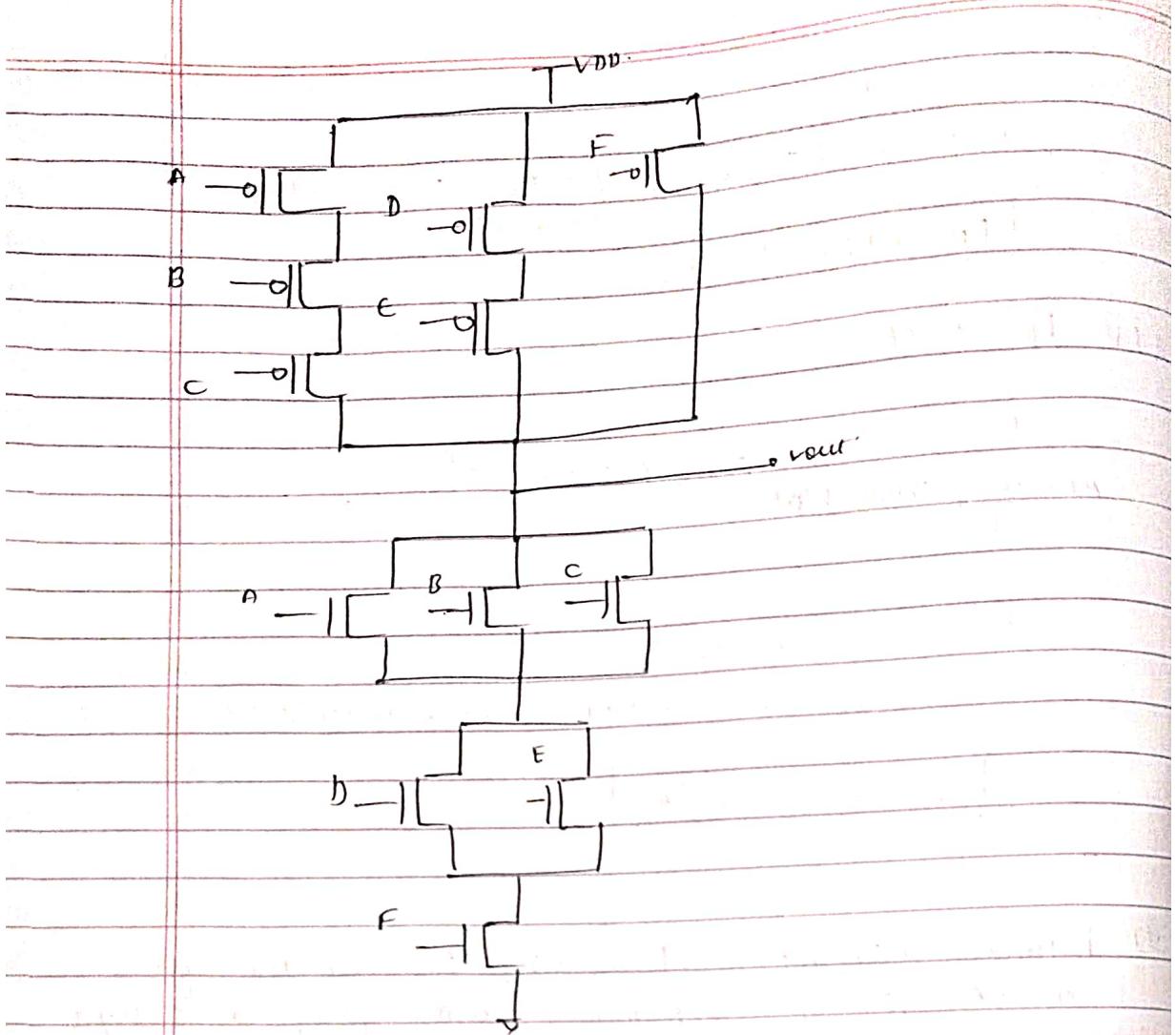
$$w = 38.2 \times 10^{-6} m$$

7) Estimate charging & discharging time constants for an OAI-321 gate implemented using fully CMOS logic.

OAI-321.



$$Y = \overline{(A+B+C) \cdot (D+E) \cdot F}$$



Q) Explain the procedural steps in photo lithography for forming diffusion with neat diagram. What is the difference between 'tire & one' photore sist.

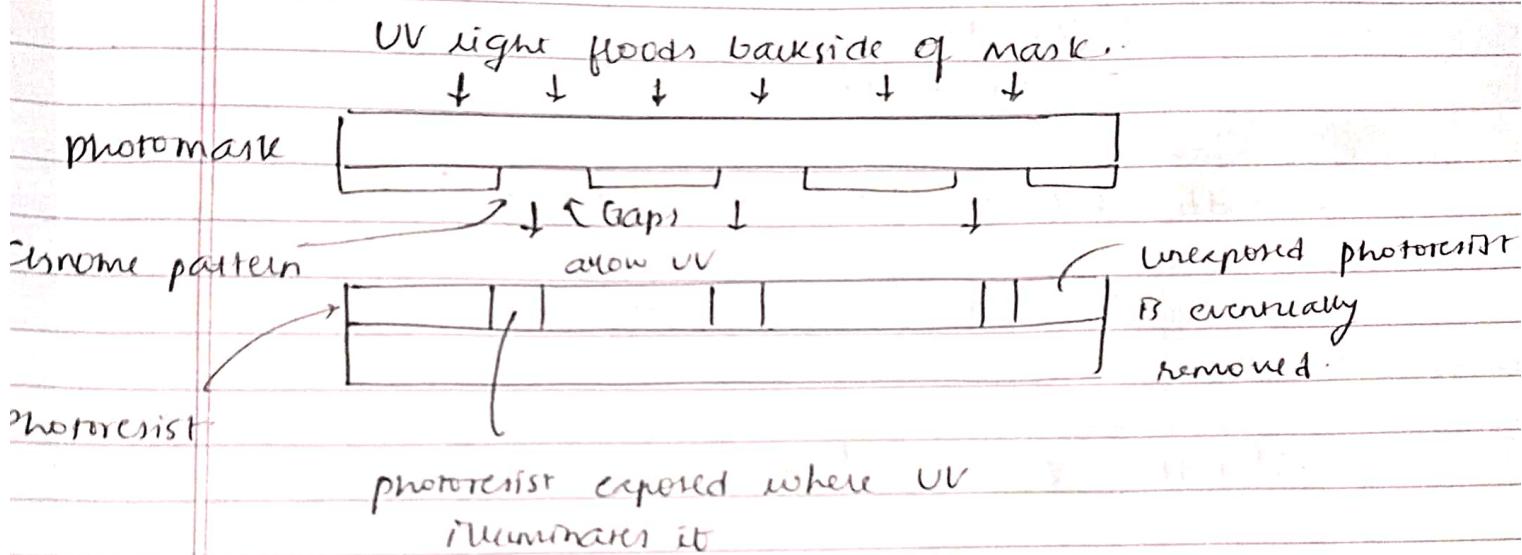
→ Photolithography:

- It is crucial step in semiconductor manufacturing.
- Used to define patterns on wafer surface for subsequent processing steps.

\* Steps:

- The semiconductor wafer is coated with thin layer of photoresist, a light sensitive material.
- The coated wafer undergoes pre-exposure to partially cure the photoresist.

- A photomask containing desired pattern is aligned on the top of the wafer.
- The wafer is exposed to UV light.
- The wafer is then immersed in the developer solution.
- If photoresist is positive, exposed regions are removed.
- If photoresist is negative, unexposed regions are removed.
- The wafer is then rinsed & dried.



Q) Calculate the diffusion parasitic  $C_{dd}$  of the unit sized contact NMOS transistor in a 130 nm process, when the drain is at 0V & 1.8V. Assume that the substrate is grounded. The transistor characteristics are  $C_J = 0.98 \text{ fF}/\mu\text{m}^2$ ,  $M_J = 0.36$ ,  $C_{JSW} = 0.22 \text{ fF}/\mu\text{m}$ ,  $M_{JSW} = 0.1$ ,  $\varphi_D = 0.78 \text{ V}$  at room temperature. Area ( $5d \times 4d$ ).

$$A = 130 \text{ nm}$$

$$V_{DD} = 1.8 \text{ V}$$

$$\Rightarrow \text{Area} = 5d \times 4d$$

$$= 20d^2$$

$$= 20(130 \times 10^{-9})^2$$

$$= 3.36 \times 10^{-13} \text{ m}^2$$

Now we have,

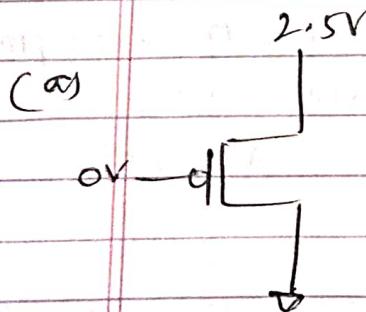
$$C_{db} = (\text{Area} \times C_J \times \left(1 + \frac{V_J}{P_B}\right)^{-M_J}) + \\ (\text{periphery} \times C_{JSW} \times \left(1 + \frac{V_J}{P_B}\right)^{-M_{JSW}})$$

$$\begin{aligned}\text{periphery} &= 2(a+b) \\ &= 2(5a+4d) \\ &> 2(9d) \\ &= 2.34 \times 10^{-6} \text{ m.}\end{aligned}$$

$$\therefore C_{db} = 3.38 \times 10^{-13} \times 0.98 \times \left(1 + \frac{1.8}{0.75}\right)^{-0.36} + \\ 2.34 \times 10^{-6} \times 0.22 \times \left(1 + \frac{1.8}{0.75}\right)^{-0.1}$$

$$\therefore \boxed{C_{db} = 8.96 \times 10^{-7} \text{ fF}}$$

- ii) Determine the bias states of the pMOS transistors, where  $V_{tp} = -0.4V$ . The gate terminal has its most (-)ve voltage wrt source terminal.

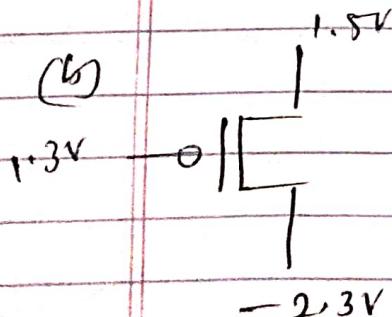


$$V_{GSS} = -2.5V$$

$$V_{DS} = -2.5V$$

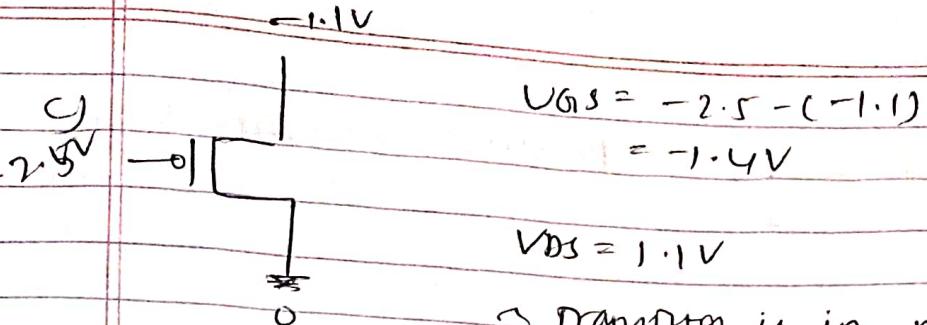
$$\therefore V_{DS} > V_{D1} + V_{tp}$$

∴ Transistor is in saturation region.



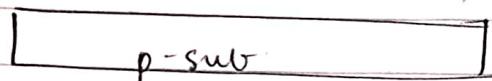
The gate voltage is not sufficiently more (-)ve than either drain or source.

∴ Transistor is in off-state.



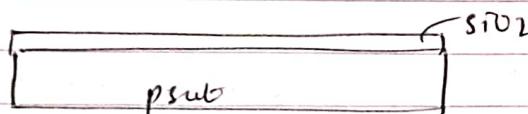
- 12) Depict the different process steps involved in the fabrication of a CMOS inverter in n-well process with neat diagrams.

1) substrate



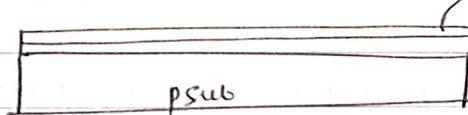
Primarily start with p-sub

2)



Oxidation performed at  $1000^{\circ}\text{C}$

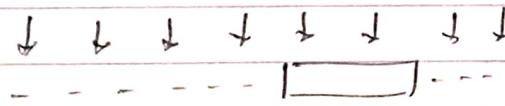
3)



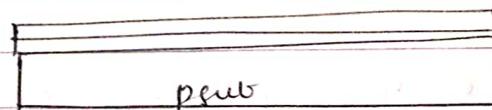
photoresist

A light sensitive material  
photoresist is deposited on  $\text{SiO}_2$

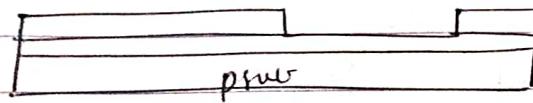
4)



Photoresist exposed to UV rays

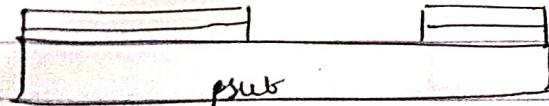


5)



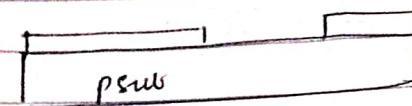
A pair of photoresist is removed with acidic solution

6)



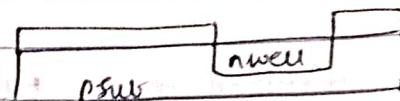
$\text{SiO}_2$  is also removed using etching.

7)

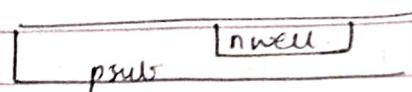


photoresist is stripped off

8)

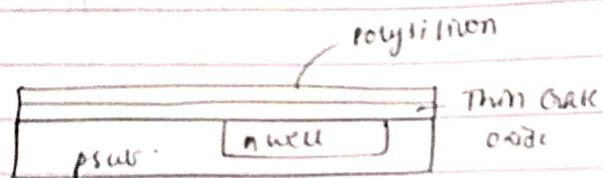


9)



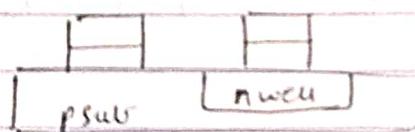
Gate formation:-

10)



16

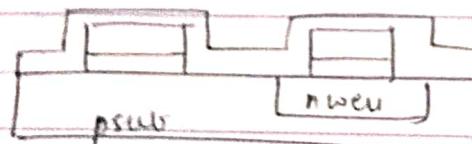
11)



Except 2 gates regions remaining  
layer is stripped off.

17)

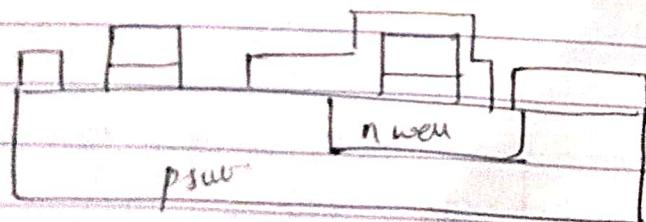
12)



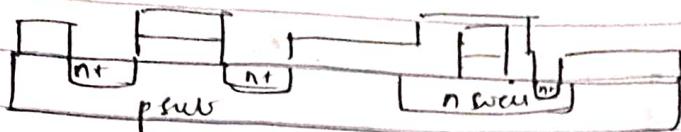
Oxidation process is done.

13)

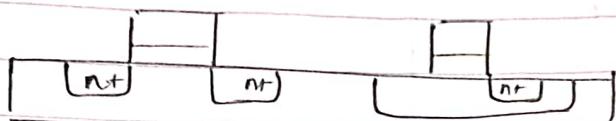
Masking done for n-diffusion:



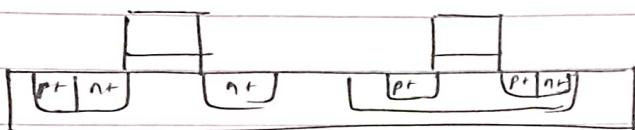
nt dopants are diffused or ion implanted



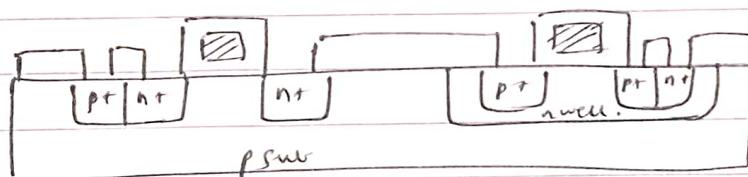
14) Oxide stripping off.



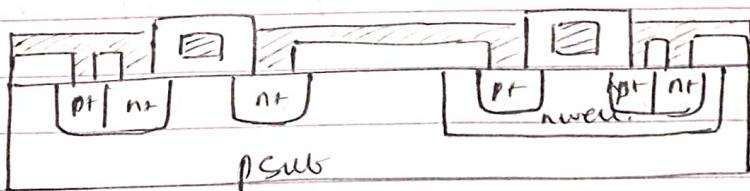
15) p diffusion done to form terminators of pmos.



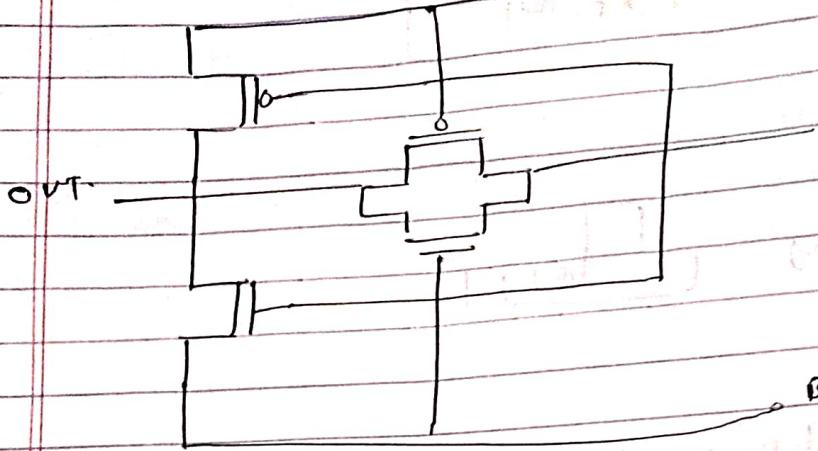
16) Thick field oxide formed except pmos & nmos terminals.



17) Metallization is done.



13) Identify the functionality of the circuit shown below.



14) An inverter uses FET's with  $\beta_n = 2.1 \text{ mA/V}^2$  &  $\beta_p = 1.8 \text{ mA/V}^2$ . The threshold voltages are given as  $V_{TH} = 0.6 \text{ V}$  &  $V_{TP} = -0.7 \text{ V}$  & power supply has a value of  $V_{DD} = 5 \text{ V}$ . The parasitic FET capacitance at the output node is estimated to be  $C_{FET} = 74 \text{ fF}$ .

a) Find  $V_m$ .

b) Find  $R_n$  &  $R_p$ .

c) calculate  $t_r$  &  ~~$t_f$~~   $t_f$ .

d) Plot  $t_r$  &  $t_f$  as a function of  $C_L$ .

$$\rightarrow \text{Eqn } \beta_n = 2.1 \text{ mA/V}^2$$

$$\beta_p = 1.8 \text{ mA/V}^2$$

$$V_{TH} = 0.6V$$

$$V_{TP} = 1 - 0.3V = 0.7V$$

$$V_{DD} = 5V$$

$$CFET = 74 fF$$

(a)  $r_m = \frac{V_{DD} - V_{TP} + V_{TH}(\sqrt{\beta_n/\beta_p})}{1 + \sqrt{\beta_n/\beta_p}}$

$$\Rightarrow r_m = \frac{5 - 0.7 + 0.6 \sqrt{\frac{1.2}{1.8}}}{1 + \sqrt{\frac{1.2}{1.8}}}$$

$$\boxed{r_m = 2.373V}$$

(b)  $R_n = \frac{1}{\beta_n(V_{DD} - 3V_{TH})} = \frac{1}{2.1 \times 10^{-3}(5 - 0.6)}$

$$\boxed{R_n = 108.225 \Omega}$$

$$R_p = \frac{1}{\beta_p(V_{DD} - (V_{TP}))} = \frac{1}{(1.8 \times 10^{-3})(5 - 0.7)}$$

$$\boxed{R_p = 129.2 \Omega}$$

(c)  $t_r = 2.2 R_p (CFET + CL)$   
 $t_r = 17.619 \times 10^{-9} s$

$$\left. \begin{aligned} t_f &= 2.2 R_p (CFET + CL) \\ t_f &= 2.103 \times 10^{-8} s \end{aligned} \right\} CL = 0$$

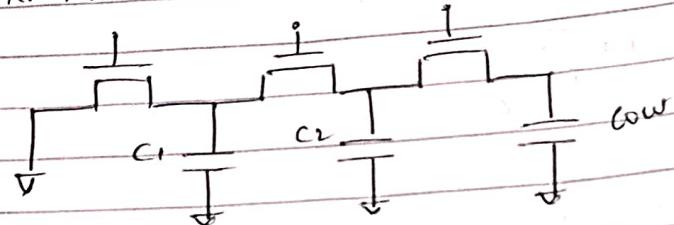
$$t_r = 2.2 R_p C_{out}$$

$$= 2.2 \times R_p \times C_{out} = 44.9 \times 10^{-9} s \quad \left. \begin{aligned} CL &= 115 fF \end{aligned} \right\}$$

$$t_f = 2.2 R_n \cdot C_{out}$$

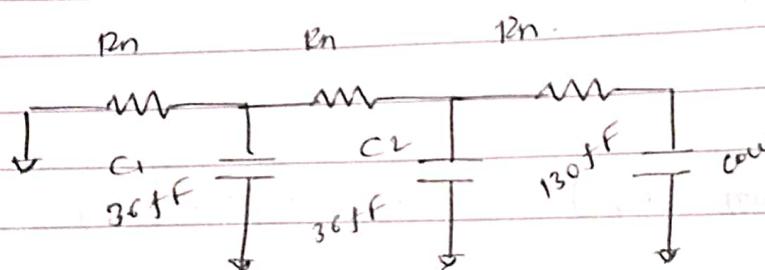
$$= 53.72136 \times 10^{-9} s$$

- (S) A circuit designer has a choice to implement combinational logic using NAND or a NOR n/w. Timing the selector if performance is the criteria, & analyze the speed of a 1 to 0 transition as shown below. The o/p capacitance has a value of  $C_{out} = 130 \text{ fF}$ , while the internal values are  $C_1 = C_2 = 36 \text{ fF}$ . The transistors are identical with  $\beta_n = 2.0 \text{ mA/V}^2$  in a process where  $V_{DD} = 3.3 \text{ V}$  &  $V_m = 0.7 \text{ V}$ .
- (a) Find the discharge time constant for  $C_{out} = 130 \text{ fF}$  using ladder n/w.
- (b) Find time constant



→

$$\begin{cases} \beta_n = 2.0 \text{ mA/V}^2 \\ V_{DD} = 3.3 \text{ V} \\ V_m = 0.7 \text{ V} \end{cases}$$



$$(i) T_n = Rn \cdot Cout$$

$$Rn = \frac{1}{\beta_n (V_{DD} - V_m)}$$

$$[ Rn = 192.30 \Omega ]$$

$$T_n = Rn \cdot C_1 + 2RnC_2 + 3RnC_{out}$$

$$[ T_n = 95.7 \times 10^{-9} \text{ s} ]$$

$$(ii) T_n = (Rn + Rn + Rn) \cdot CFET$$

$$= 3Rn \times CFET = 74.99 \times 10^{-9} \text{ s.}$$

$$\text{error \%} = \frac{95.3 \times 10^{-9} - 84.99 \times 10^{-9}}{95.3 \times 10^{-9}} \\ = 21.63\%$$