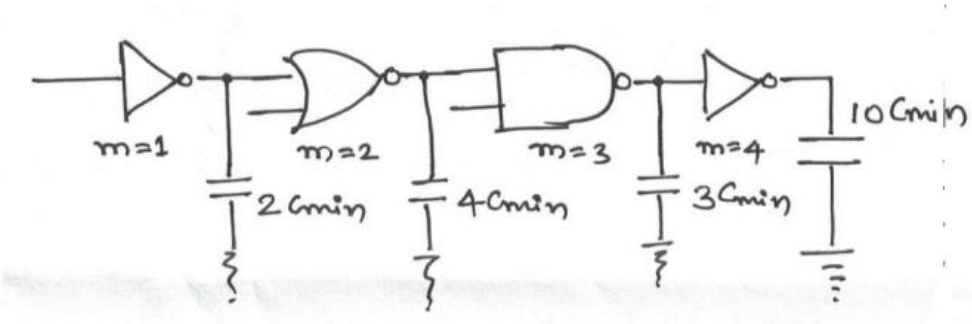
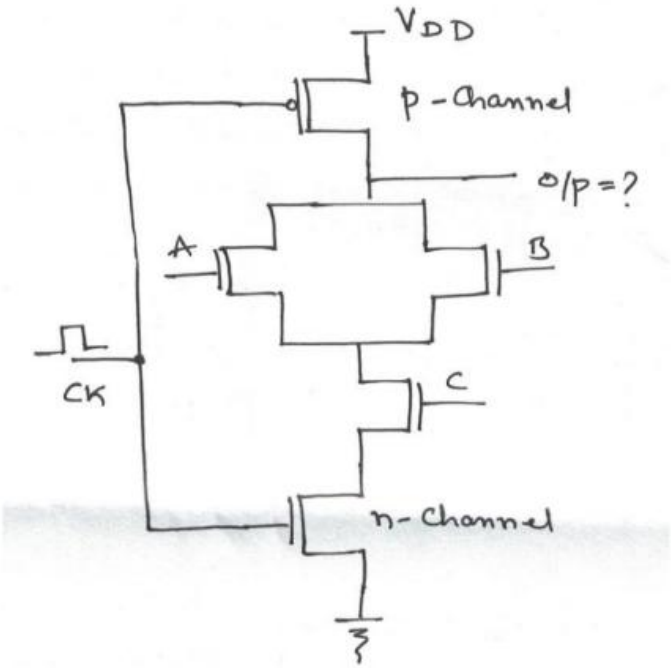
CMOS VLSI Circuits

Assignment 02

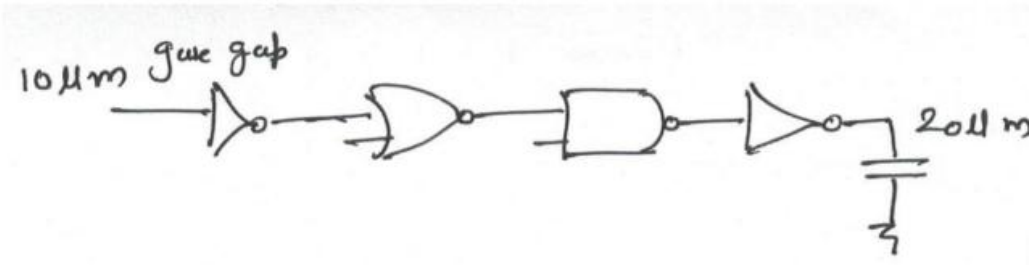
1. Discuss the phenomenon of latch-up? Explain ways of dealing with latch-up in CMOS VLSI design.
2. Odering the poly gates of a CMOS gate expressed by Y = ((D+E+A) * (BC))' using suitable optimizing technique and represent its equivalent stick diagram.
3. For the AOI – 22, implement the logic using CVSL equivalent.
4. Consider the logic chain of Co-processor shown below. The input at A is switched from 0 to 1. Find the expression for the delay through the chain using an appropriate procedure. Also chose appropriate inputs at other gates to ensure switching across the entire chain.



5. In the figure, the boolean expression for the output in terms of A,B,C, when the clock CK is high, find the function and also implement the clocked CMOS equivalent of the same.



6. Implement an AOI-221 gate using C^2MOS logic, Explain its working.
7. Consider the logic cascade shown in figure below. Use logical effort to find the capacitor and path electrical effort at each stage in the chain. Assume symmetric gate with r = 2.5.



8. Why is pseudo nMOS called ratioed logic and CMOS logic called ratioless logic? Analyze with appropriate equation and graph.
9. Illustrate
    a. the CVSL working with example.
    b. Complementary Pass Logic(CPL).
10. Consider a CMOS process with VDD = 5V, Vtn = 0.7V, Vtp = -0.8V, Kn' = 150 μA/ V2 , Kp' = 68 μA/ V2 Calculate VOH and VOL for a pseudo nMOS with (W/L)p= 4 and (W/L)n = 6. What would you do to improve the design?
11. Sketch a stick diagram for a CMOS gate computing Y=(A+B+C) D)' and estimate the cell width and height using lambda based design rules.
12. Justify the design of inverter chain to drive a large input capacitance gate with appropriate equations.
13. Consider the dual expressions g=(xy+zw) and G=(x+ y) (z+w) . Which form (AOI or OAI) would provide the best performance when built using pseudo- nMOS design?
14. Analyze the shortcomings of Dynamic CMOS logic. Illustrate for an example with appropriate waveforms how Domino logic can overcome them.
15. The following circuit has input A and B and output Z. Write the function implemented by the circuit, draw the schematic.