KLE Technological University | Creating Value, Leveraging Knowledge

Dr. M. S. Sheshgiri Campus, Belagavi

Department of Electronics & Communication Engineering

Architectural Design of Integrated Circuits

23EECE302

OPEN ENDED REPORT

"Design of a 5-Stage Pipelined MIPS32 RISC Processor on Verilog"

Submitted by:

Mr. Pratik P Patil

SRN:02FE21BEC063

Sem VI , Div A

KLE TU, Dr. M S Sheshgiri Campus, Belagavi.

Mentored by:

Dr. Kunjan D. Shinde

Assistant Professor, Dept. of E&CE,

KLE Technological University, Dr. M S Sheshgiri Campus, Belagavi.

Academic Year 2023-24

Contents

Problem Statement:

The goal of this project is to design, implement, and analyze a pipelined Reduced Instruction Set Computing (RISC) processor using Verilog. The processor should efficiently handle basic arithmetic, logic operations, memory access, and branch instructions in a pipelined manner to improve instruction throughput and overall performance.

Introduction :

A pipelined processor architecture divides the processing of instructions into separate stages, each handled by a different part of the processor. This approach allows multiple instructions to be processed simultaneously, significantly increasing the throughput of the system. The RISC architecture is known for its simplicity and efficiency, making it an ideal candidate for pipelined execution. This project implements a pipelined RISC processor with stages for instruction fetch, decode, execution, memory access, and write-back.

Objectives and methodology :

1. Design a pipelined RISC processor with five stages: Instruction Fetch (IF), Instruction Decode (ID), Execute (EX), Memory Access (MEM), and Write-Back (WB).
2. Implement the processor in Verilog.
3. Simulate and verify the functionality of the processor.
4. Analyse the performance and efficiency of the pipelined architecture

Methodology

1. Design the Processor: Define the architecture and Datapath for the pipelined processor.
2. Implement in Verilog: Write Verilog code to implement the designed processor.
3. Simulation: Use testbenches to simulate the processor and verify its functionality.
4. Analysis: Evaluate the performance of the pipelined processor through simulation results and comparative analysis with non-pipelined counterparts.

Design and Architectures

The processor is designed with the following stages:

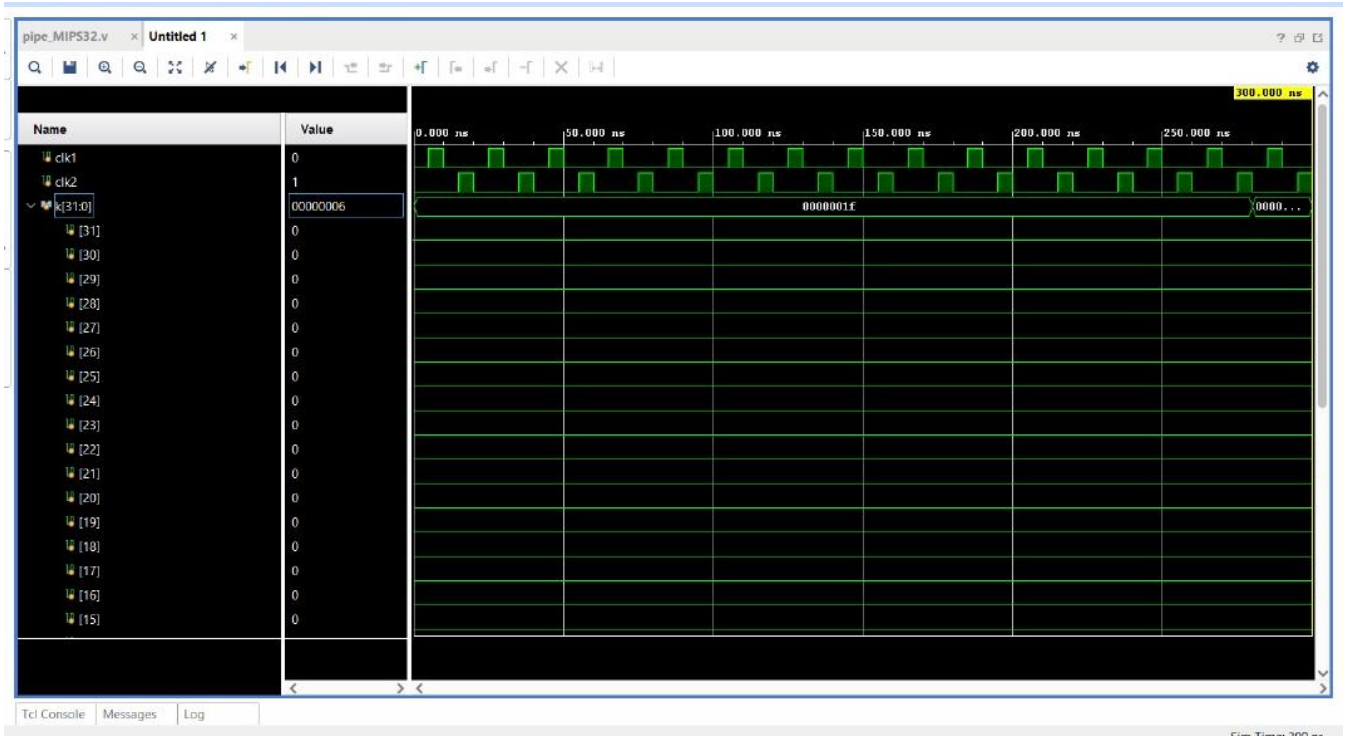
1. **Instruction Fetch (IF)**: Fetches the instruction from memory.
2. **Instruction Decode (ID)**: Decodes the instruction and reads the operands from the register file.
3. **Execute (EX)**: Performs arithmetic, logical, or branch operations.
4. **Memory Access (MEM)**: Reads from or writes to the data memory.
5. **Write-Back (WB)**: Writes the result back to the register file

Datapath and Control Signals

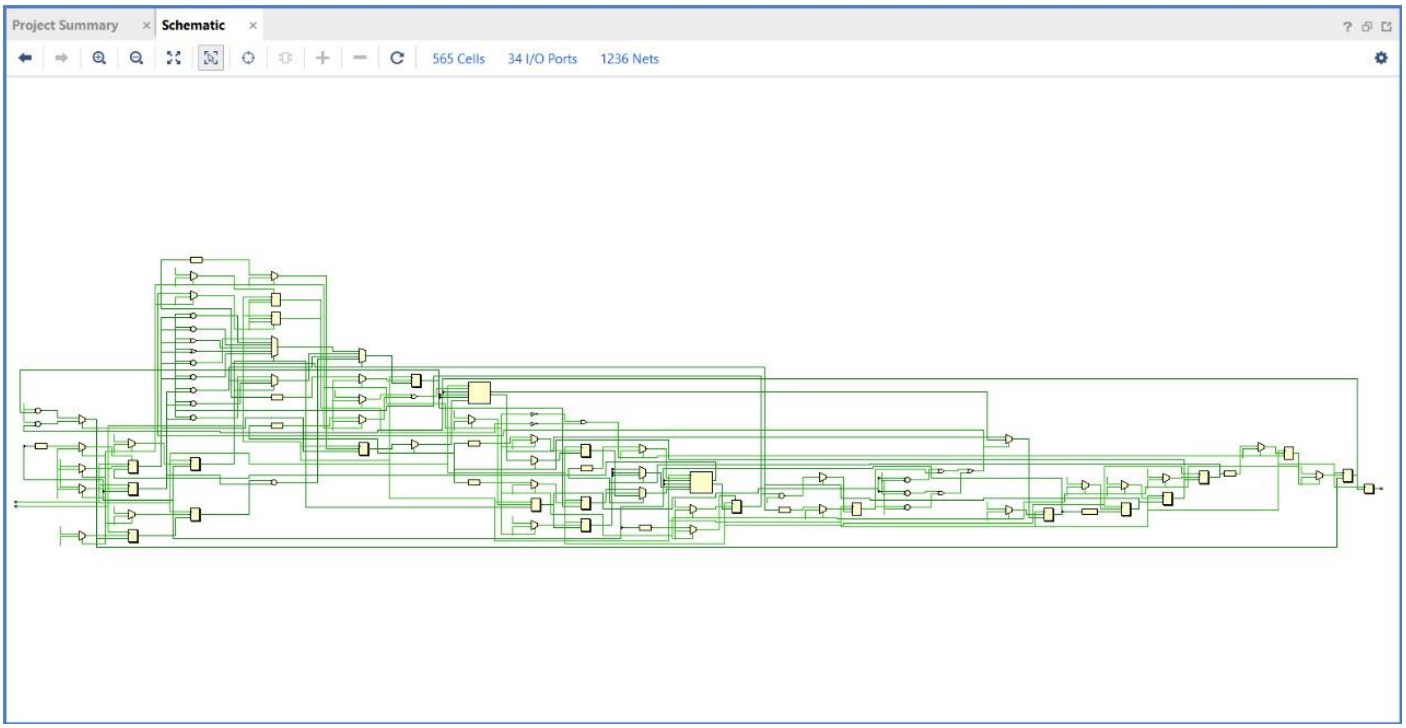
1. The processor uses a set of control signals to manage data flow through the pipeline stages.
2. Registers are used to store intermediate results between stages.
3. A hazard detection and forwarding unit manages data hazards to ensure correct execution of instructions.

Results:

a. Simulation



b. implementation



Advantages and Applications :

Advantages

1. Increased Throughput: The pipelined architecture allows multiple instructions to be processed concurrently, significantly increasing the overall throughput.
2. Efficiency: The simple and efficient design of RISC makes it suitable for a pipelined implementation.
3. Scalability: The modular design allows easy scalability and extension of the processor capabilities

Applications

1. **Systems**: Suitable for use in embedded systems where efficiency and performance are critical.
2. **Educational Tools**: Useful for teaching concepts of computer architecture and pipelining.
3. **Custom Computing Solutions**: Can be used in custom computing applications requiring specialized instruction sets and performance optimization.

Conclusion :

The implementation of a pipelined RISC processor in Verilog demonstrates the benefits of pipelining in enhancing instruction throughput and overall processor performance. Through simulation, the processor's functionality and efficiency are validated, showcasing its potential applications in various fields.

References:

- NPTEL & IIT KGP 'Hardware Modeling using Verilog'- Prof. Indranil Sengupta
- https://github.com/arpit306/5-Stage-Pipelined-MIPS32-RISC-Processor-Design-on-Verilog?tab=readme-ov-file