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Dr. M. S. Sheshgiri Campus, Belagavi

Department of Electronics and Communication Engineering

Minor Project II Report

on

Design and optimization of high performance SRAM

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

CERTIFICATE

This is to certify that project entitled **"Design and optimization of high performance SRAM"** is a bonafide work carried out by the student team of **"Aleena Mulla (02fe21bec006), Basavesh Patil (02fe21bec018), Harsh A Patil (02fe21bec035), Pratik Pati(02fe21bec063)"**. The project report has been approved as it satisfies the requirements with respect to the minor project II work prescribed by the university curriculum for B.E. (VI Semester) in Department of Electronics and Communication Engineering of KLE Technological University Dr. M. S. Sheshgiri CET Belagavi campus for the academicyear 2023-2024.

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-The project team

ABSTRACT

This report delves into the design and optimization of an 8T SRAM (Static Random-Access Memory) cell, focusing on enhancing stability and noise margin through skewness modification. SRAM cells are pivotal in modern digital systems due to their speed and density, but optimizing their stability is critical for reliable performance. The study begins with an overview of conventional SRAM architectures and the importance of high stability and noise margins in contemporary digital systems. The proposed 8T SRAM cell is designed with a focus on skewness adjustment to maximize stability and improve the Static Noise Margin (SNM). The research investigates the impact of skewness on various performance metrics, including read stability, write ability, and overall noise tolerance. Simulation results are presented to highlight the effectiveness of skewness modification in enhancing SNM and maintaining robust performance under various operational conditions.

Contents

1 Introduction **9**
- 1.1 Motivation . . . 9
- 1.2 Objectives . . . 9
- 1.3 Literature survey . . . 9
- 1.4 Problem statement . . . 10
- 1.5 Application in Societal Context . . . 10
- 1.6 Project Planning . . . 11
- 1.7 Organization of the report . . . 11

2 System design **12**
- 2.1 Functional block diagram . . . 12
- 2.2 Final design . . . 13

3 Implementation details **14**
- 3.1 Specifications and final system architecture . . . 14
- 3.2 Algorithm . . . 15
- 3.3 Flowchart . . . 16

4 Optimization **17**
- 4.1 Introduction to optimization . . . 17
- 4.2 Types of Optimization . . . 17
- 4.3 Selection and justification of optimization method . . . 18

5 Results and discussions **19**
- 5.1 Result Analysis . . . 19
- 5.2 Discussion on optimization . . . 20

6 Conclusions and future scope **21**
- 6.1 Conclusion . . . 21
- 6.2 Future scope . . . 21

References **21**

List of Tables

3.1 Specifications for 8T SRAM using CMOS 45nm Technology 14

5.1 Analysis Results 19

List of Figures

2.1 Block Diagram 13

3.1 Design of 8T SRAM. 14
3.2 Flowchart. 16

5.1 Transient analysis 20
5.2 Butterly curve 20

Chapter 1

Introduction

1.1 Motivation

Our team embarked on this project driven by a shared passion for Very Large Scale Integration (VLSI) and electronic design. We concentrated on the critical component of memory arrays, the 8T SRAM (Static Random-Access Memory) cell, aiming to optimize stability and noise margin in contemporary electronic systems. Understanding that improving SRAM reliability is essential for modern digital applications, we sought to demonstrate the powerful combination of our common interests in integrated circuit design. By working together to explore skewness modifications within the 8T SRAM structure, we aimed to advance VLSI technology and enhance the robustness of memory cells in various operational scenarios.

1.2 Objectives

In this work, the main focus is on the crucial problem of integrated circuit stability and noise margin, especially for memory arrays where reliability is critical. The 8T SRAM (Static Random-Access Memory) cell is a vital component in modern digital systems, responsible for efficient data storage and retrieval. Achieving effective skewness modifications within the 8T SRAM framework is the main objective. We aim to enhance stability and improve the Static Noise Margin (SNM) without compromising the speed and efficiency that make the 8T SRAM a desirable option for memory applications, thereby significantly improving its reliability in various operational conditions.

1.3 Literature survey

The authors of the paper titled **Area Optimization in 8T SRAM Cell for Low Power Consumption** covers 8T SRAM memory cell which have eight transistors whereas in a conventional SRAM have six transistors per cell. The additional two transistors act as an inverter which reduces the necessity of two input signal for bitline and bitline bar. So, this initially reduces the required input power. A dual-port cell (8T-cell) is created by adding two transistors; the read can be entirely decoupled from the write operation in an 8T cell by sensing the data through a separate read stack controlled by a separate read word lines (RWL).The power consumption is improved by varying the width and length of channels. SRAM cell is designed and simulated at 0.12m technology. The design is implemented in CMOS technology. Power consumption and frequency of memory cell have been observed from simulation result. This result have also verified by mathematical calculation. Power consumption is reducedby 12.34 percentage with respect to the previous works.[2]

The authors of the study titled **A Novel 8T SRAM Cell with Improved Read and Write Margins** A single-ended write design has comparative degradation in write performance in comparison to the conventional write structure using complementary bit-line pair. Nevertheless a dynamic mechanism of cutting feedback loop can effectively improve the write ability in the proposed 8T cell. In the write operation, WWL is set to VDD to prepare a path from internal node 'QB 'to BL and break the feedback loop. The RWL is set to VDD in the entire write operation.The proposed 8T SRAM cell improves the RSNM by at least 2.06x and as compared with conventional 6T SRAM cell. During the read operation, the bit-line is pre-charged to VDD, RWL is set to high. The WWL is set to low in the entire read operation, which turns off and turns on N3 and P3. As 'Q' node stores '1' logic (Q= '1', Q= '0'), the transistors N2, N5 and P1 are on and N1 as well as P2 is off.The proposed cell has been found to perform better in read and write. [1]

The authors of the paper **Performance and Area Optimization of SRAM Cell in Nanocomputing Application** This design has total 8 transistor.The requirement of read durability in 6T SRAM cell is enhanced with one separate read circuit which has two NMOS transistors NM5, NM6 . The internal node is totally isolated from read circuit, so data at internal nodes In write mode, read word line (RWL) is deactivated and write action is remaining same as 6T memory cell. In read mode, WL is deactivated and precharged the read bit line (RBL) then activates the RWL. The internal node P is connected to the gate of NM6. If data at P is 1, then NM6 is turned ON. There is a close path from RBL to ground through access transistor NM5 and NM6. Discharging current start flowing and voltage level of RBL starts reducing.[3]

1.4 Problem statement

In the design of integrated circuits, power consumption and delay play a vital role due to the increased necessity of efficient and reliable memory systems. Modern digital systems use 8T SRAM (Static Random-Access Memory) cells for efficient data storage and retrieval. Based on the structure of the 8T SRAM, the scope is to optimize its power consumption and reduce delay through effective skewness modifications. The study involves comparing various skew configurations to identify the optimal design for minimizing power and delay while maintaining high performance in different operational conditions.

1.5 Application in Societal Context

Applications for 8T SRAM (Static Random-Access Memory) cells in Complementary Metal-Oxide-Semiconductor (CMOS) technology are numerous across various domains, particularly in the realms of memory systems and digital circuit design. The following are a few potential uses and societal impacts:

1. **Memory Systems:** 8T SRAM cells are essential parts of memory systems in a variety of electronic devices, including computers, cellphones, and IoT devices. They provide rapid and effective data storage and retrieval, which improves the overall performance of the devices.

2. **Digital Circuit Design:** 8T SRAM cells are widely utilized in digital circuit architecture, including cache memory in microprocessors and FPGA (Field Programmable Gate Array) topologies. They provide dependability, low power consumption, and a high integration density, making them excellent for complicated digital systems.

3. **Data Security:** 8T SRAM cells help to provide data security and integrity in systems that require speedy and safe data access. They are employed in encryption and decryption procedures, safe key storage, and data buffering, which improves the overall security of digital systems.

1.6 Project Planning

The project uses 45nm CMOS technology to create an 8T SRAM cell. Goals include learning digital circuit design and having practical experience using CMOS technology. A detailed literature study guides the project's direction, defining the project's parameters as well as outlining the necessary tools and procedures. The design process follows strict standards, thanks to tools like Cadence Virtuoso. The 8T SRAM cell is tested and verified thoroughly to assure its operation and dependability. The project culminates in a final presentation and full report. Future efforts will center on investigating scalability and further improving the 8T SRAM architecture for improved performance.

1.7 Organization of the report

In the System Design phase, we will go over the thorough selection and integration of important components required to build an 8T SRAM (Static Random-Access Memory) cell. This phase will feature a full description of the components used, as well as insights into the functional block diagram of the SRAM cells. The goal is to lay a firm basis for the project's succeeding phases, culminating in the successful production of the components required for a working 8T SRAM cell.

The system architecture, algorithm, and flowchart that represent the end result of our work will be presented as we go on to the Implementation Details section. This detailed explanation will cover each stage of the design flow process and offer a comprehensive understanding of the project's execution plan.

The Optimization section will discuss the techniques used to improve our system's performance. Justifications will be provided together with a detailed explanation of numerous optimization approaches, providing insight into how these tactics contribute to the overall improvement of our system.

Results and Discussion will be dedicated to analyzing the conclusions drawn from our architecture's thorough investigation. Through an extensive discussion, this part will clarify the performance measures and validate the efficiency of our design selections.

The section titled "Conclusions and Future Scope" wraps up our analysis by summarizing the important discoveries and outlining future directions. This will involve a careful examination of our project's possible extensions and future directions, highlighting its ongoing significance for the advancement of the discipline.

Chapter 2

System design

In this chapter, we delve into the essential components integral to the architecture of our 8T SRAM (Static Random-Access Memory) cell for a single bit. The design implementation leverages transistor-level configurations and circuitry, strategically employed to optimize data storage and retrieval in binary format. Transistors are utilized to establish the storage node, access transistors, and control signals necessary for efficient read and write operations within the SRAM cell.

The initial phase of our design entails the meticulous crafting of the 8T SRAM cell at the transistor level for a single bit. This includes designing the storage node with 8 transistors, access transistors, and control signals necessary for efficient read and write operations. The focus is on ensuring stability, reliability, and fast access times for the single-bit SRAM cell.

Subsequently, rigorous simulations and analysis are conducted to verify the performance characteristics of the designed single-bit 8T SRAM cell. This includes evaluating read and write access times, stability margins, power consumption, and data integrity to ensure optimal functionality.

A critical phase in our exploration will focus on optimization techniques aimed at refining the single-bit 8T SRAM cell for improved power efficiency and data integrity. This chapter serves as a comprehensive exploration of the architectural elements, design intricacies, implementation procedures, verification methodologies, and an insightful exploration of optimization strategies for our single-bit 8T SRAM cell. The block diagram is shown in the figure2.1.

2.1 Functional block diagram

The figure 2.1 outlines the detailed process of designing an 8-transistor (8T) static random-access memory (SRAM) cell. The initial stage involves crafting the SRAM cell architecture using eight transistors to balance data storage stability, read/write access speeds, and power efficiency. The next stage, implementation, translates the design into a detailed circuit schematic, specifying the connections and functionality of each transistor. Following this, simulation and analysis mimic the circuit's behavior, allowing to identify and rectify issues. Finally, transistor-level optimization fine-tunes the design of individual transistors, improving performance metrics like read/write speeds and power consumption by adjusting transistor parameters. By following these stages, designers can create high-performing and reliable 8T SRAM cells.

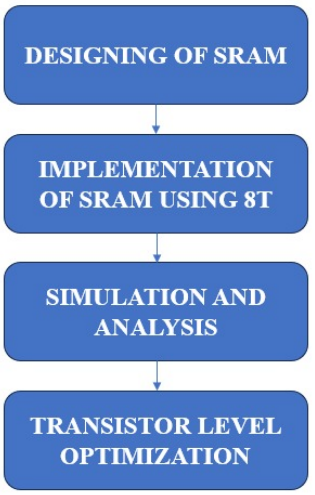

Figure 2.1: Block Diagram

2.2 Final design

The proposed 8T SRAM memory cell which have eight transistors whereas in a conventional SRAM have six transistors per cell. The additional two transistors act as an inverter which reduces the necessity of two input signal for bitline and bitline bar. So, this initially reduces the required input power

A dual-port cell (8T-cell) is created by adding two transistors; the read can be entirely decoupled from the write operation in an 8T cell by sensing the data through a separate read stack controlled by a separate read word lines (RWL).The remaining 6T portion of the cell is optimized for write, resulting in an overall lower Vmin. Separation of data retention element and data output element means that there will be no correlation between the read SNM Cell and I Cell. Thus, an 8T SRAM design [9] contains a write assist in which a horizontally routed VDD line is collapsed during write. As a result, the bit cell array Vmin is limited by the hold margin.[3]

Chapter 3

Implementation details

3.1 Specifications and final system architecture

In engineering and design, specifications serve as detailed recommendations that specify the properties and requirements of a system or component. For an 8T SRAM (Static Random-Access Memory) cell, specifications include information on the technology (e.g., CMOS 45nm), power supply voltage, number of transistors, EDA tools, operating conditions, input/output characteristics, and performance metrics. These specifications act as a guide, ensuring that the design meets the project's objectives and the capabilities of the available technology, allowing for efficient development and verification. A concise summary of these specifications is presented in the table 3.1 and the final architecture is showin in figure 3.1

Table 3.1: Specifications for 8T SRAM using CMOS 45nm Technology

Specification	**Value**
Technology	CMOS 45nm
Power Supply Voltage (Vdd)	1v
Number of Transistors	8
EDA Tool	Cadence Virtuoso

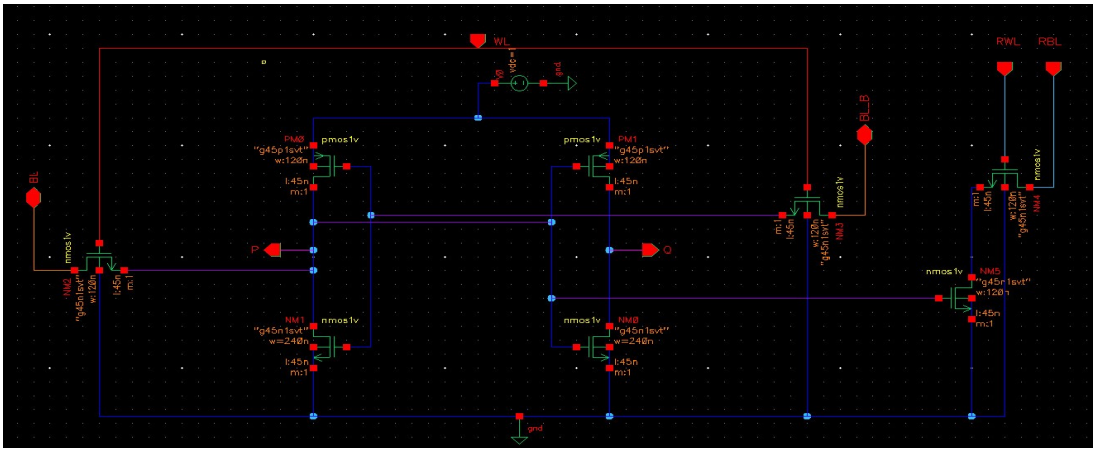

Figure 3.1: Design of 8T SRAM.

3.2 Algorithm

1. **Input:** Define the write enable (WL), read enable (RWL), and bit lines (BL, BL_bar, and RBL) for the 8T SRAM cell operation. These signals will control the data storage and retrieval processes.

2. **Initialize:** Initialize the SRAM cell by setting the initial states for the bit lines (BL, BL_bar and RWL) and the control signals (WL and RWL). This establishes the conditions necessary for either reading from or writing to the SRAM cell.

3. **Read and Write Operation:** The 8T SRAM cell performs both read and write operations efficiently. For a write operation, when the write enable (WL) signal is active, the input data is latched onto the bit lines (BL and BL_bar), and the write transistors store this data in the cell's storage nodes. For a read operation, the bit line (RBL) is precharged, and when the read enable (RWL) signal is active, the read operation works. The cell's stability and noise margin are maintained, and optimization techniques are used to minimize power consumption and ensure fast access times. The read operation outputs the stored data, verifying the cell's performance.

4. **Stability and Noise Margin:** In designing the 8T SRAM cell, assessing the Static Noise Margin (SNM) is critical to ensure stable operation amidst voltage fluctuations and external noise, thereby safeguarding data integrity. Another essential aspect involves optimizing transistor sizes to achieve a balance between read and write stability. This optimization ensures that the SRAM cell maintains reliable performance across varying operating conditions, enhancing its overall reliability and functionality.

5. **Optimization:** To enhance power efficiency in the 8T SRAM cell, optimizing the W/L (Width/Length) ratio of transistors is vital. This optimization reduces power consumption during read and write operations while maintaining fast access times for improved performance and energy efficiency.

6. **Output:** The data output of the 8T SRAM cell corresponds to the retrieved data during a read operation, reflecting the stored value. Performance evaluation involves assessing key metrics like read/write access times, power consumption, and Static Noise Margin (SNM) to validate the efficiency and effectiveness of the SRAM cell design. This comprehensive analysis ensures optimal functionality and reliability in data storage and retrieval operations.

3.3 Flowchart

The flowchart, illustrating the sequential design flow and the tools employed, is further detailed in figure 3.2. This visual representation succinctly outlines the steps of the design process and identifies the specific tools integral to the successful execution of the project.

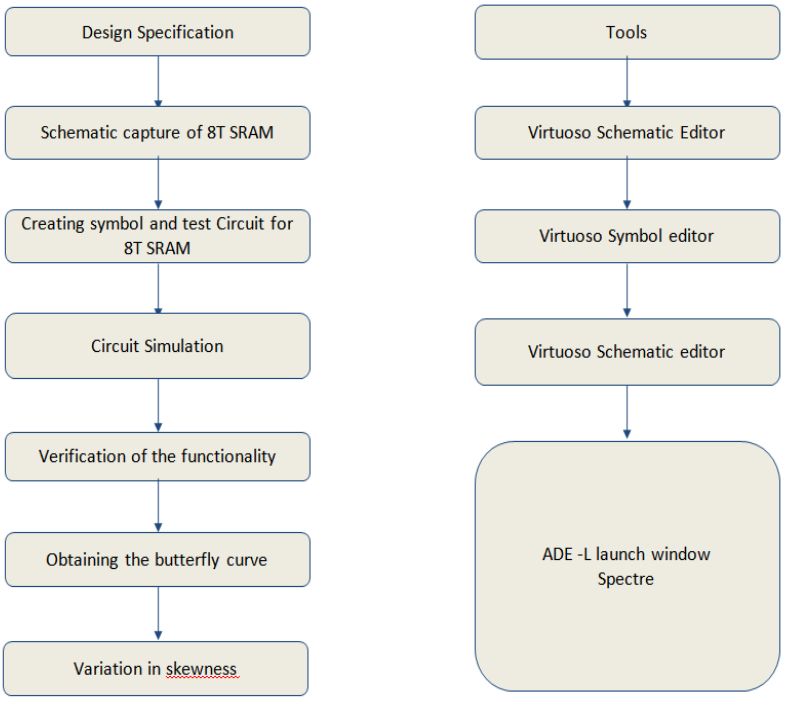

Figure 3.2: Flowchart.

Chapter 4

Optimization

4.1 Introduction to optimization

Optimizing an 8T SRAM cell using CMOS 45nm technology is crucial for enhancing performance, reducing power consumption, and ensuring efficient utilization of resources. This optimization process involves a systematic approach to refine the design, circuitry, and overall architecture. An important step in optimizing the 8T SRAM cell in CMOS 45nm technology involves carefully adjusting the W/L ratios of transistors and minimizing skewness to improve efficiency and performance.

4.2 Types of Optimization

A variety of optimization approaches are essential for improving performance, increasing efficiency, and addressing important design problems in the field of digital circuit design. The following summarizes a wide range of optimization techniques:

1. **Transistor Sizing:** Optimizing the width-to-length (W/L) ratio of each transistor in the 8T SRAM cell is crucial for balancing drive strength, power consumption, and speed. Proper sizing ensures that the transistors provide adequate drive current for fast read and write operations while minimizing leakage and dynamic power consumption. Adjusting the drive strength of the transistors helps achieve reliable performance without unnecessary power usage, contributing to the overall efficiency and effectiveness of the SRAM cell.

2. **Static Noise Margin (SNM):** Improving the Static Noise Margin (SNM) involves strengthening the cross-coupled inverters by optimizing the sizing of the pull-up and pull-down transistors ensures that the stored data remains stable under noisy conditions. These adjustments are critical for maintaining data integrity and reliability in the presence of voltage fluctuations and external noise.

3. **Skewness Minimization:** Minimizing skewness involves designing the transistors symmetrically in the read and write access paths to ensure balanced signal propagation. Using matched transistor pairs in critical paths reduces timing mismatches, which enhances performance consistency and reliability. These design considerations are crucial for maintaining uniform access times and stable operation across the SRAM cell.

4.3 Selection and justification of optimization method

The approach of optimizing transistor sizing (W/L ratio) and adjusting skewness is preferable for designing an 8T SRAM cell due to its specific advantages. Optimizing the W/L ratio ensures a balance between read/write stability and power efficiency, which is crucial for energy-efficient devices. Adjusting skewness helps in reducing access time and improving overall circuit performance by minimizing delays. This method simplifies the design by fine-tuning transistor parameters, ensuring effective use of space and compatibility with modern semiconductor technology. The flexibility of this approach allows it to be tailored to meet specific design requirements. In conclusion, the optimization method of fixing W/L ratio and adjusting skewness is selected for its superiority in enhancing stability, power efficiency, and performance, making it suitable for the demands of modern high-performance memory applications.

Chapter 5

Results and discussions

5.1 Result Analysis

The transient response analysis of the 8T SRAM cell provides insights into its behavior under changing input conditions, particularly in terms of stability and power efficiency. The design philosophy of the 8T SRAM cell, prioritizing stability and efficient read/write operations, is evident in its transient performance characteristics.

In the context of the 8T SRAM, the transient response demonstrates a rapid and efficient adaptation to input changes. The specialized design, guided by the careful arrangement of eight transistors, contributes to minimal power fluctuations and stable data retention during alterations in input signals. This design ensures not only efficient power utilization but also emphasizes the importance of maintaining stability and reliable data storage.

Furthermore, the optimization through transistor sizing (W/L ratio) and skewness adjustment enhances the 8T SRAM cell's performance. The fine-tuned transistor parameters and skewness adjustments contribute to minimal power fluctuations and improved access times during read/write operations. This optimized design places a strong emphasis on efficient power utilization and stability, highlighting the significance of its tailored structure for modern high-performance memory applications. The results are shown in the table 5.1

Table 5.1: Analysis Results

Sl.No	Technology	Skewness	Power Dissipated	Write 1 delay	Read 0 delay	SNM
1	45nm	Low	1.642 μW	35 .01 ns	25.01 ns	0.45 V
2	45nm	High	2.247 μW	35.02 ns	25.00 ns	0.40 V
3	45nm	Balanced	1.638 μW	35.00 ns	25.01 ns	0.42 V

Figure 5.1 illustrates the transient behavior of the 8T SRAM, detailing both read and write operations. Figure 5.2 presents the DC analysis (Butterfly Graph), which provides the Static Noise Margin (SNM) value. These figures collectively offer a comprehensive view of the 8T SRAM's operational characteristics and stability.

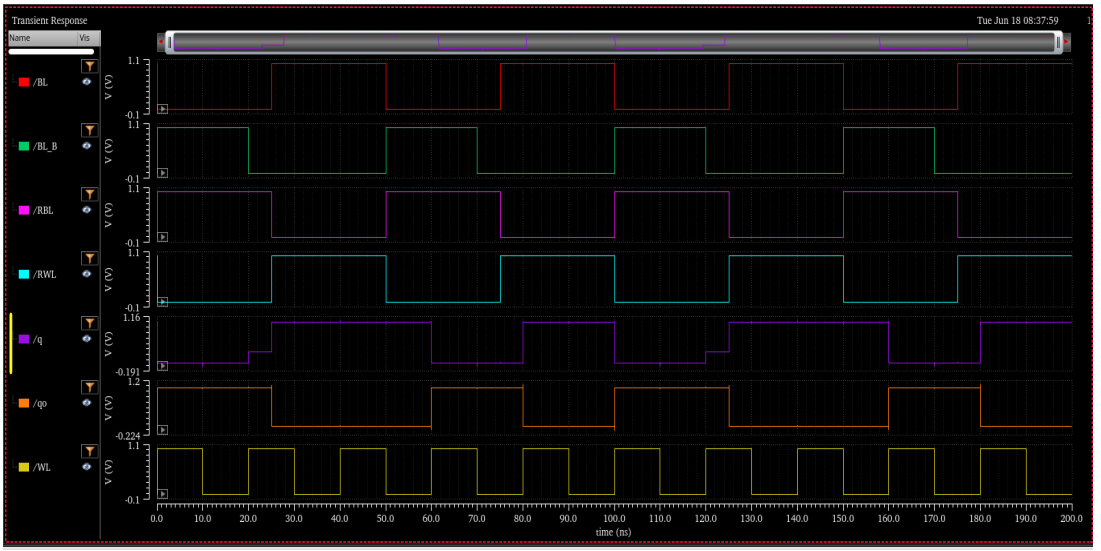

Figure 5.1: Transient analysis

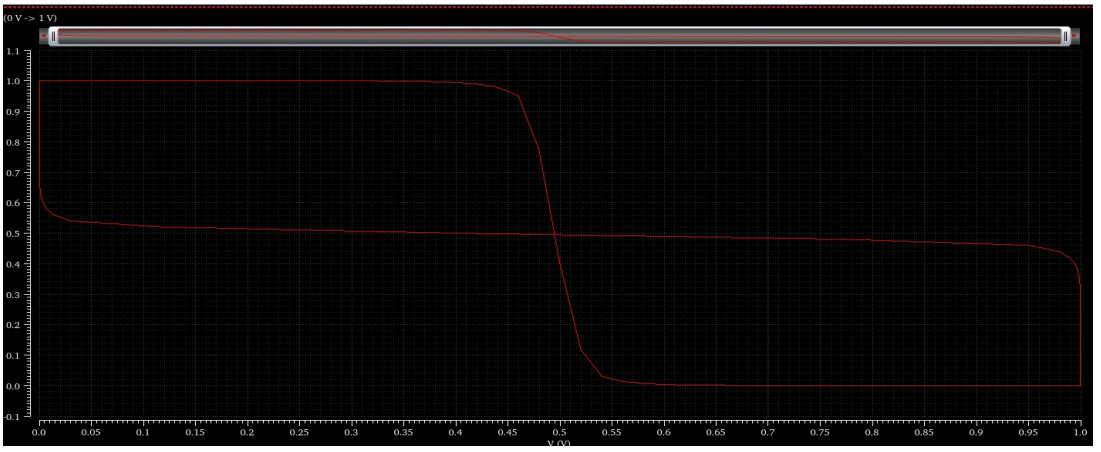

Figure 5.2: Butterly curve

5.2 Discussion on optimization

When 8T SRAM cells are carefully examined with varying skewness settings, it becomes clear that certain configurations perform better in terms of stability and power efficiency. The data in Table 5.1 indicates that optimizing skewness in 8T SRAM designs significantly enhances stability and reduces power usage compared to other configurations. This finding highlights the effectiveness of adjusting skewness as a powerful method for improving 8T SRAM cells, especially in applications where stability and power efficiency are crucial design factors. The ability of skewness-optimized 8T SRAM designs to achieve superior performance is a remarkable result, showcasing their potential to make significant contributions to advancements in digital memory design.

Chapter 6

Conclusions and future scope

6.1 Conclusion

The power consumption analysis of 8T SRAM cells reveals distinct trade-offs between performance and efficiency based on balanced skewness settings. Optimal skewness configurations significantly lower power consumption and access delays compared to other designs, as demonstrated in the findings detailed in Table 5.1. This emphasizes the effectiveness of balanced skewness in enhancing the efficiency of 8T SRAM cells, making them suitable for applications where minimizing energy usage and optimizing performance are critical considerations. The ability of skewness-balanced 8T SRAM designs to achieve superior power efficiency and reduced delays highlights their potential to meet demanding requirements in digital memory technologies.

6.2 Future scope

The future scope for the 8T SRAM cell designed using 45nm CMOS technology involves a thorough exploration of power-performance optimization and scaling possibilities across various nodes, including 32nm and lower. The research agenda encompasses an in-depth examination of the SRAM's integration into advanced memory architectures and large-scale memory arrays. This includes implementing sophisticated power optimization strategies, enhancing data security mechanisms, and refining layout designs for heightened area efficiency. Additionally, developing techniques for improving array-level performance, such as optimizing bit-line and word-line structures, is crucial. These initiatives aim to fortify the 8T SRAM cell's adaptability to evolving technological demands, particularly in the realms of high-performance computing, secure data storage applications, and efficient large-scale memory arrays.

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