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#### > Introduction

- ► The project aims to implement Edge Detection for an image using Sobel Operator on a Field Programmable Gate Array(FPGA) device.
- ► The Edge Detection is an Image Processing Technique for finding the boundaries of objects within image.
- ▶ It works by detecting discontinuities in brightness.
- Edge Information for a particular pixel is obtained by exploring the brightness of pixels in the neighbourhood of that pixel.
- Edge Detection is used for Image Segmentation and Data Extraction in areas such as Image Processing, Computer Vision and Machine Vision.





Fig. Edge Detection



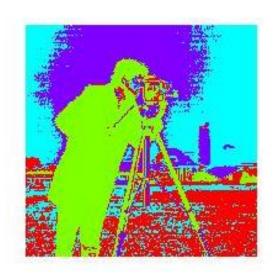


Fig. Image Segmentation

### Edge Detection Theory

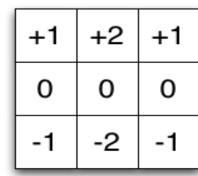
- An edge can be defined as an abrupt change in brightness as we move from one pixel to its neighbour. In digital image processing, each image is quantized into pixels.
- ▶ With grayscale images, each pixel indicates the level of brightness of image in a particular spot: 0->black, 255->white with 8-bit pixels.
- ▶ If, for a particular pixel, all the pixels in neighbourhood have almost same brightness, probably there is no edge at that point.
- Detecting edges is an important task in boundary detection, motion estimation, texture analysis and object identification.

## Sobel Edge Detection Operator

- Sobel Operator, as it is commonly known, is used particularly within edge detection algorithms where it creates an image emphasising edges.
- It is named after Irwin Sobel.
- ► It uses two 3×3 kernels(or masks) which are convolved with the original image to calculate approximations of its derivative-one for horizontal and one for vertical.

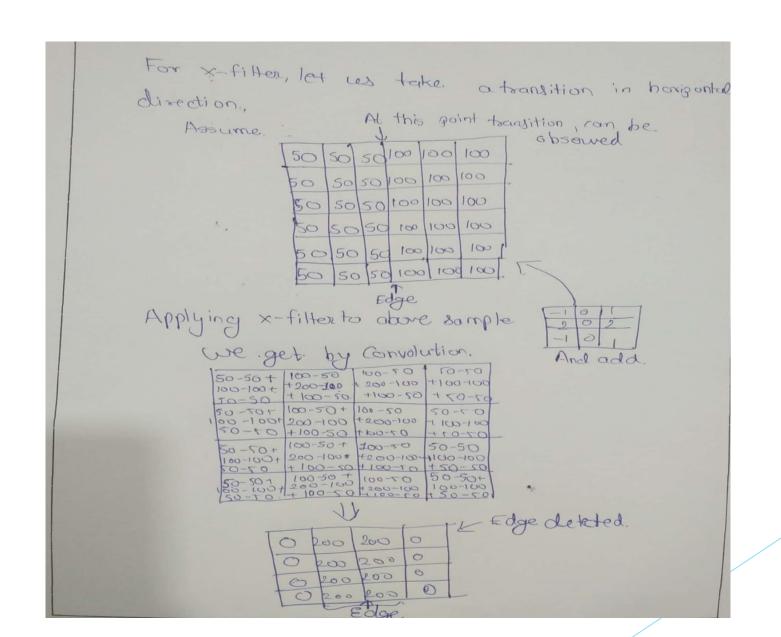
-1	0	+1
-2	0	+2
-1	0	+1

x filter



y filter

An example can be demonstrated as following.



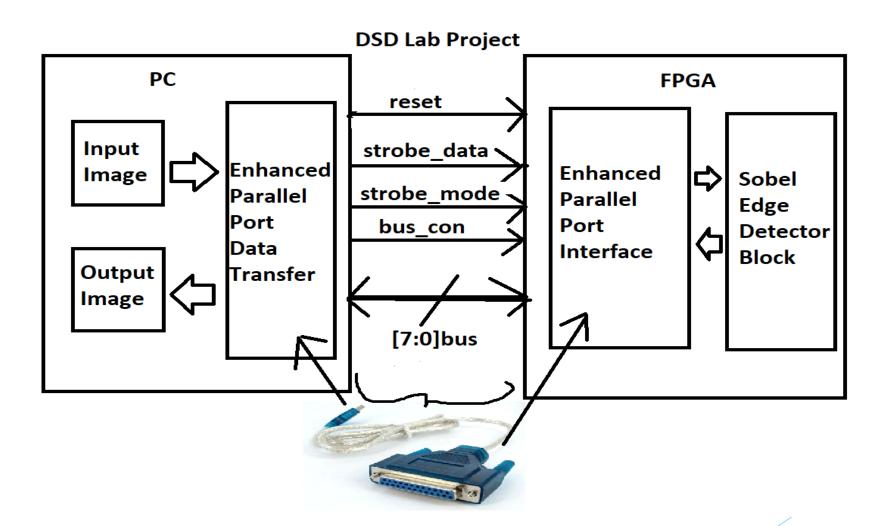
## Relevance of Hardware Implementation

- ► The implementation of image edge detection on hardware is important for increasing processing speed of image processing systems.
- ► Edge detection is a very complex process affected by noise. A number of operators are defined to solve the problem of edge detection.
- ► They are effective for certain images, but not suitable for others. Since, it is a very crucial step in Image Processing, we need a more faster, efficient solution.
- Software Implementation can be slower due to limited processor speed, so a dedicated hardware for edge detection can be helpful in Efficient Implementation

#### > PC Interface

- The first step involves in converting the image to a processable data format i.e. in pixels for further actions.
- A pixel data file has to be generated which contains data about image in a form where we use 8-bits to represent a pixel.
- This file is now suitable for providing data for our digital system and enable the further processing steps.
- ► A parallel port or similar communication ports help in transfer of this data to the FPGA interface. But, one major problem can be mostly with operating voltages at parallel ports (generally, 5V) and for FPGAs(Spartan 3 Series, 3.3.V).
- So, generally to comply with the uninterrupted two-way communication, a transceiver such as IC 74LS641 (20 pin DIP IC, two data buses) can be used at the interface.

## Overview of System



### Software Implementation

- The software implementation is the complete execution of the project undertaken based solely on Xilinx Vivado Tool along with some supported files which enable us to see the results of the implementation
- ► This section can be classified into a few steps based on the process undertaken sequentially for implementation
- Verilog Design Code
- Creating Testbench for a given Input Image
- Simulation and Fetching Output

- We already know about the evaluation of edges by operator
- In the Verilog Design module, the 8 pixel values are the neighbouring values for a single pixel with values ranging from 0-255 (8-bit) and 'edges(8-bit output)' is the final value of evaluation
- The x & y are the mathematical calculation based (in pixels term)

  where x= (upper right upper left) + 2\*(middle right middle left)+

  (lower right lower left)

  y= (upper left lower left) + 2\*(upper centre lower centre) +

  (upper right lower right)
- Now, the edges can be in any direction i.e. transition from left to right can be either lower->higher pixel value or vice versa and similarly for y-direction Hence, mod\_x and mod\_y are required to treat any transition as edge
- Next ,we will take the resultant of both.
- Finally, the resultant value is obtained but when back conversion to image will take place, the maximum pixel value should not exceed 255, therefore any value greater than 255 is scaled down to 255 to avoid any error.

#### Creating Testbench for a given Input Image

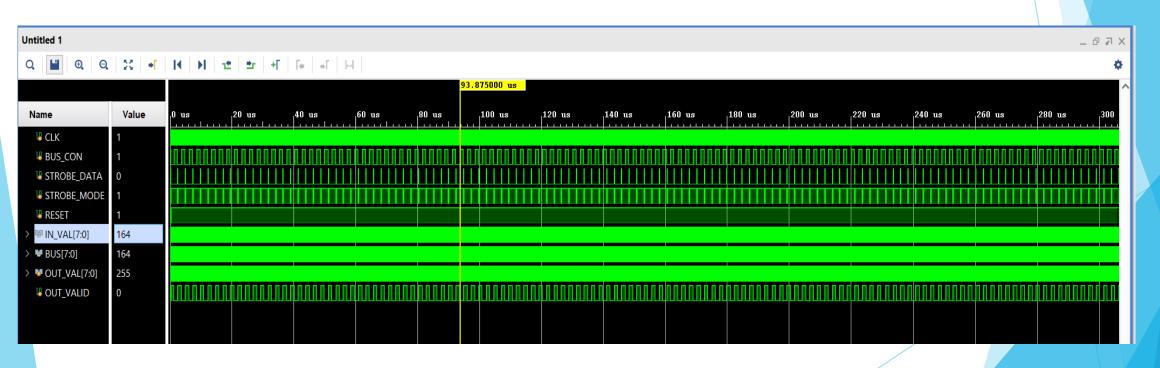
```
rom PIL import Image
img = Image.open('tstan.png').convert('L')
 WIDTH, HEIGHT = img.size
 data = list(img.getdata())
 data = [data[offset:offset+WIDTH] for offset in range(0, WIDTH*HEIGHT, WIDTH)]
              or row in data:
                         print("BUS_CON=0;OUT_VALID=1;STROBE_DATA=0;STROBE_MODE=1; OUT_VAL=")
                        print(';#10 OUT_VAL='.join('{:3}'.format(value) for value in row)) #WRITE
           print('$write("%d, ", IN_VAL);#10 $write("%d, ",
                         print('$write("%d, ", IN_VAL);#10 $write("%d, ",
                         print("BUS_CON=0;OUT_VALID=1;STROBE_MODE=0;STROBE_DATA=1; #10 ") #DISPLAY
```

- The python code will help us generate testbench for the Verilog code with respective write, shift and display conditions.
- The testbench can be copied and pasted inside an initial block as given below and observe the output.

```
`timescale 1ns / 1ps
module tss_tb;
reg CLK,BUS_CON,STROBE_DATA,STROBE_MODE,RESET;
wire [7:0]IN VAL;
wire [7:0]BUS;
reg [7:0]OUT VAL;
reg OUT VALID;
test_just_2 T1(.clk(CLK),.bus(BUS),.bus_con(BUS_CON),.strobe_data(STROBE_DATA),.strobe_mode(STROBE_MODE),.reset(RESET));
assign IN VAL =BUS;
assign BUS = (OUT VALID==1'b1)? OUT VAL : 8'hZZ;
initial begin
CLK=0;
forever
#5 CLK=~CLK;
end
initial begin
RESET=0;
#10
RESET=1;
//Take auto generated testbench from python file
$finish;
end
endmodule
```

### Simulation and Fetching Output

- The simulation can be done and we can see the pixel outputs on our Tcl Console
- We've already designed the output such that we will get the pixel s for edgedetected image.

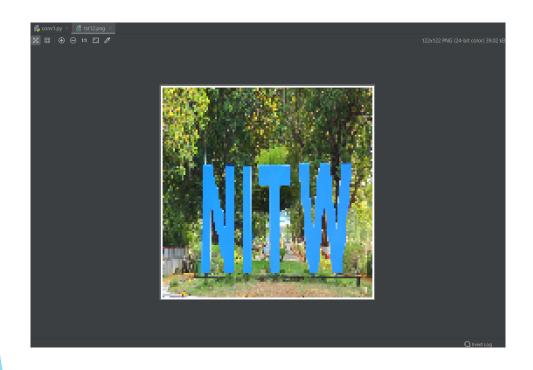


198, 200, 208, 214, 222, 228, 228, 228, 236, 246, 248, 244, 242, 246, 252, 250, 244, 240, 238, 230, 242, 242, 244, 242, 248, 236, 234, 238, 250, 254, 248, 255, 255, 255, 25 8, 24, 12, 24, 34, 20. 56, 54, 36, 74, 100, 108. 1 64, 114, 82. 148. 1 80, 86, 144, 118, 72, 160, 134, 94, 136, 142, 90, 72, 56, 122, 38. 24, 18, 12, 12, 14, 22, 30, 48, 82, 96, 114, 102, 18, 16, 16, 16, 40, 46, 82, 100, 26, 36, 40, 30, 18, 16, 12, 14, 18, 24, 50, 74. 70. 60. 24, 24, 116. 66, 116, 76. 112, 6, 14, 6. 30, 58, 54, 44, 60, 52, 42, 44, 24, 36, 72, 92, 70, 26, 34, 72, 24, 36, 56, 38, 84, 12, 26, 38, 8, 58, 78, 124, 104, 123. 6, 4, 8, 14, 14, 28, 72, 90, 36, 64, 64, 16, 52, 50, 40, 22, 18, 42, 8, 54, 98, 38, 72, 86, 118, 50, 135, 12, 12, 14, 6, 8, 4, 8, 68, 20, 78, 68, 8, 36, 56, 36, 52, 70, 114, 90, 10, 118, 22, 26, 40, 68, 20, 46, 56, 56, 84, 92, 128, 114, 24, 14, 40, 66, 86, 96, 112, 78, 68, 12, 16, 26, 52, 30, 56, 52, 72, 132, 176, 108, 78, 72, 112, 118, 104, 10, 20, 14, 4, 70, 42, 72, 20, 66, 4, 8, 74, 74, 92, 64, 168, 160, 6, 140, 94, 98, 92, 14, 46, 44, 54, 14, 10, 14, 22, 30, 22, 26, 42, 68, 42, 102, 72, 200, 88, 130, 162, 68, 90, 86, 88, 76, 16, 66, 66, 70, 14, 38, 26, 20, 20, 60, 70, 18, 134, 172, 68, 146, 96, 42, 118, 72, 42, 76, 66, 46, 130, 10, 12, 16, 32, 28, 36. 26. 40. 32, 22, 18, 34, 70, 20, 120, 154, 98. 46, 136, 70, 52, 134, 50, 46, 18, 74, 80, 124, 128, 127, 16, 24, 22, 30, 24. 32, 38, 26, 10, 14, 2, 24, 68, 18, 122, 128, 44, 56, 164, 88, 66, 132, 44, 86, 56, 118, 16, 168, 76. 129. 24, 26, 22, 16, 18, 18, 4, 18, 32, 78, 20, 144, 96, 38, 86, 152, 66, 44, 126, 46, 94, 98, 124, 54, 48, 202, 128, 20, 16, 16, 14, 4, 2, 22, 22, 12, 20, 52, 22, 120, 112, 46, 78, 112, 64, 50, 110, 38, 66, 88, 82, 18, 136, 186, 56. 125, 14, 14, 14, 6, 6, 22, 20, 14, 14, 56, 30, 72, 120, 6, 76, 106, 74, 34, 70, 34, 38, 68, 38, 28, 188, 116. 2, 12, 20, 26, 28, 4, 8, 20, 24, 34, 114, 52, 26, 104, 120, 20, 62, 36, 22, 52, 24, 44, 188, 60, 1 16, 104, 160, 122, 14, 8, 4, 14, 14, 24, 32, 28, 34, 28, 112, 80, 46, 92, 124, 56, 56, 24, 16, 48, 88, 110, 119, 6, 12, 10, 16, 8, 8, 6, 10, 10, 4, 14, 48, 12, 68, 86, 46, 94, 140, 64, 24, 26, 16, 42, 8, 134, 88, 114, 78, 120, 10, 12, 0, 4, 4, 8, 6, 4, 40, 32, 40, 90, 62, 88, 56, 30, 36, 6, 40, 20, 130, 66, 114, 12, 70, 38, 129, 14, 8, 6, 10, 6, 10, 14, 10, 14, 16, 10, 2, 8, 36, 62, 48, 60, 56, 80, 30, 22, 12, 22, 12, 94, 58, 42, 10, 58, 72, 22, 20, 28, 40, 42, 88, 18, 72, 126, 6, 10, 10, 8, 6, 6, 36, 20, 60, 10, 10, 14, 12, 12, 12, 48, 88, 48, 24, 22, 32, 78, 48, 121, 4, 20, 10, 6, 2, 14, 46, 44, 24, 54, 88, 48, 74, 54, 10, 8, 4, 4, 12, 12, 58, 56, 20, 24, 14, 40, 58, 28, 48, 40, 12, 52, 14, 72, 243, 16, 10, 20, 12, 14, 14, 18, 20, 14, 48, 38, 62, 40, 14, 4, 54, 62, 26, 38, 42, 42, 18, 14, 46, 254. 12. 10. 4. 12. 6. 16. 26. 30. 14. 14. 50. 56. 28. 26. 58. 70. 18. 40. 60. 44. 10.

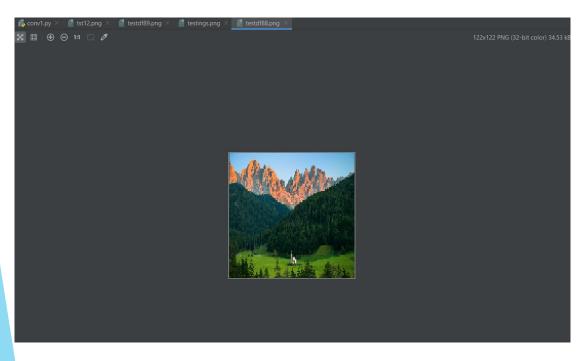
- Now we can copy the contents of Tcl Console to another python file to obtain the image back from pixel data.
- We will paste the contents inside the pixels=[] array in the given python file

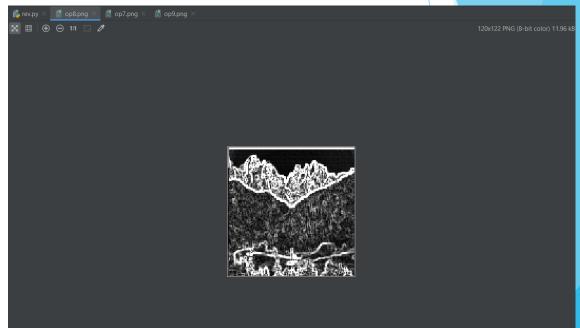
```
from PIL import Image
import numpy as np
pixels = [
# Convert the pixels into an array using numpy
array = np.array(pixels, dtype=np.uint8)
new_image = Image.fromarray(array)
new_image.save('op10.png')
```

- Now we got the output from the given input and we've completed the software implementation
- Some Examples :









#### References

► Basic Idea

https://www.hackster.io/

- Wikipedia https://en.wikipedia.org/wiki/Sobel\_operator
- Sobel Operator https://www.youtube.com/watch?v=uihBwtPIBxM

# Thank You!