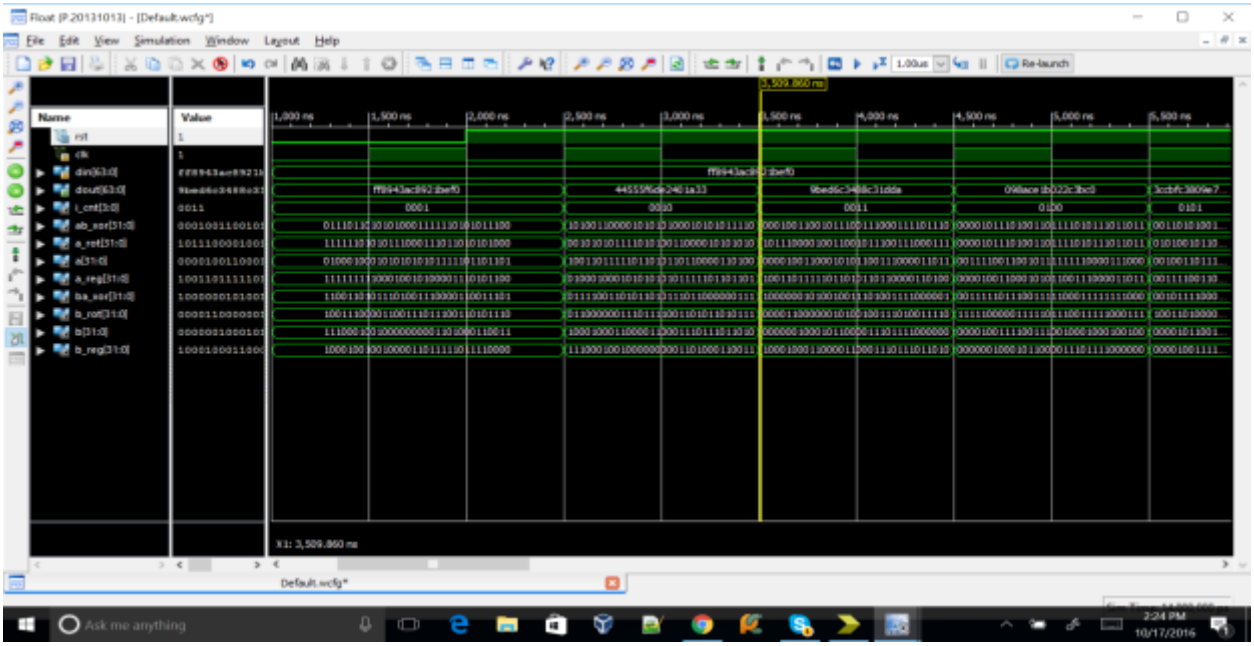
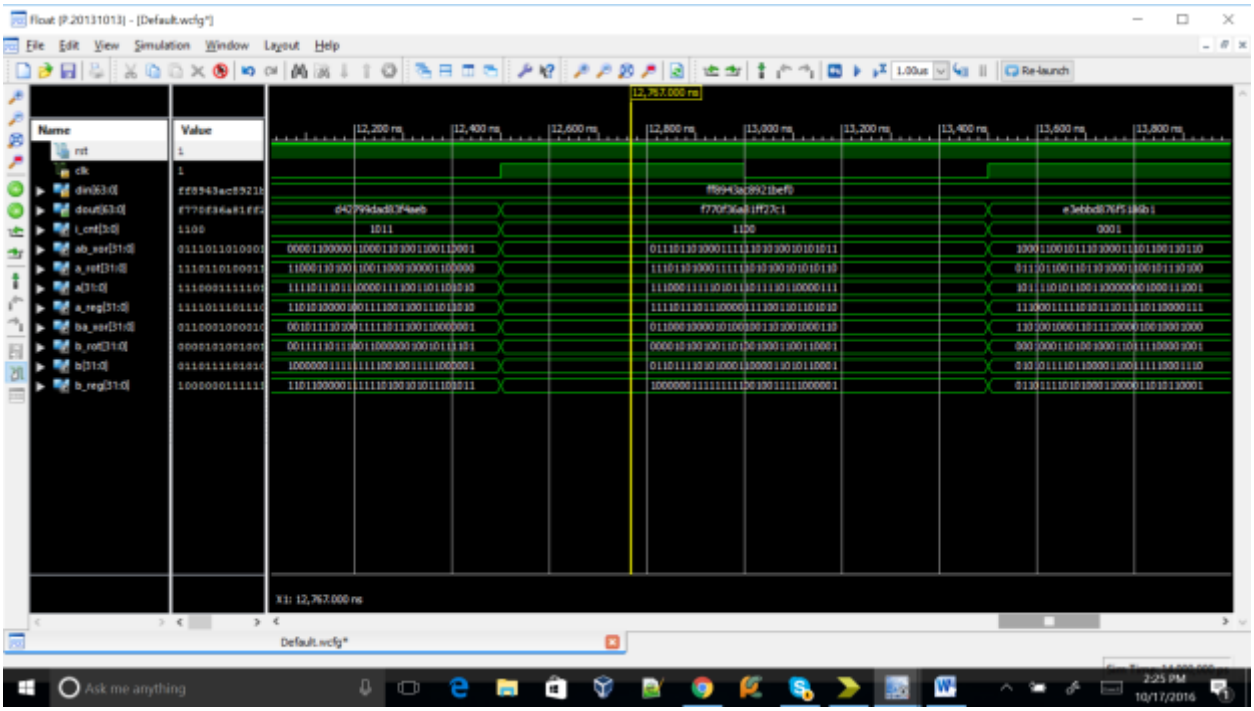
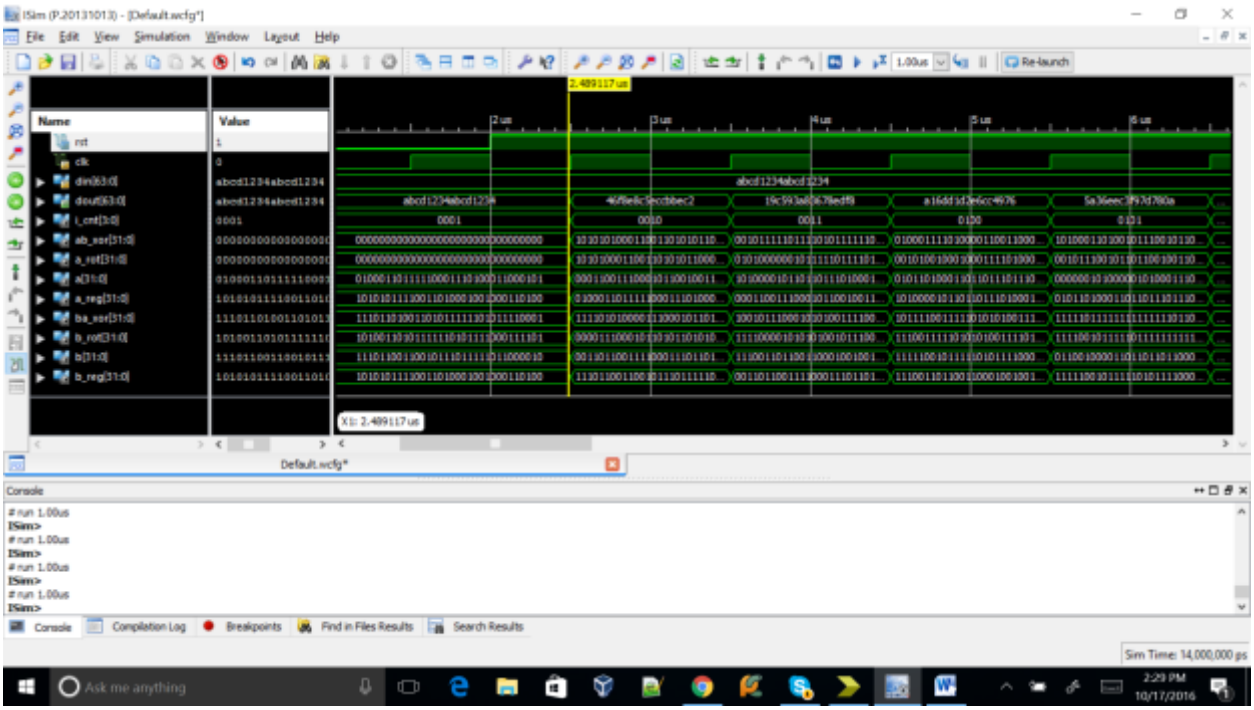
Lab 3
Pratik Thakker
Pat323

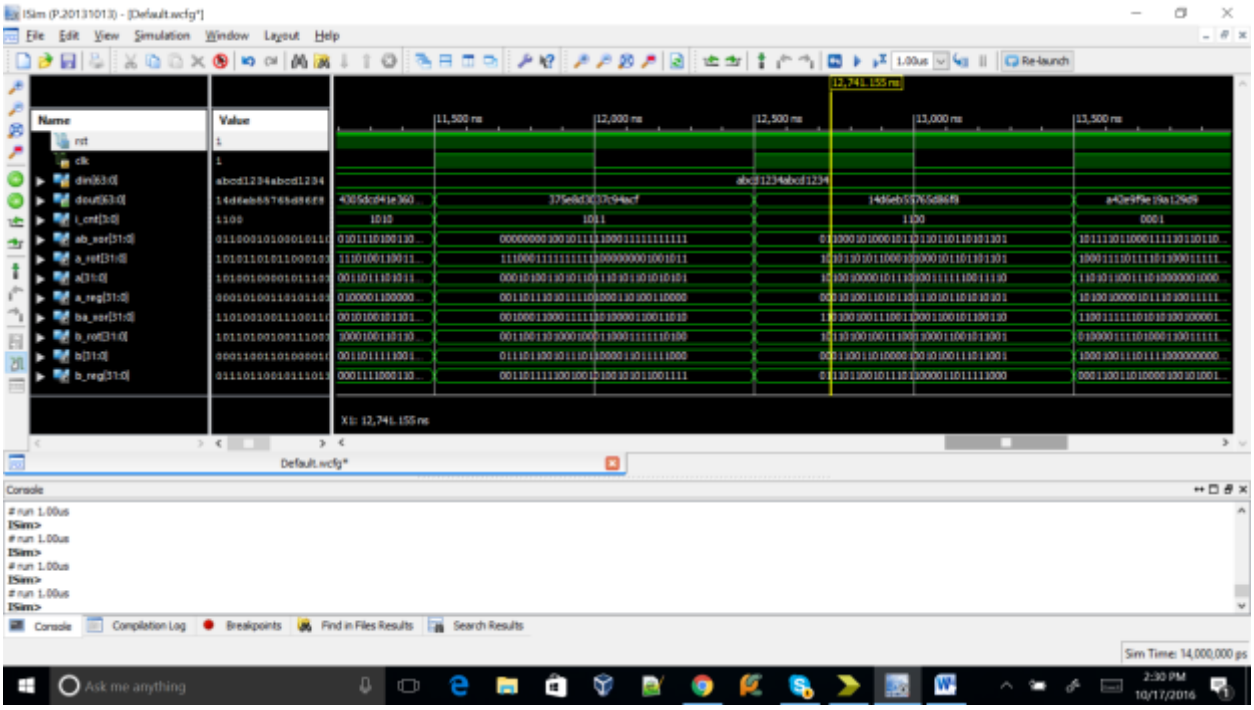
1 function



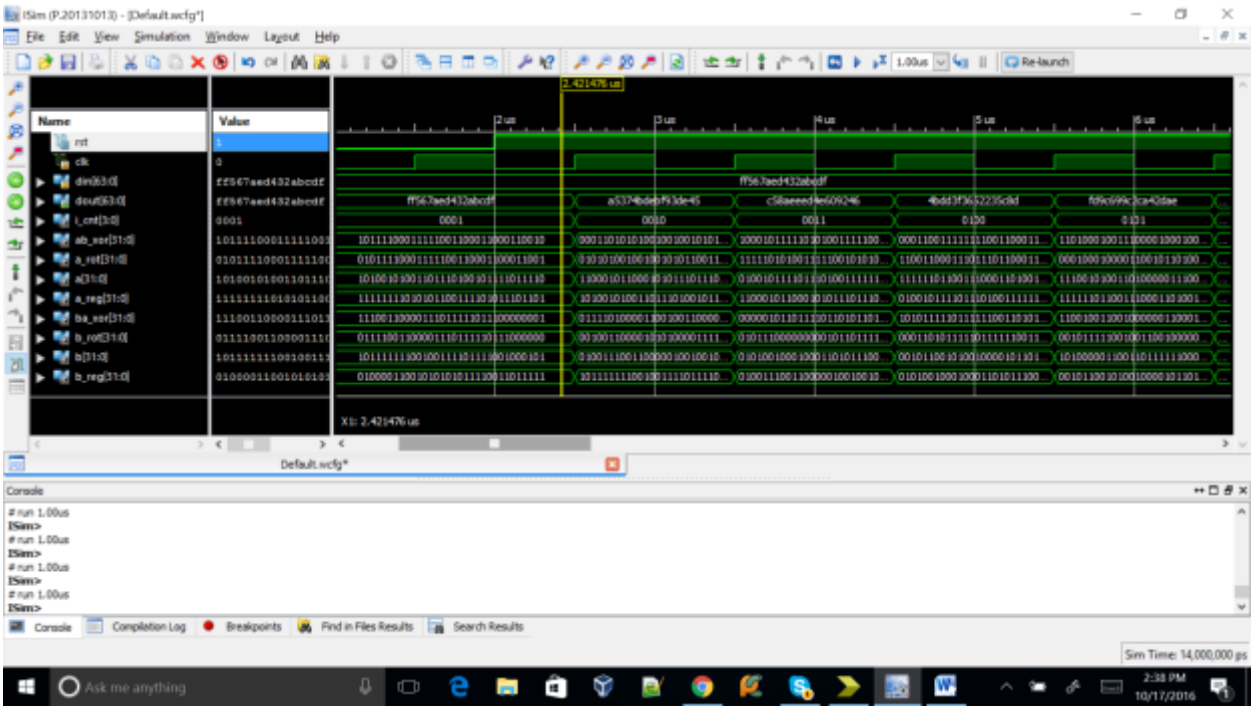


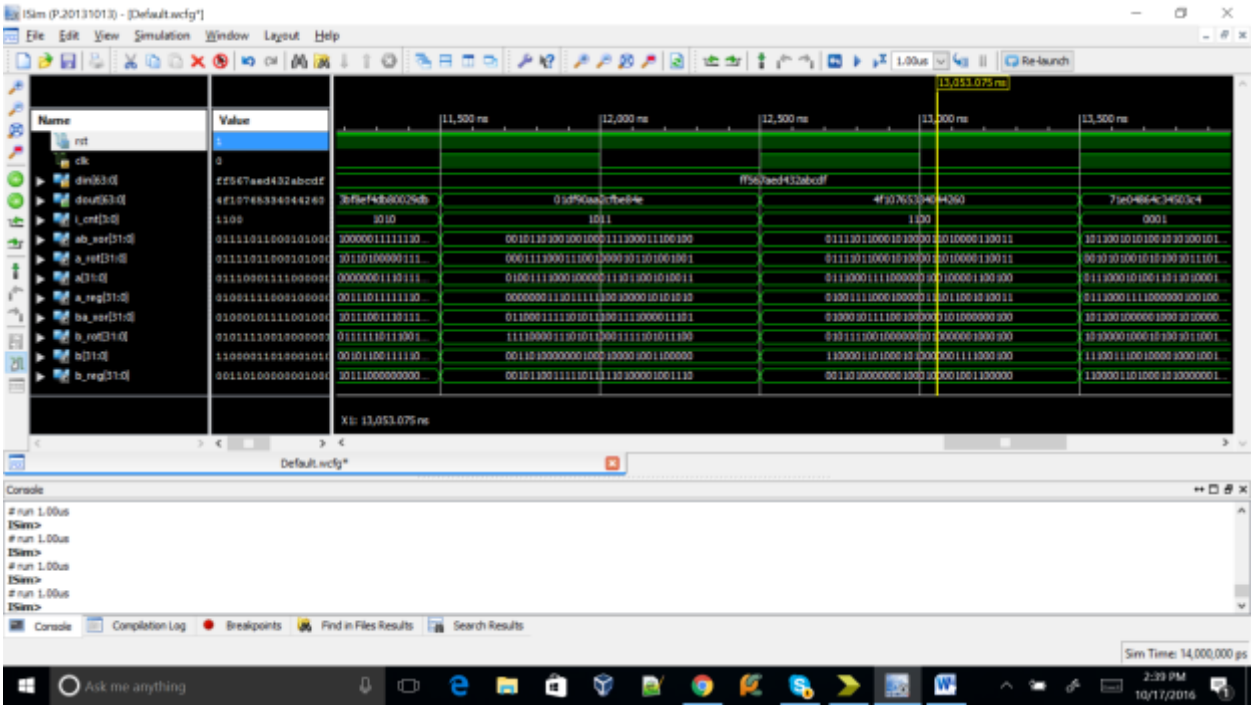
Lab 3
Pratik Thakker
Pat323



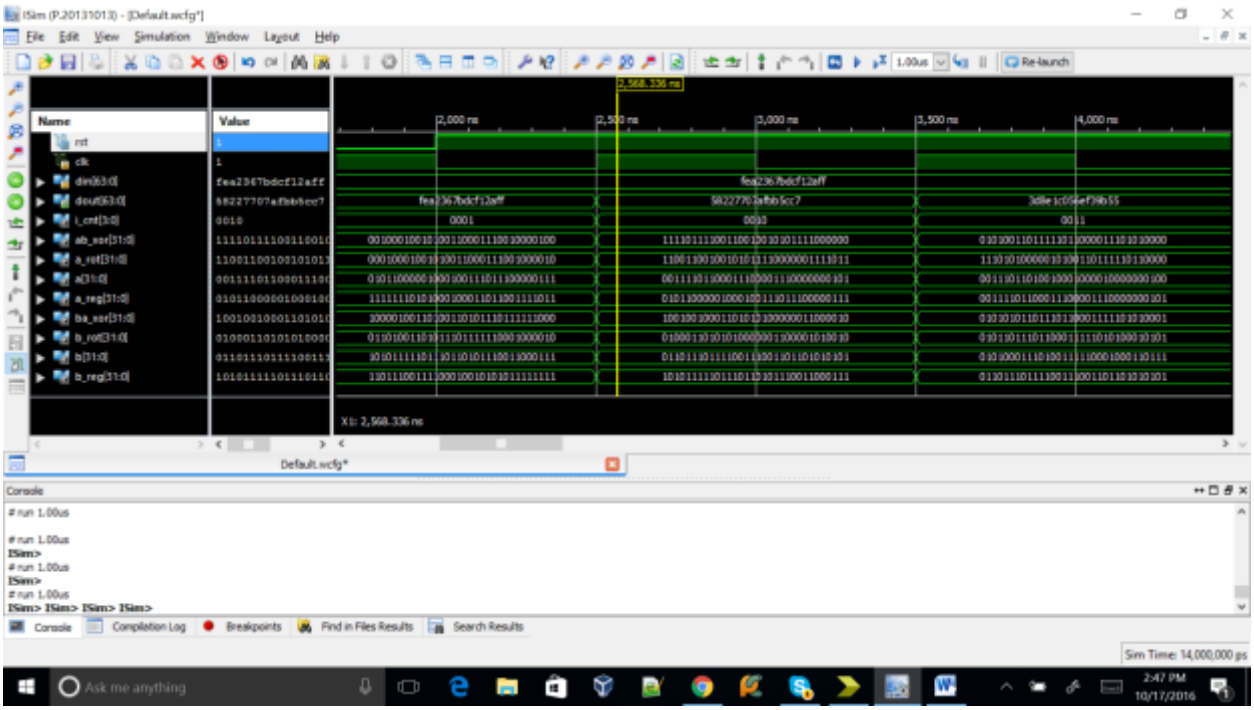


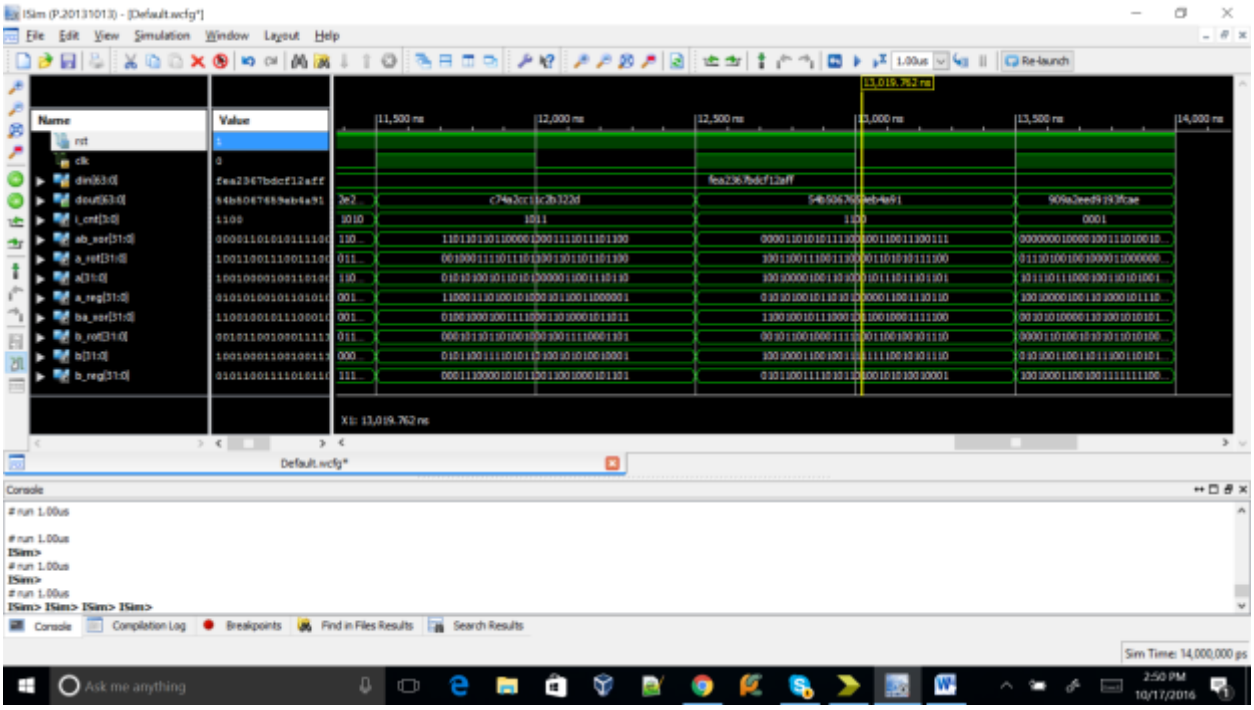
Lab 3
Pratik Thakker
Pat323



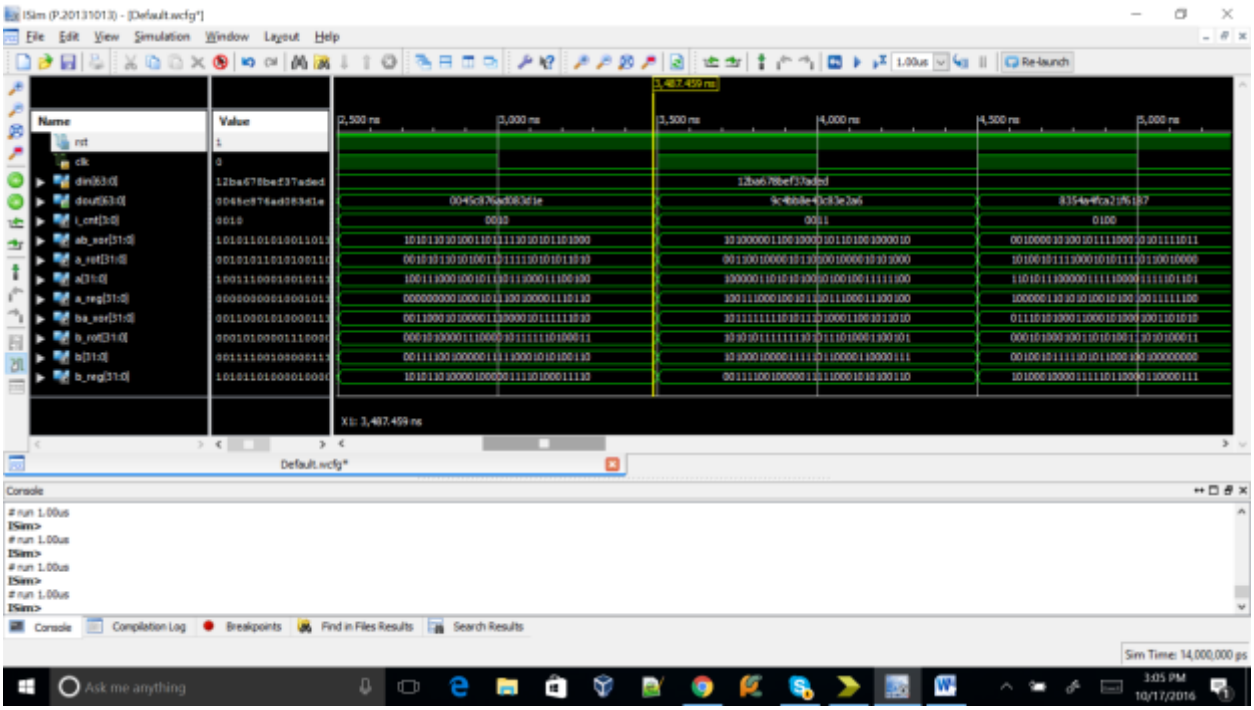


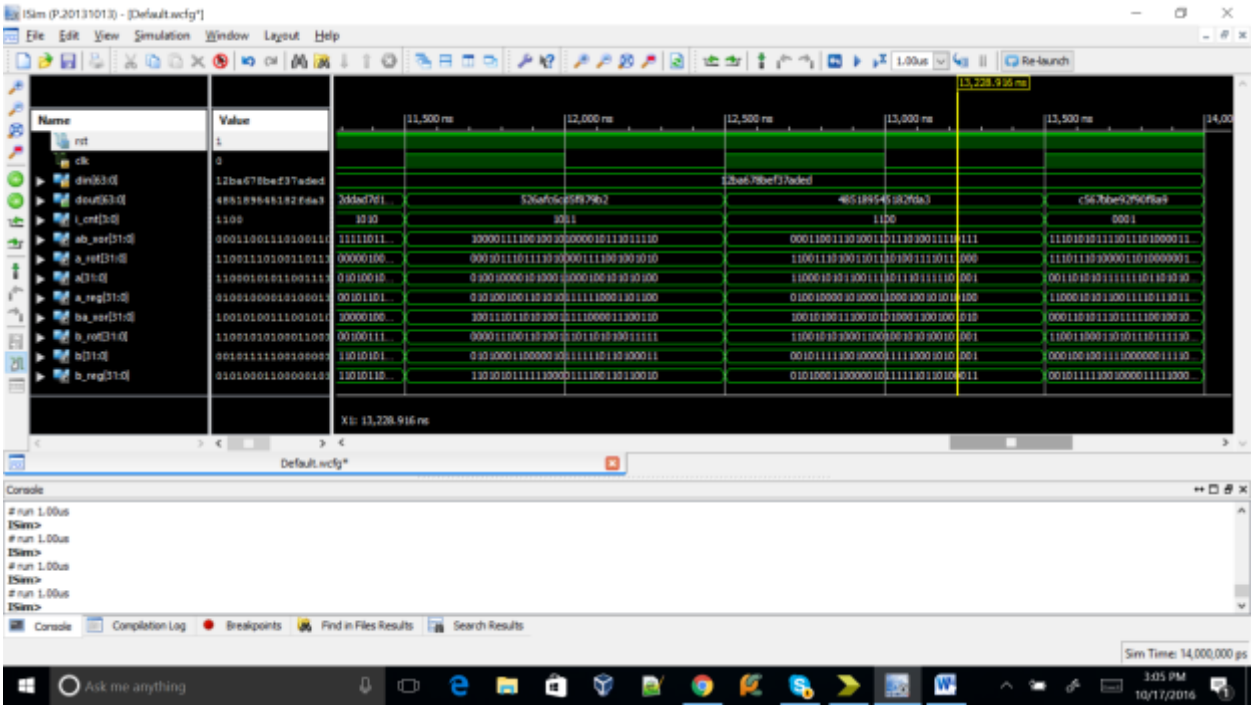
Lab 3
Pratik Thakker
Pat323



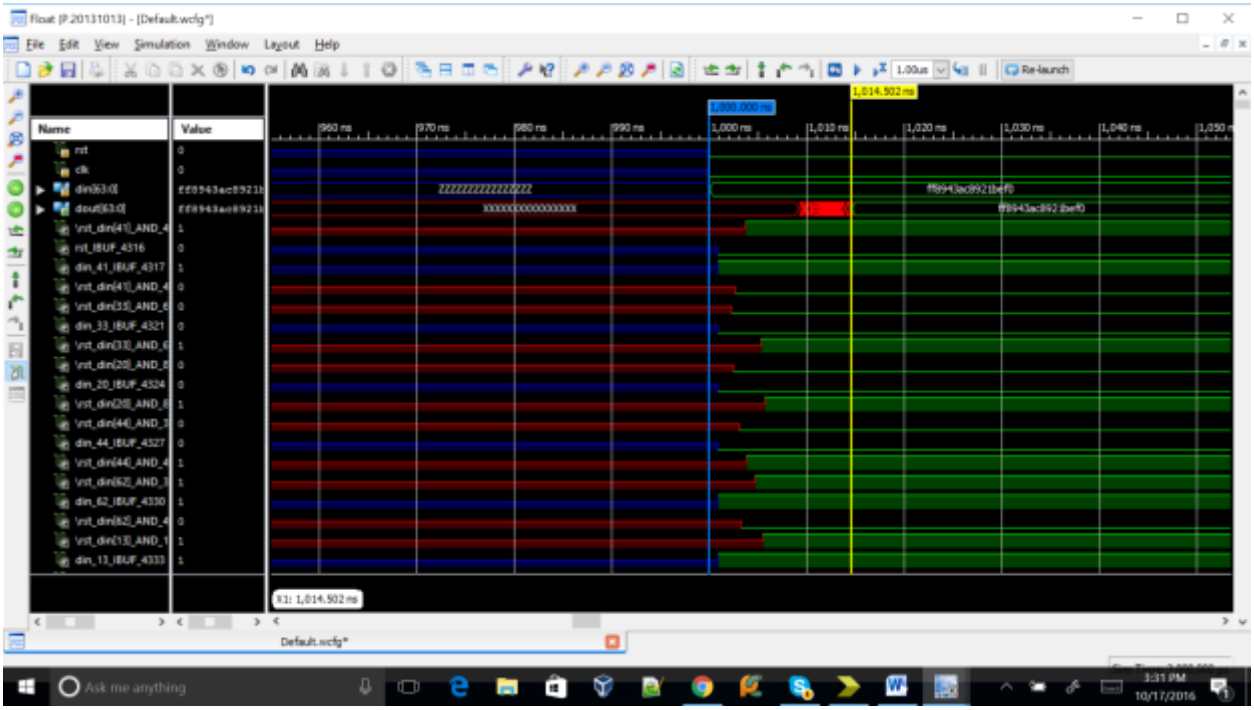


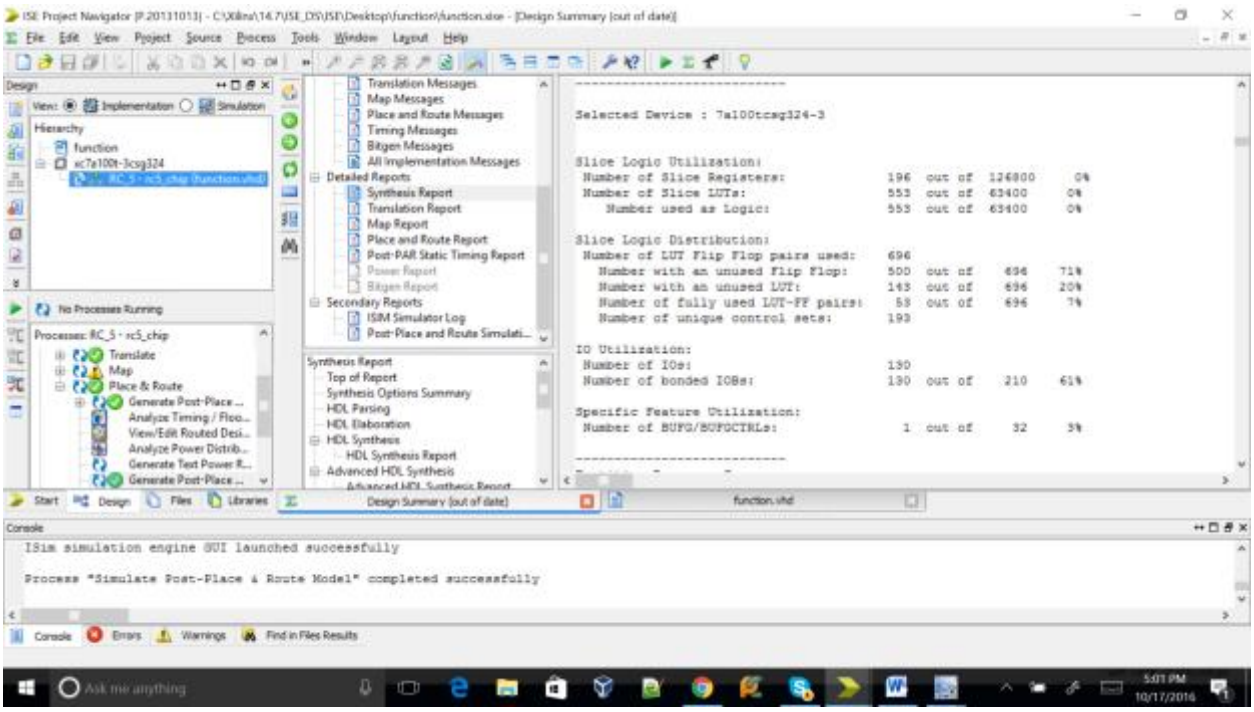
Lab 3
Pratik Thakker
Pat323





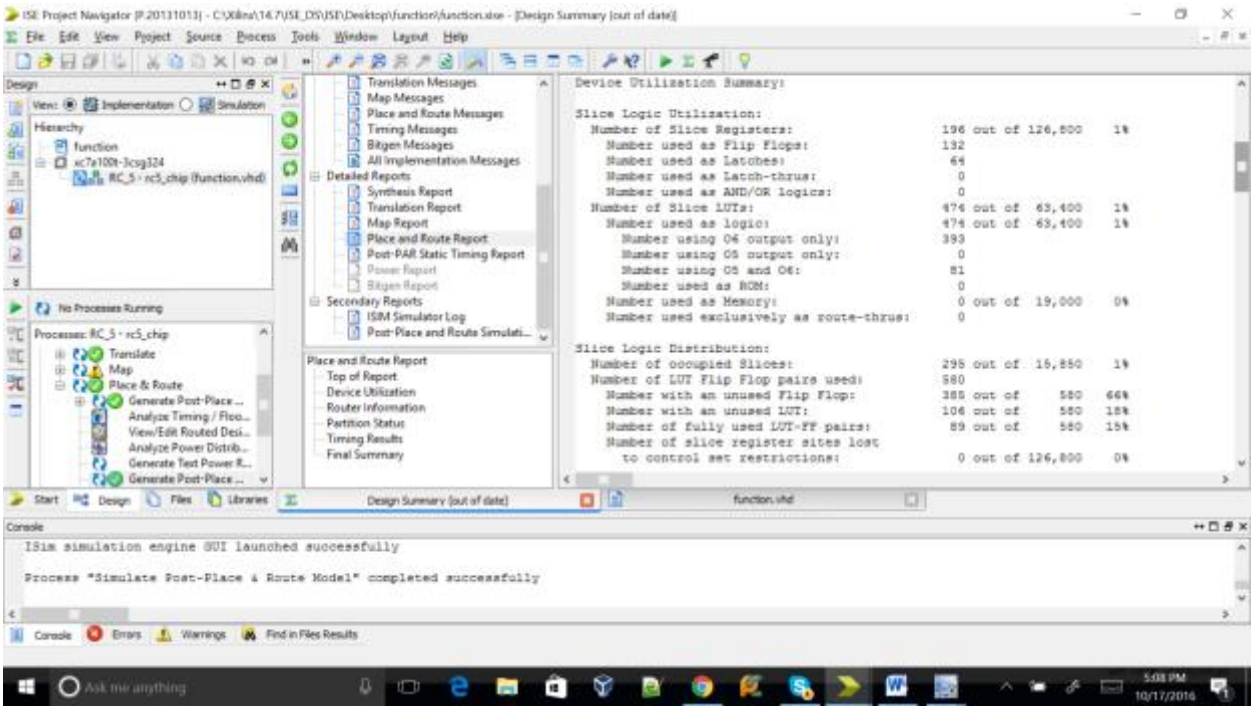
Lab 3
Pratik Thakker
Pat323





The device utilization in post place route phase is less as only required number of gates and circuit is used as compared to the synthesis report.

Lab 3
Pratik Thakker
Pat323



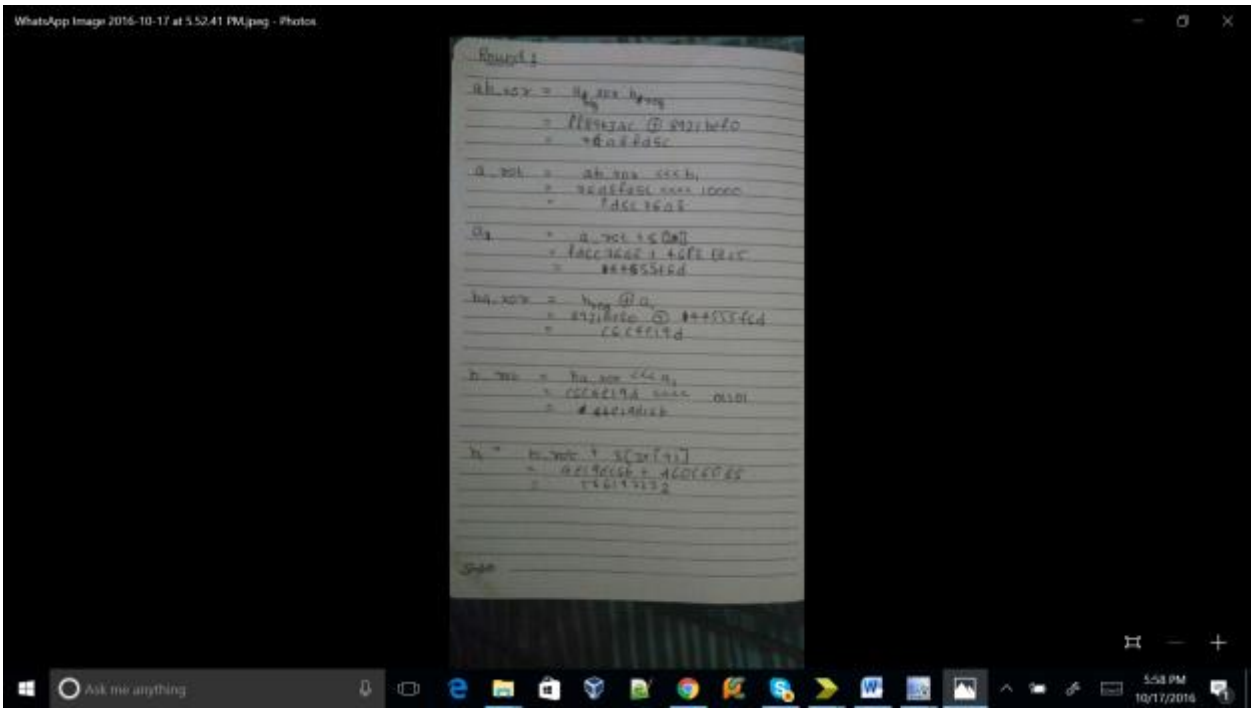
Total delay is 14.502 ns.

Latency is 13 clock cycles

Max clock frequency 127.087MHz

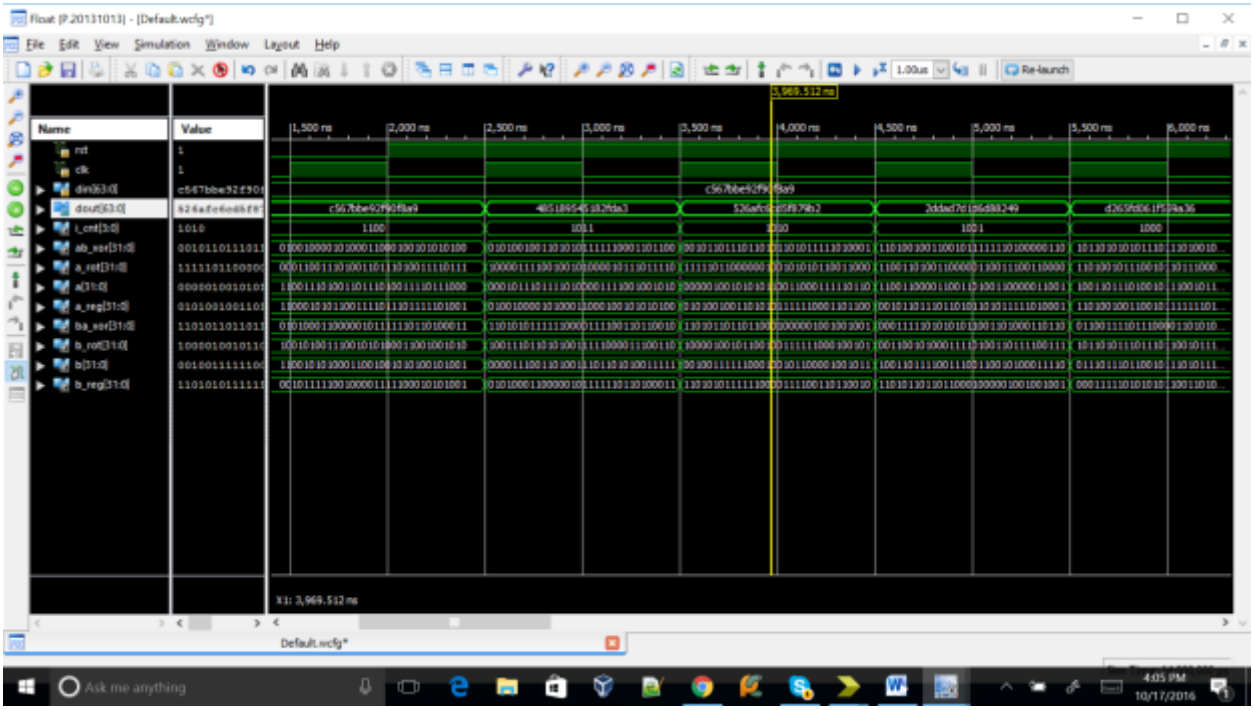
Critical path delay is 1.123 us

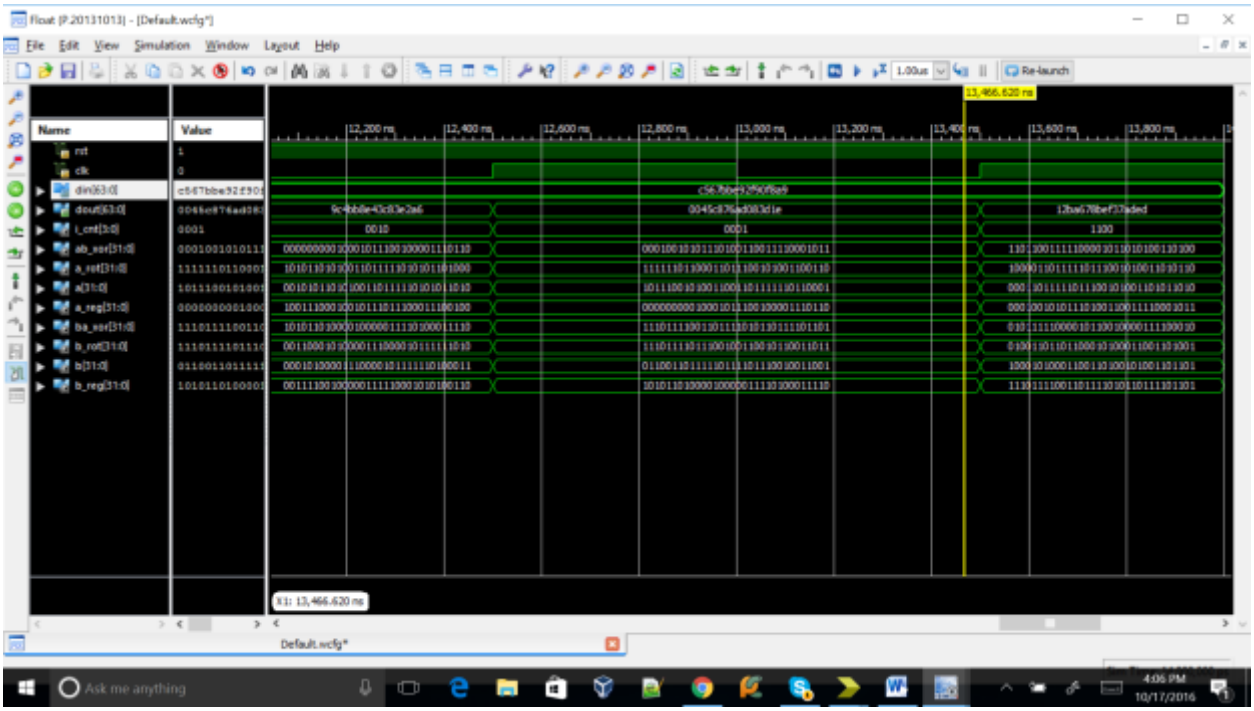
Lab 3
Pratik Thakker
Pat323



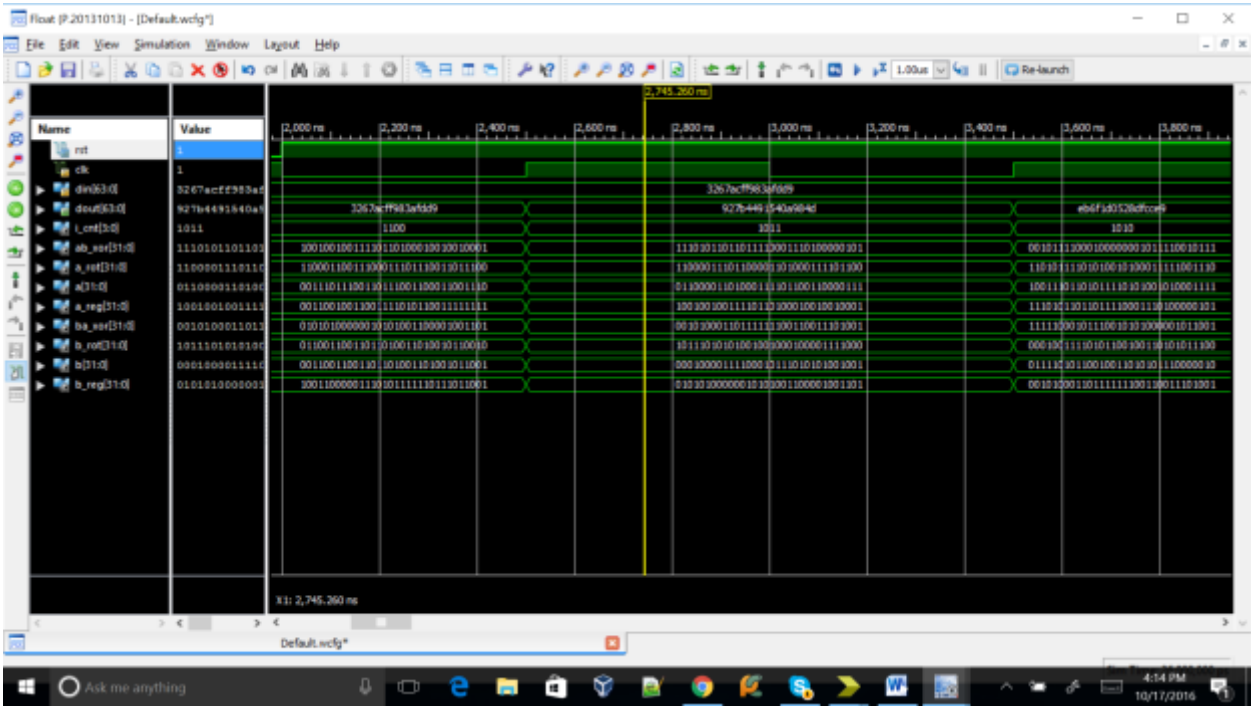
2 Inverse

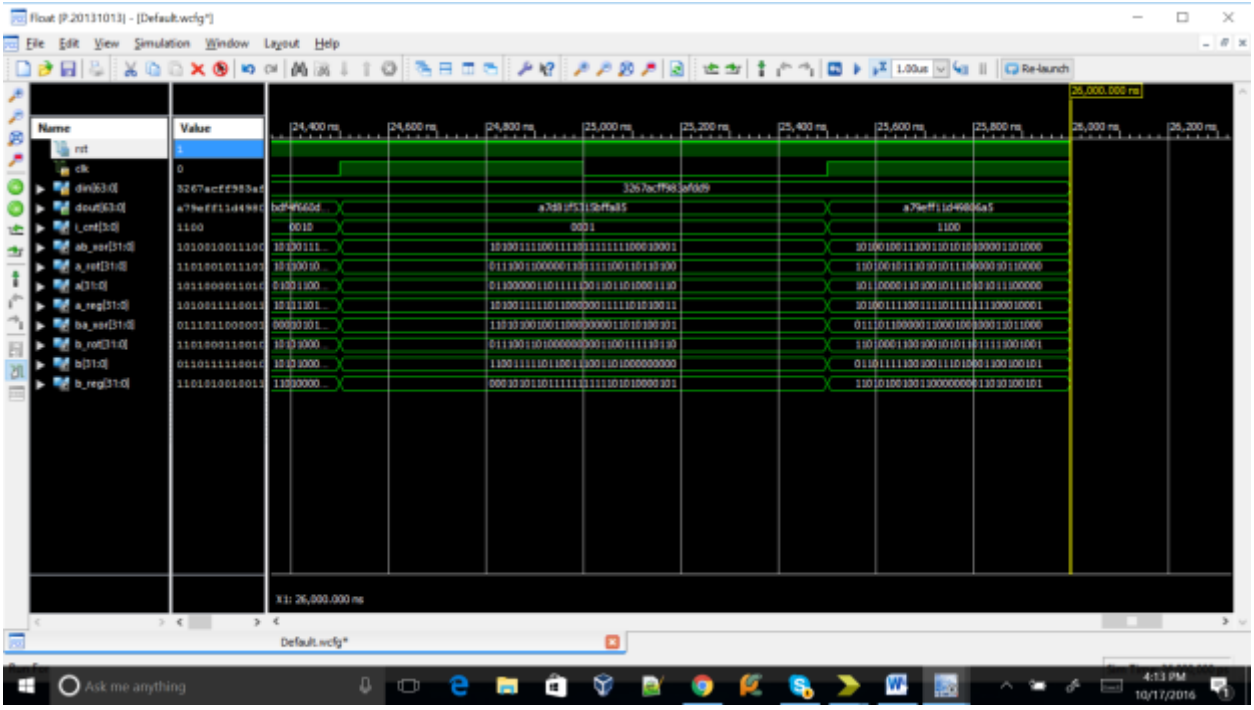
Lab 3
Pratik Thakker
Pat323



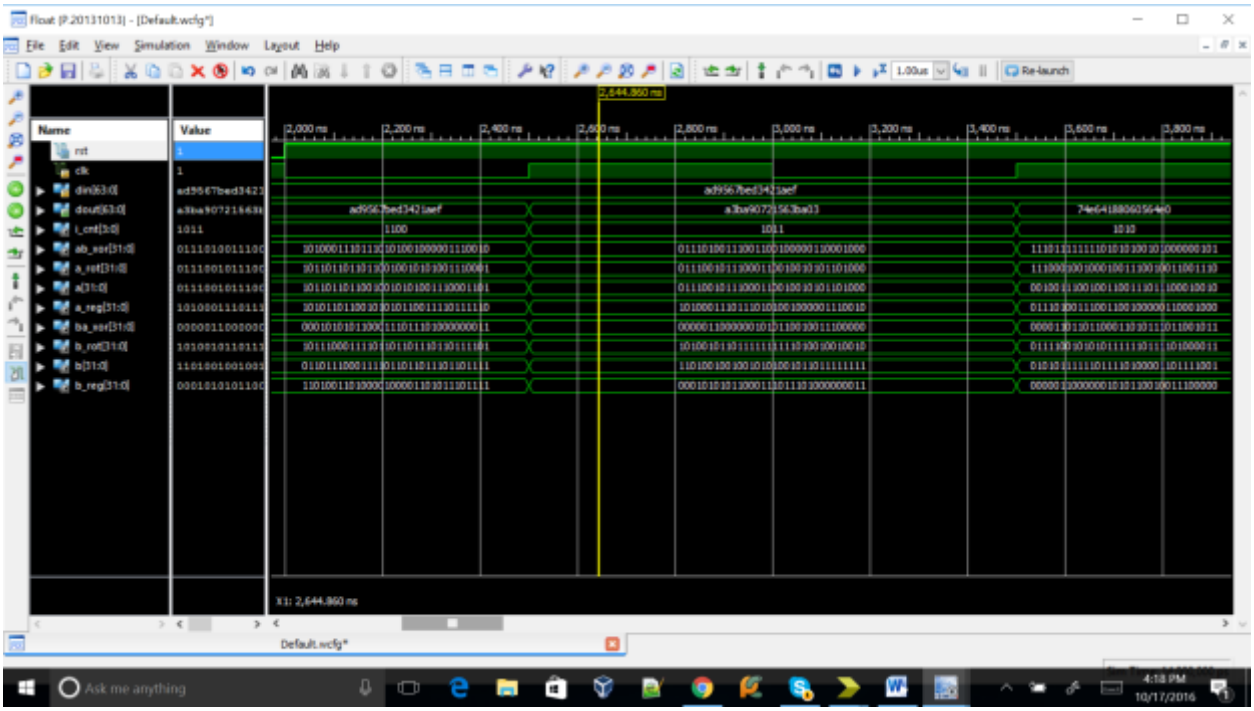


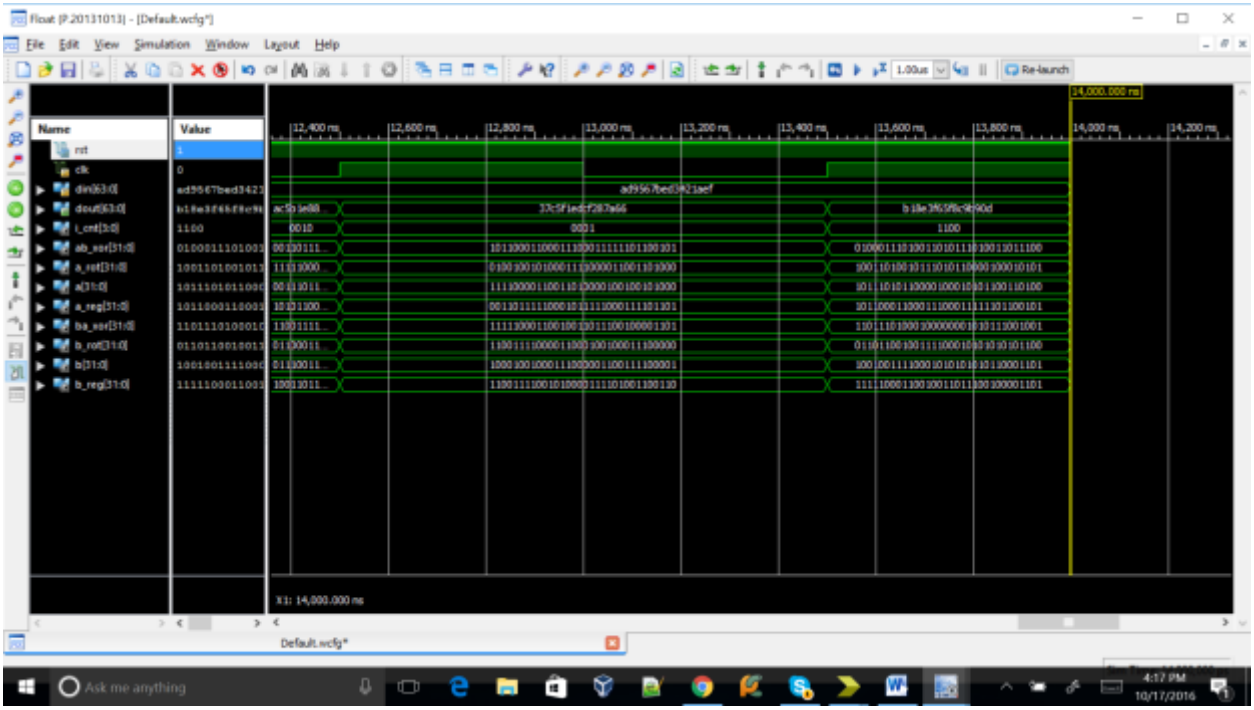
Lab 3
Pratik Thakker
Pat323



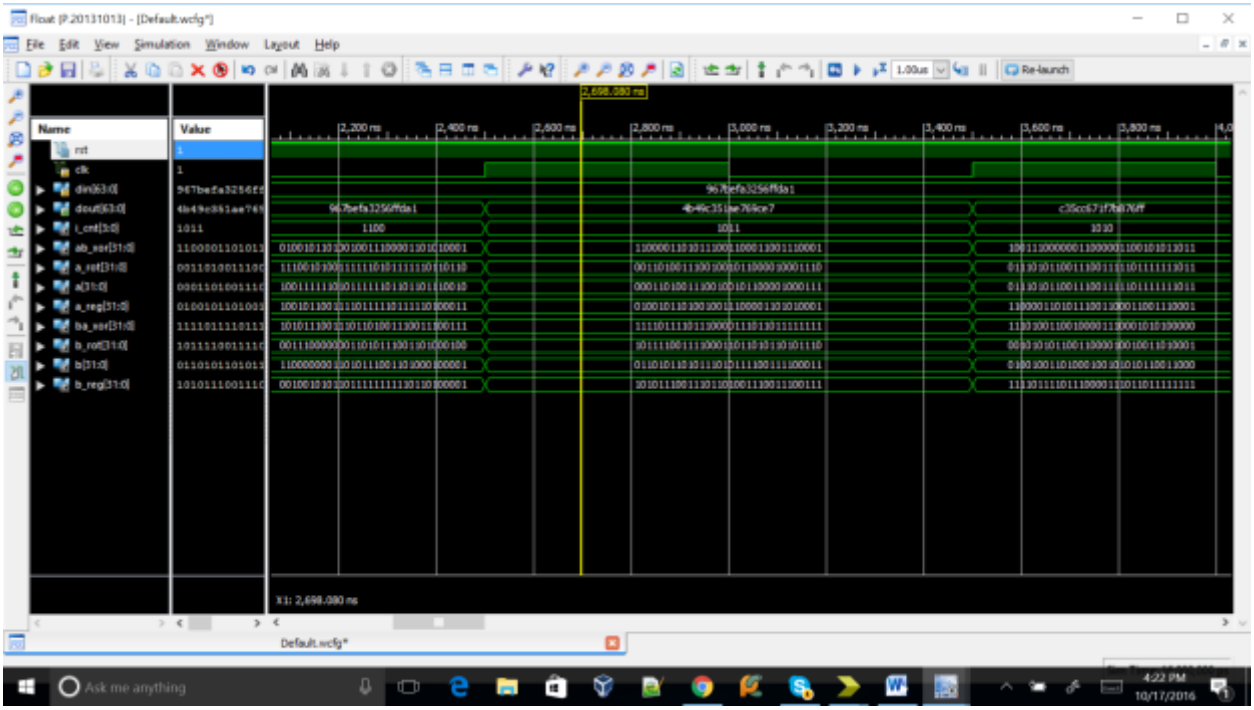


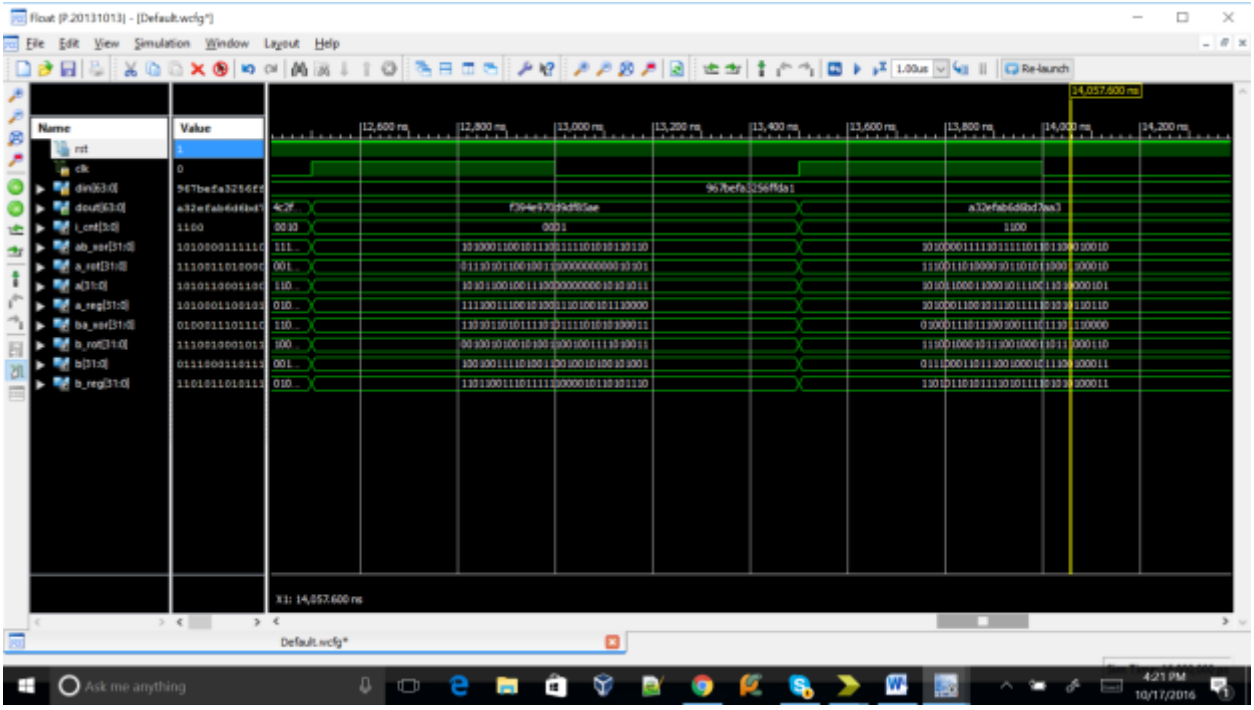
Lab 3
Pratik Thakker
Pat323



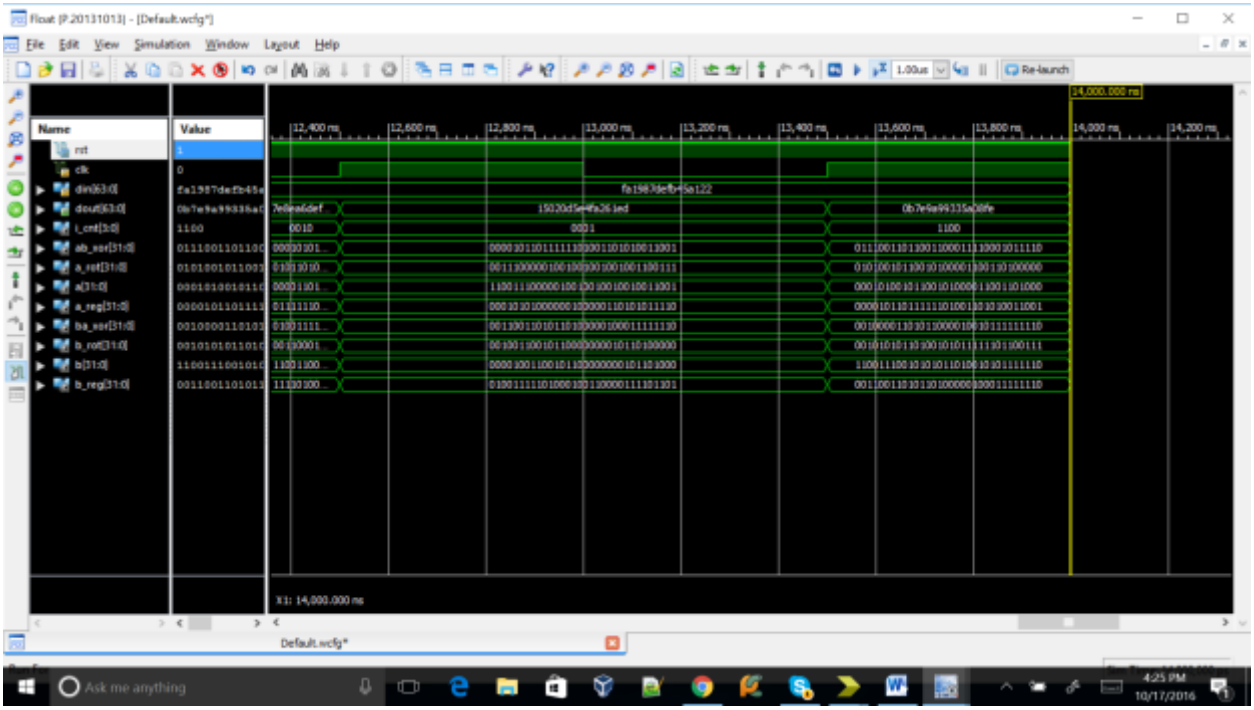


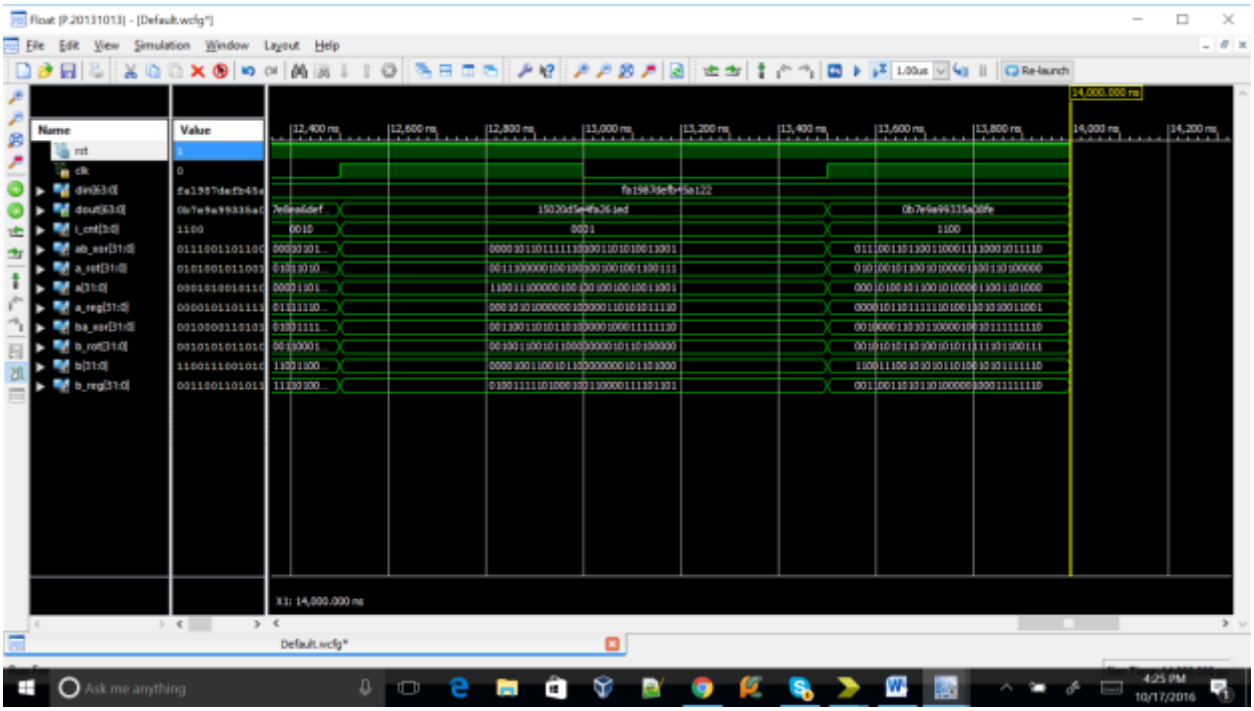
Lab 3
Pratik Thakker
Pat323



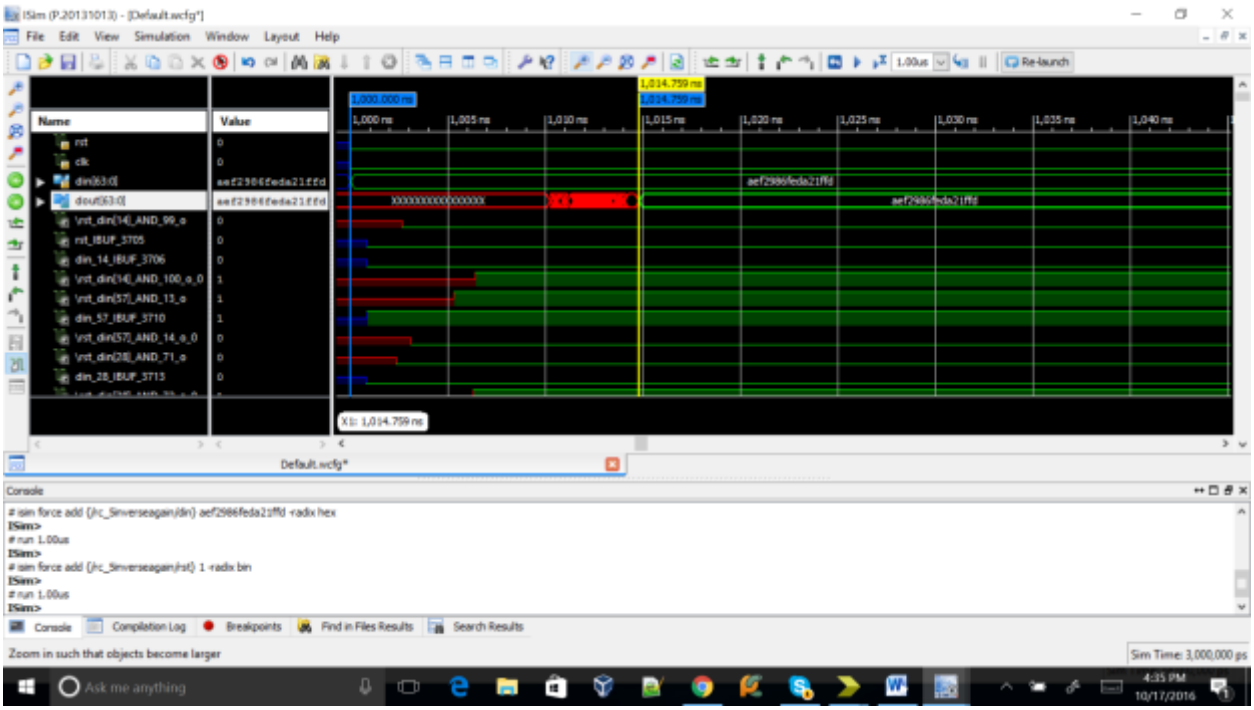


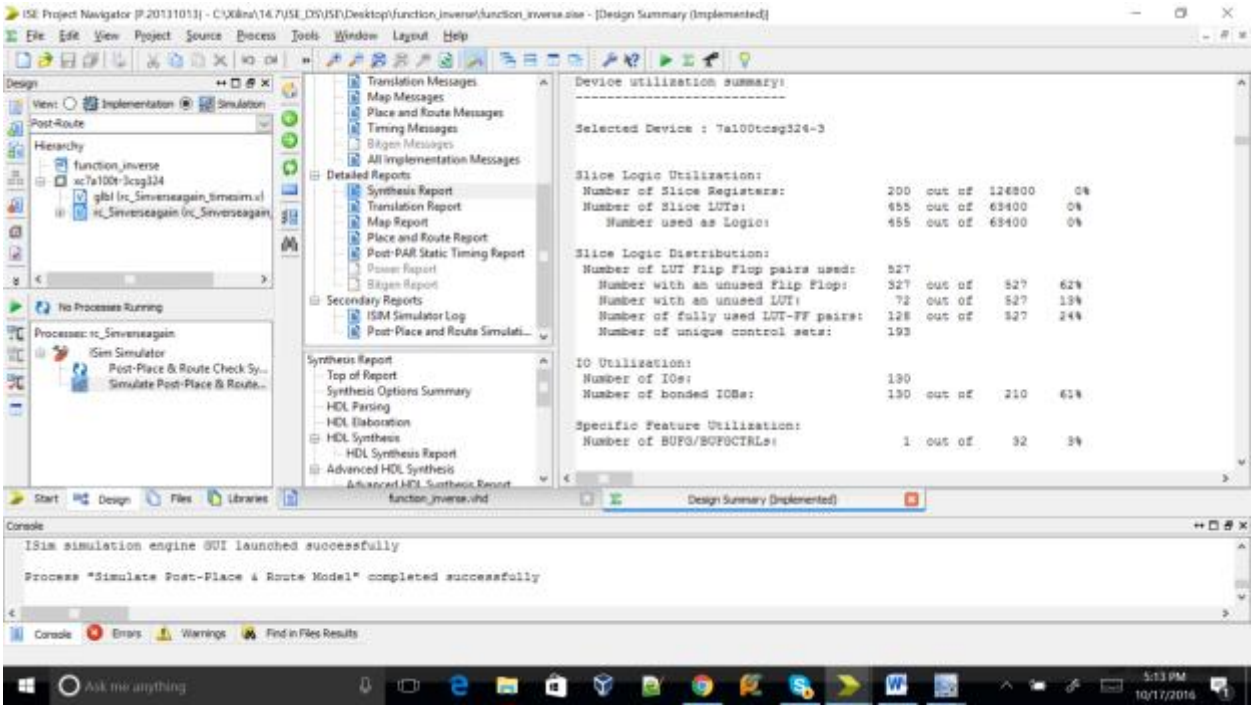
Lab 3
Pratik Thakker
Pat323





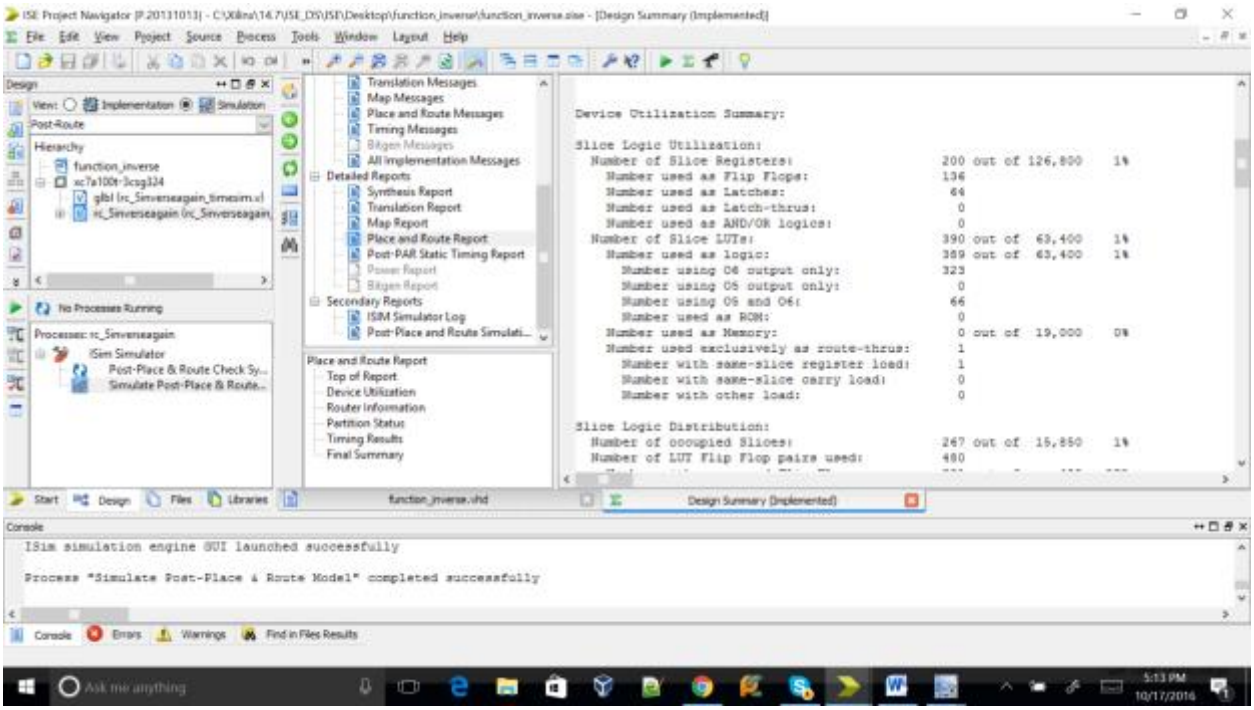
Lab 3
Pratik Thakker
Pat323





The device utilization in post place route phase is less as only required number of gates and circuit is used as compared to the synthesis report.

Lab 3
Pratik Thakker
Pat323



Total delay is 14.759 ns.

Latency is 13 clock cycles

Max clock frequency 172.454 MHz

Critical path delay is 1.241 us

https://youtu.be/-tOYTFvQCXk