

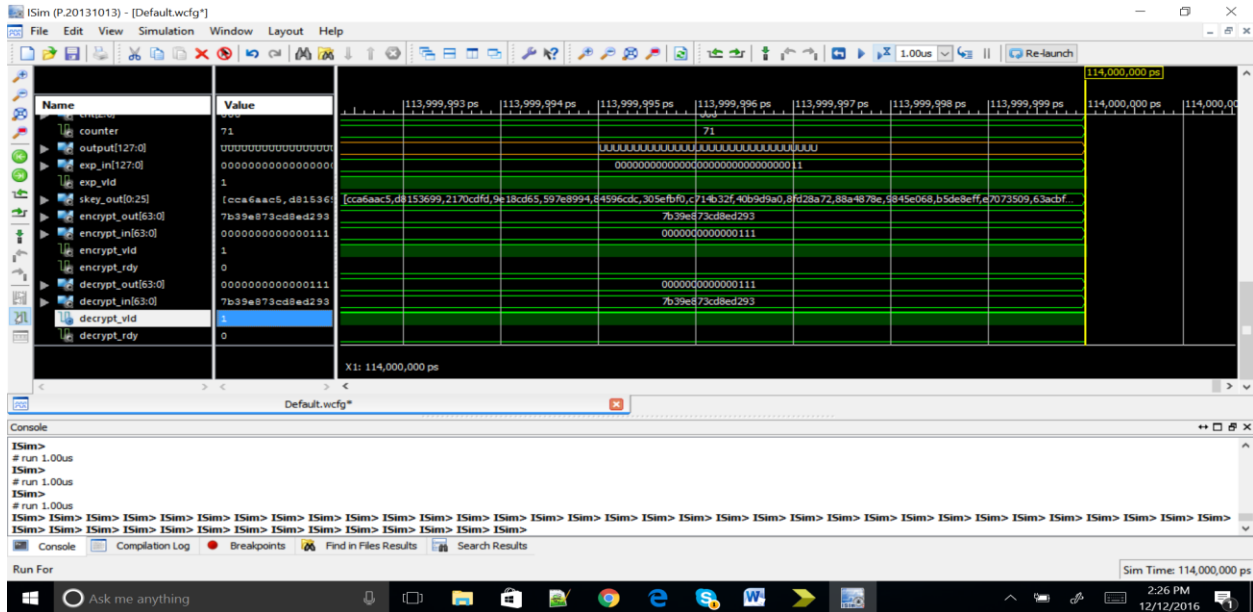
Pratik Thakker
Pat323Pratik Thakker
Pat323

Functional Simulation:

Test Case:

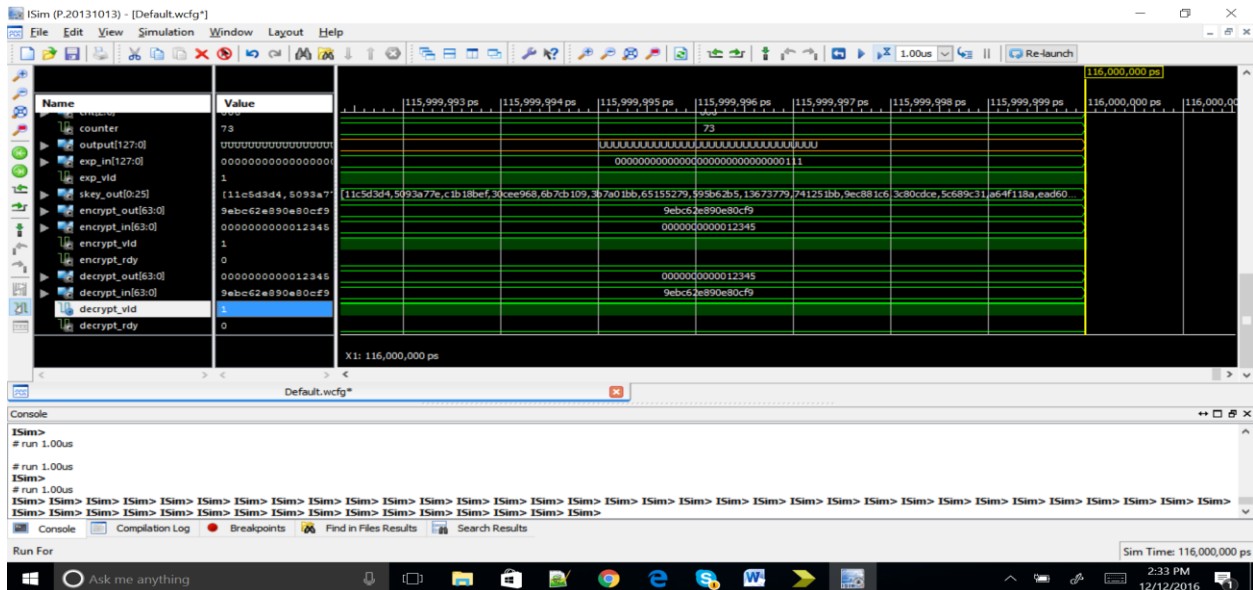
Input: 0000000000000000000000000000000011

Encryption Input: 00000000000000111



Input: 00000000000000000000000000000000111

Encryption Input: 0000000000012345



Lab 7

Pratik Thakker
Pat323

Resource Utilization:

ISE Project Navigator (P.20131013) - C:\Xilinx\14.7\ISE_DS\ISE\Desktop\test_lab7\test_lab7.xise - [Design Summary (Implemented)]

File Edit View Project Source Process Tools Window Layout Help

Design View: Implementation Simulation

Post-Route Hierarchy

- test_lab7
 - xc7a100t-3csg324
 - gbl (rc5_timesim.v)
 - rc5 (rc5_timesim.v)

Processes: rc5

No Processes Running

ISim Simulator

Post-Place & Route Check Sy...
Simulate Post-Place & Route...

Detailed Reports

- Place and Route Messages
- Timing Messages
- Bitgen Messages
- All Implementation Messages
- Synthesis Report
- Translation Report
- Map Report
- Place and Route Report
- Post-PAR Static Timing Report
- Power Report
- Bitgen Report

Secondary Reports

- ISIM Simulator Log
- Post-Place and Route Simulati...
- WebTalk Report
- WebTalk Log File

Synthesis Report

- Top of Report
- Synthesis Options Summary
- HDL Parsing
- HDL Elaboration
- HDL Synthesis
- HDL Synthesis Report
- Advanced HDL Synthesis
- Advanced HDL Synthesis Report

rc5.vhd

Design Summary (Implemented)

Device utilization summary:

Selected Device : 7a100tcsg324-3

Slice Logic Utilization:

Metric	Value	Out of	Percentage
Number of Slice Registers:	2691	126800	2%
Number of Slice LUTs:	2672	63400	4%
Number used as Logic:	2672	63400	4%

Slice Logic Distribution:

Metric	Value	Out of	Percentage
Number of LUT Flip Flop pairs used:	4816	4816	100%
Number with an unused Flip Flop:	2125	4816	44%
Number with an unused LUT:	2144	4816	44%
Number of fully used LUT-FF pairs:	547	4816	11%
Number of unique control sets:	62		

IO Utilization:

Metric	Value	Out of	Percentage
Number of IOs:	53		
Number of bonded IOBs:	53	210	25%

Specific Feature Utilization:

Metric	Value	Out of	Percentage
Number of BUFG/BUFGCTRLs:	1	32	3%

Console

ISim simulation engine GUI launched successfully

Process "Simulate Post-Place & Route Model" completed successfully

Ask me anything

2:45 PM 12/12/2016

ISE Project Navigator (P.20131013) - C:\Xilinx\14.7\ISE_DS\ISE\Desktop\test_lab7\test_lab7.xise - [Design Summary (Implemented)]

File Edit View Project Source Process Tools Window Layout Help

Design View: Implementation Simulation

Post-Route Hierarchy

- test_lab7
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 - rc5 (rc5_timesim.v)

Processes: rc5

No Processes Running

ISim Simulator

Post-Place & Route Check Sy...
Simulate Post-Place & Route...

Detailed Reports

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Secondary Reports

- ISIM Simulator Log
- Post-Place and Route Simulati...
- WebTalk Report
- WebTalk Log File

Place and Route Report

- Top of Report
- Device Utilization
- Router Information
- Partition Status
- Timing Results
- Final Summary

rc5.vhd

Design Summary (Implemented)

Device Utilization Summary:

Slice Logic Utilization:

Metric	Value	Out of	Percentage
Number of Slice Registers:	2,720	126,800	2%
Number used as Flip Flops:	2,691		
Number used as Latches:	0		
Number used as Latch-thrus:	0		
Number used as AND/OR logics:	29		
Number of Slice LUTs:	2,512	63,400	3%
Number used as logic:	2,318	63,400	3%
Number using O6 output only:	1,950		
Number using O5 output only:	15		
Number using O5 and O6:	353		
Number used as ROM:	0		
Number used as Memory:	0	19,000	0%
Number used exclusively as route-thrus:	194		
Number with same-slice register load:	193		
Number with same-slice carry load:	1		
Number with other load:	0		

Slice Logic Distribution:

Metric	Value	Out of	Percentage
Number of occupied Slices:	1,257	15,850	7%
Number of LUT Flip Flop pairs used:	3,960		
Number with an unused Flip Flop:	1,475	3,960	37%
Number with an unused LUT:	1,448	3,960	36%

Console

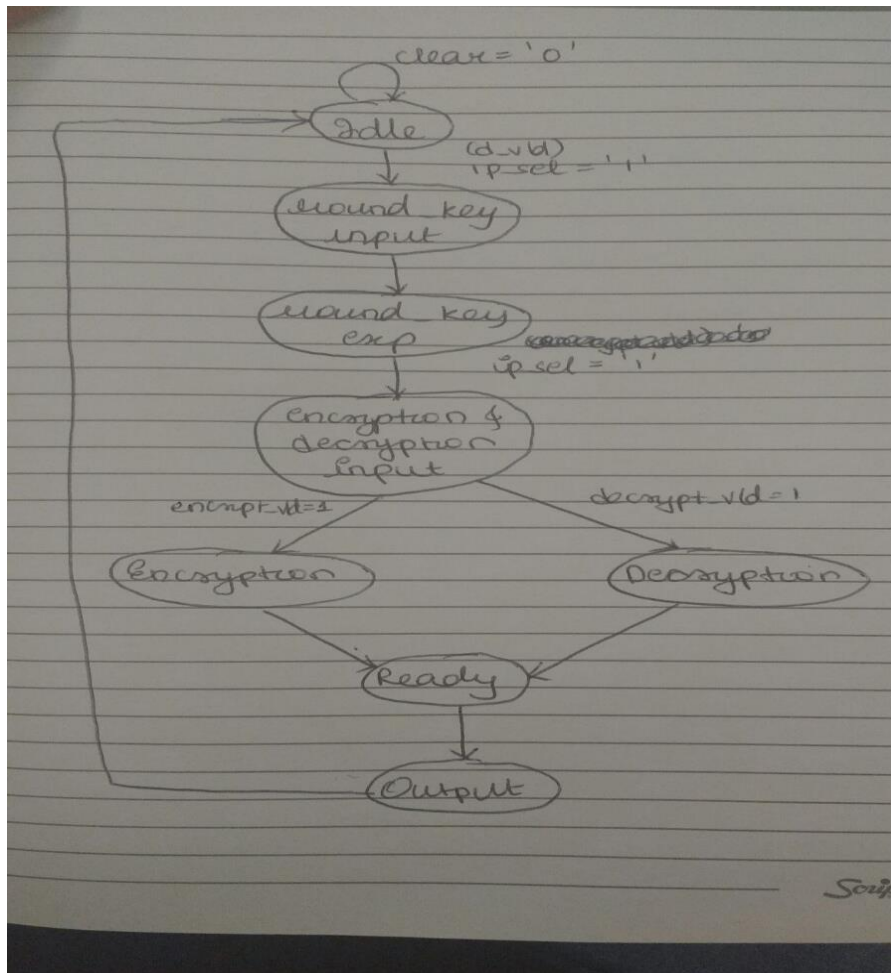
ISim simulation engine GUI launched successfully

Process "Simulate Post-Place & Route Model" completed successfully

Ask me anything

2:46 PM 12/12/2016

FSM:



Methodology:

Press the CPU reset button to clear

Switch 15 – 8 are used as input and Switch 7-4 are used to select the position of input.

For ex if switch 7-4 are 0000 then the input is 1st 8 bits i.e. from LSB to MSB.

Give input that you want and then press BTNC to validate.

Now turn switch 0 to high this will give your input to encryption and then press BTNC this will encrypt the input.

Now press BTNR to see the encrypted output.

Now turn switch 1 to high this will give the encrypted output as input to decryption module.

Once the input is given press BTNC for decryption.

Now press BTNR to see the decrypted output. Which will be same as input given for encryption.

Critical Path Delay is 9.13 ns

The design can run at 109.53 Mhz

Propagation Delay of the design is 976.91 ns

Youtube Link :

<https://youtu.be/CvRUkeAypIA>