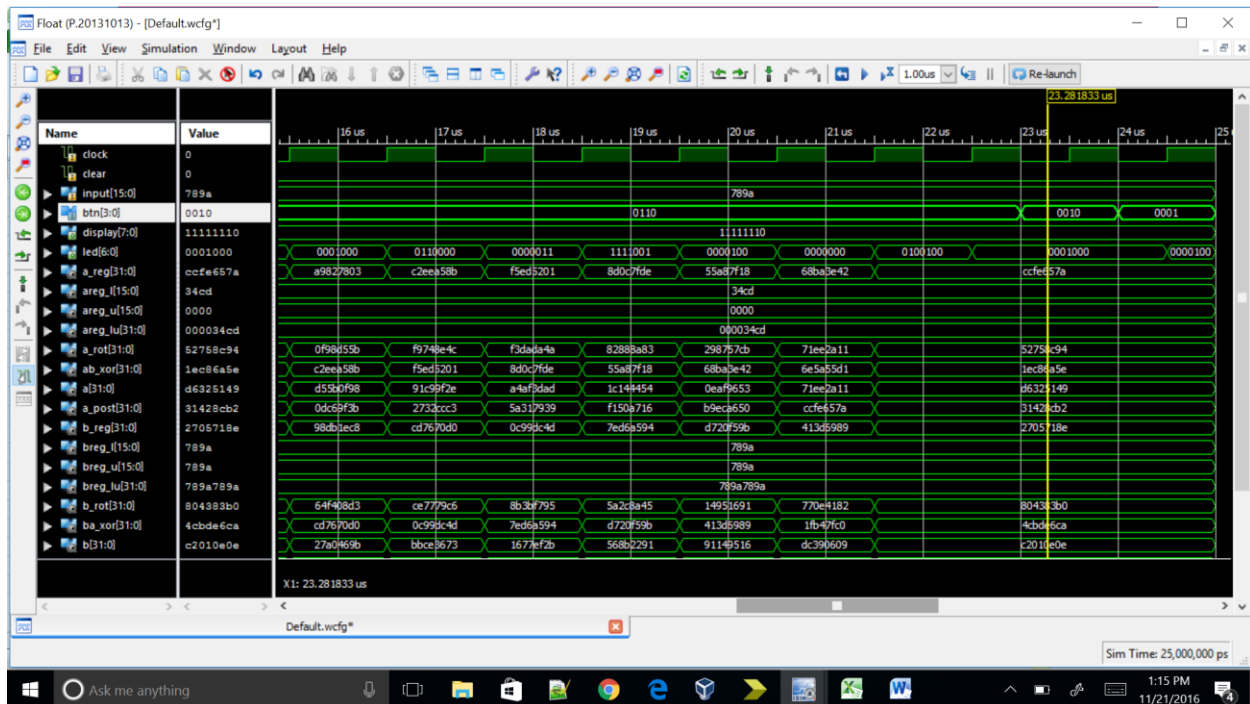
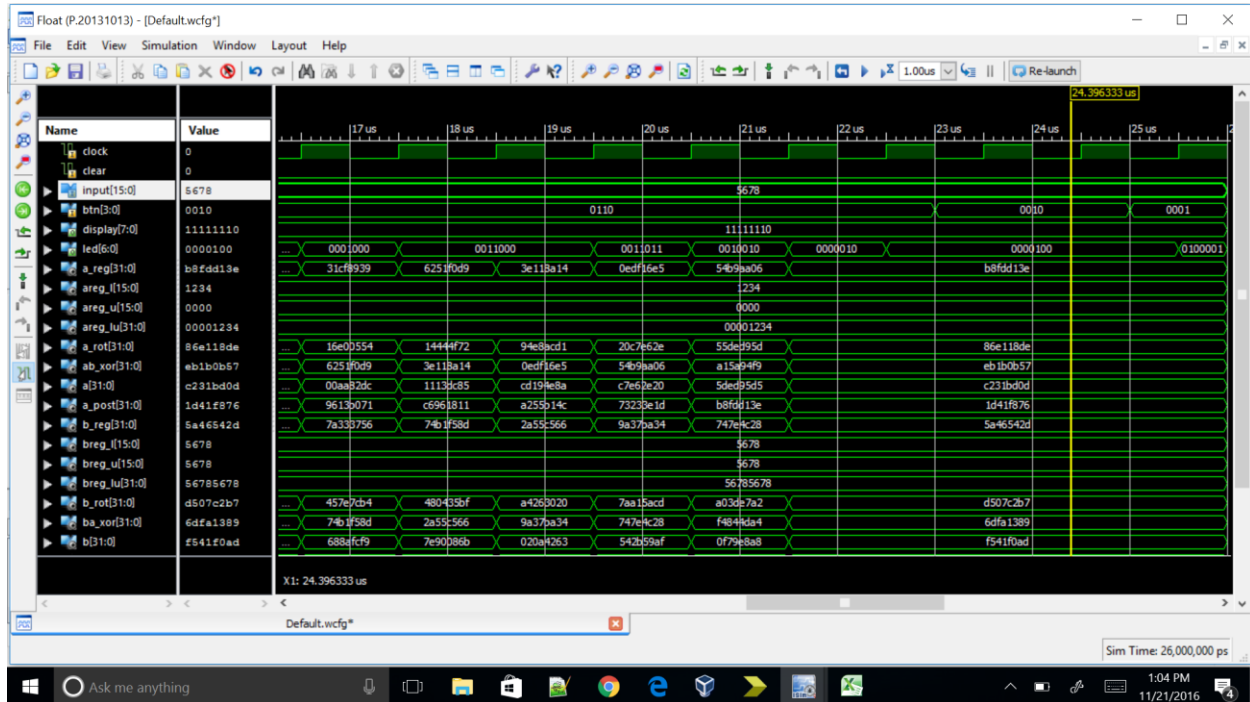


Lab 6

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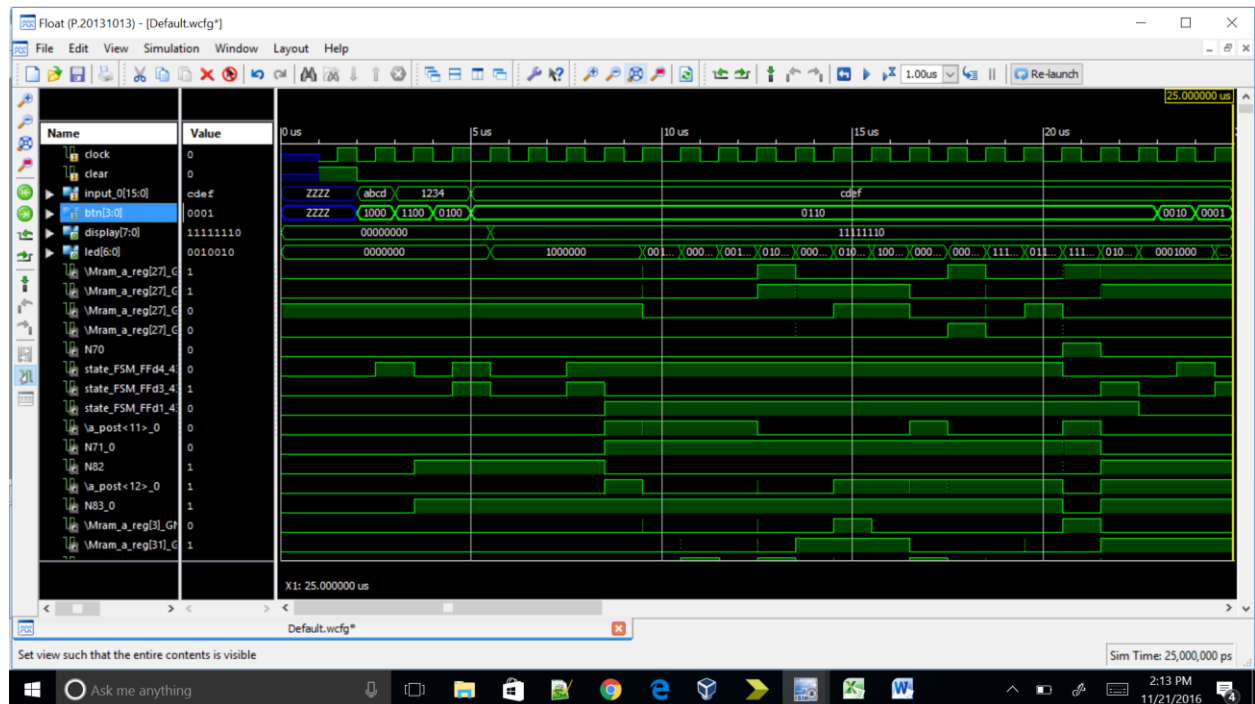


Lab 6

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Microsoft Excel (Product Activation Failed)

	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S
1		Round 1	Round 2	Round 3															
2	a_rot	61267fc0	2d3277d9	3ef99003															
3	ab_xor	5e09e2e3	8cb95a79	08c6d683															
4	a	0933fe03	2d3277d9	3ef99003															
5	b_rot	3f2f8f17	ff82cf43	ba861cf9															
6	ba_xor	3f2f9d23	a18b2da0	363f4680															
7	b	f173f2f8	fc167a1f	f3750c39															
8																			
9																			
10		Round 1	Round 2	Round 3															
11	a_rot	49a104e0	69064ec2	b017fe3c															
12	ab_xor	e171ac9d	a5cb994	6382c643															
13	a	0934209c	b09a4193	580bff1e															
14	b_rot	a8d09cb0	2dbc2bcb	765ef1eb															
15	ba_xor	a8d0a87d	cccd8756	d395387f															
16	b	1396151a	65b73579	1eb765ef															
17																			
18																			
19																			
20																			
21																			
22																			
23																			
24																			



Critical path delay is 5.71 ns

Latency is 21

Propagation delay is 119.91 ns

Lab 6

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The screenshot shows the Xilinx ISE Project Navigator interface. The 'Design Summary' report is open, displaying the following information:

Clock Information:

Clock Signal	Clock buffer (FF name)	Load
clock	BUFGP	191

Asynchronous Control Signals Information:
No asynchronous control signals found in this design

Timing Summary:
Speed Grade: -3

Minimum period: 5.710ns (Maximum Frequency: 175.126MHz)
Minimum input arrival time before clock: 1.482ns
Maximum output required time after clock: 0.640ns
Maximum combinational path delay: No path found

Timing Details:
All values displayed in nanoseconds (ns)

The console window shows the following messages:

```
ISim simulation engine GUI launched successfully
Process "Simulate Post-Place & Route Model" completed successfully
```

Max frequency 175.126 Mhz

The screenshot shows the Xilinx ISE Project Navigator interface. The 'Device Utilization summary' report is open, displaying the following information:

Device utilization summary:

Selected Device : 7a100tcsg324-3

Slice Logic Utilization:

Metric	Value	Out of	Percentage
Number of Slice Registers:	191	126800	0%
Number of Slice LUTs:	667	63400	1%
Number used as Logic:	667	63400	1%

Slice Logic Distribution:

Metric	Value	Out of	Percentage
Number of LUT Flip Flop pairs used:	732		
Number with an unused Flip Flop:	541	732	73%
Number with an unused LUT:	65	732	8%
Number of fully used LUT-FF pairs:	126	732	17%
Number of unique control sets:	9		

IO Utilization:

Metric	Value	Out of	Percentage
Number of IOs:	37		
Number of bonded IOBs:	37	210	17%

Specific Feature Utilization:

Metric	Value	Out of	Percentage
Number of BUFG/BUFGCTRLs:	1	32	3%

The console window shows the following messages:

```
ISim simulation engine GUI launched successfully
Process "Simulate Post-Place & Route Model" completed successfully
```

Lab 6

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ISE Project Navigator (P.20131013) - C:\Xilinx\14.7\ISE_DS\ISE\Desktop\inverse_fpga\inverse_fpga.ise - [Design Summary (out of date)]

File Edit View Project Source Process Tools Window Layout Help

Design

View: Implementation Simulation

Post-Route

Hierarchy

- inverse_fpga
 - xc7a100t-3csg324
 - gbl (inverse_fpga_timesim.v)
 - inverse_fpga (inverse_fpga_timesim.v)

No Processes Running

Processes: inverse_fpga

- ISim Simulator
 - Post-Place & Route Check Sy...
 - Simulate Post-Place & Route...

Translation Messages

- Map Messages
- Place and Route Messages
- Timing Messages
- Bitgen Messages
- All Implementation Messages

Detailed Reports

- Synthesis Report
- Translation Report
- Map Report
- Place and Route Report
- Post-PAR Static Timing Report
- Power Report
- Bitgen Report

Secondary Reports

- ISIM Simulator Log
- Post-Place and Route Simulati...

Place and Route Report

- Top of Report
- Device Utilization
- Router Information
- Partition Status
- Timing Results
- Final Summary

Device Utilization Summary:

Slice Logic Utilization:

Number of Slice Registers:	191 out of 126,800	1%
Number used as Flip Flops:	191	
Number used as Latches:	0	
Number used as Latch-thrus:	0	
Number used as AND/OR logics:	0	
Number of Slice LUTs:	548 out of 63,400	1%
Number used as logic:	546 out of 63,400	1%
Number using O6 output only:	333	
Number using O5 output only:	69	
Number using O5 and O6:	144	
Number used as ROM:	0	
Number used as Memory:	0 out of 19,000	0%
Number used exclusively as route-thrus:	2	
Number with same-slice register load:	0	
Number with same-slice carry load:	2	
Number with other load:	0	

Slice Logic Distribution:

Number of occupied Slices:	187 out of 15,850	1%
Number of LUT Flip Flop pairs used:	615	
Number with an unused Flip Flop:	448 out of 615	72%
Number with an unused LUT:	67 out of 615	10%

Console

ISim simulation engine GUI launched successfully

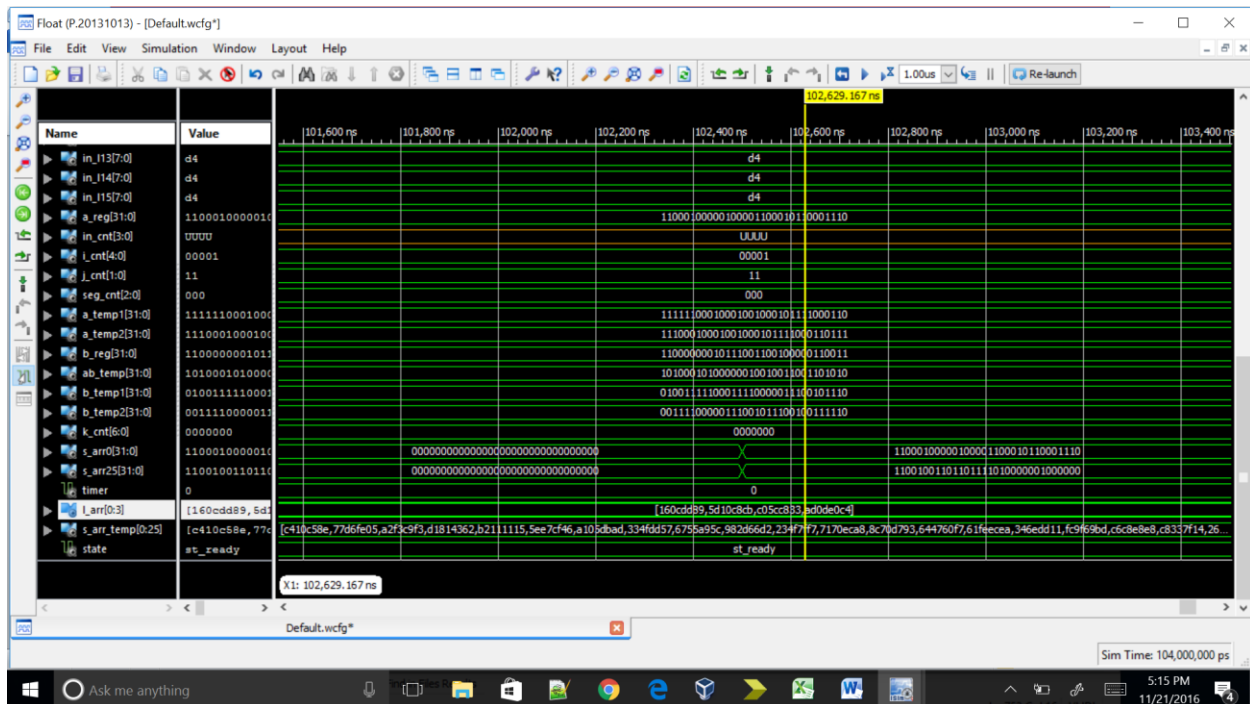
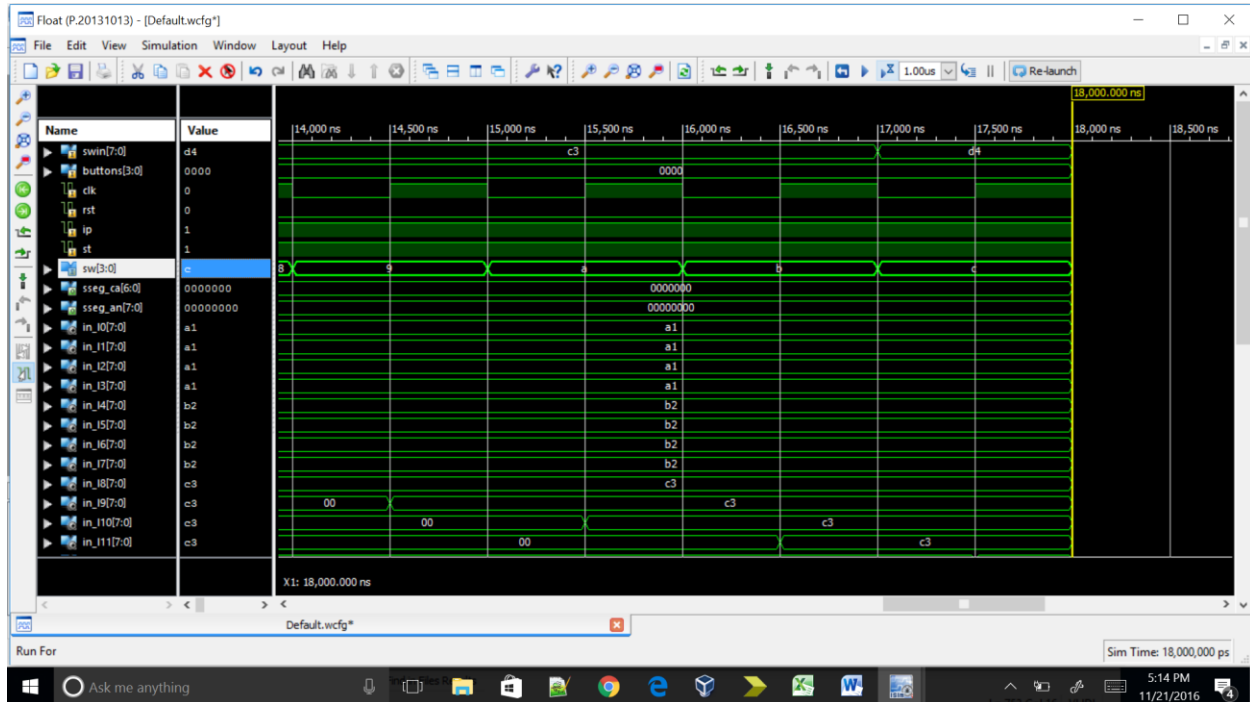
Process "Simulate Post-Place & Route Model" completed successfully

Console Errors Warnings Find in Files Results

Windows Taskbar: Ask me anything, 2:26 PM, 11/21/2016

Lab 6

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Lab 6

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ISE Project Navigator (P.20131013) - C:\Xilinx\14.7\ISE_DS\ISE\Desktop\exp\exp.xise - [Design Summary (Implemented)]

File Edit View Project Source Process Tools Window Layout Help

Design

View: ☐ Implementation ☒ Simulation

Hierarchy

- exp
 - xc7a100t-3csg324
 - lab6_Roundkey - Behavioral (exp.vhd)

Processes: lab6_Roundkey - Behavioral

- ISim Simulator
 - Behavioral Check Syntax
 - Simulate Behavioral Model

Parser Messages

- Synthesis Messages
- Translation Messages
- Map Messages
- Place and Route Messages
- Timing Messages
- Bitgen Messages
- All Implementation Messages

Detailed Reports

- Synthesis Report
- Translation Report
- Map Report
- Place and Route Report
- Post-PAR Static Timing Report
- Power Report
- Bitgen Report

Secondary Reports

- Synthesis Report
 - Top of Report
 - Synthesis Options Summary
 - HDL Parsing
 - HDL Elaboration
 - HDL Synthesis
 - HDL Synthesis Report
 - Advanced HDL Synthesis
 - Advanced HDL Synthesis Report

exp.vhd

Design Summary (Implemented)

Slice Logic Utilization:

Metric	Value	Out of	Percentage
Number of Slice Registers:	1285	126800	1%
Number of Slice LUTs:	1069	63400	1%
Number used as Logic:	1069	63400	1%

Slice Logic Distribution:

Metric	Value	Out of	Percentage
Number of LUT Flip Flop pairs used:	2071		
Number with an unused Flip Flop:	786	2071	37%
Number with an unused LUT:	1002	2071	48%
Number of fully used LUT-FF pairs:	283	2071	13%
Number of unique control sets:	52		

IO Utilization:

Metric	Value	Out of	Percentage
Number of IOs:	35		
Number of bonded IOBs:	35	210	16%

Specific Feature Utilization:

Metric	Value	Out of	Percentage
Number of BUFG/BUFGCTRLs:	1	32	3%

Partition Resource Summary:

Console

```
to the simulator, see your Simulator tool documentation.
Process "Generate Post-Place & Route Simulation Model" completed successfully
```

Ask me anything

5:16 PM 11/21/2016

ISE Project Navigator (P.20131013) - C:\Xilinx\14.7\ISE_DS\ISE\Desktop\exp\exp.xise - [Design Summary (Implemented)]

File Edit View Project Source Process Tools Window Layout Help

Design

View: ☐ Implementation ☒ Simulation

Hierarchy

- exp
 - xc7a100t-3csg324
 - lab6_Roundkey - Behavioral (exp.vhd)

Processes: lab6_Roundkey - Behavioral

- ISim Simulator
 - Behavioral Check Syntax
 - Simulate Behavioral Model

Parser Messages

- Synthesis Messages
- Translation Messages
- Map Messages
- Place and Route Messages
- Timing Messages
- Bitgen Messages
- All Implementation Messages

Detailed Reports

- Synthesis Report
- Translation Report
- Map Report
- Place and Route Report
- Post-PAR Static Timing Report
- Power Report
- Bitgen Report

Secondary Reports

- Place and Route Report
 - Top of Report
 - Device Utilization
 - Router Information
 - Partition Status
 - Timing Results
 - Final Summary

exp.vhd

Design Summary (Implemented)

Device Utilization Summary:

Slice Logic Utilization:

Metric	Value	Out of	Percentage
Number of Slice Registers:	1,314	126,800	1%
Number used as Flip Flops:	1,285		
Number used as Latches:	0		
Number used as Latch-thrus:	0		
Number used as AND/OR logics:	29		
Number of Slice LUTs:	985	63,400	1%
Number used as logic:	963	63,400	1%
Number using O6 output only:	826		
Number using O5 output only:	30		
Number using O5 and O6:	107		
Number used as ROM:	0		
Number used as Memory:	0	19,000	0%
Number used exclusively as route-thrus:	22		
Number with same-slice register load:	21		
Number with same-slice carry load:	1		
Number with other load:	0		

Slice Logic Distribution:

Metric	Value	Out of	Percentage
Number of occupied Slices:	531	15,850	3%
Number of LUT Flip Flop pairs used:	1,790		
Number with an unused Flip Flop:	514	1,790	28%

Console

```
to the simulator, see your Simulator tool documentation.
Process "Generate Post-Place & Route Simulation Model" completed successfully
```

Ask me anything

5:20 PM 11/21/2016

Critical path delay 9.126 ns

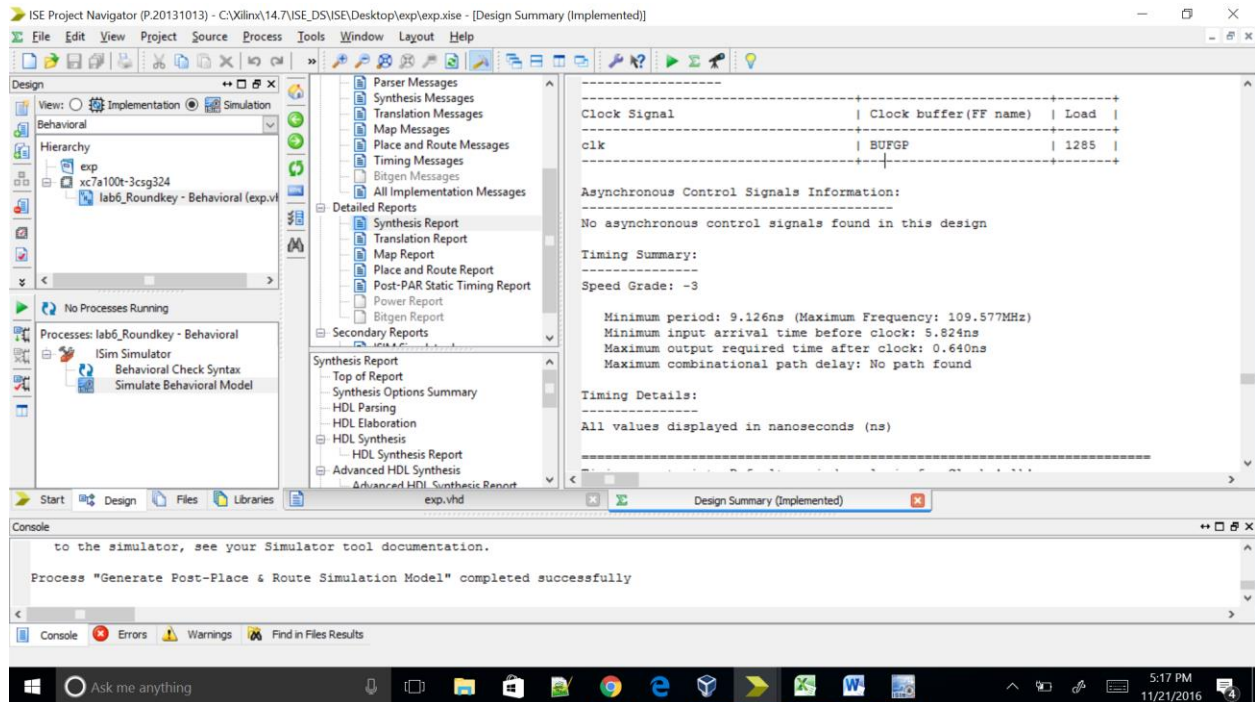
Latency is 98

Propagation delay is 894.348 ns

Lab 6

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Pat323



Max Frequency is 109.577 Mhz

You tube link

https://youtu.be/OeFsQmQq_6E