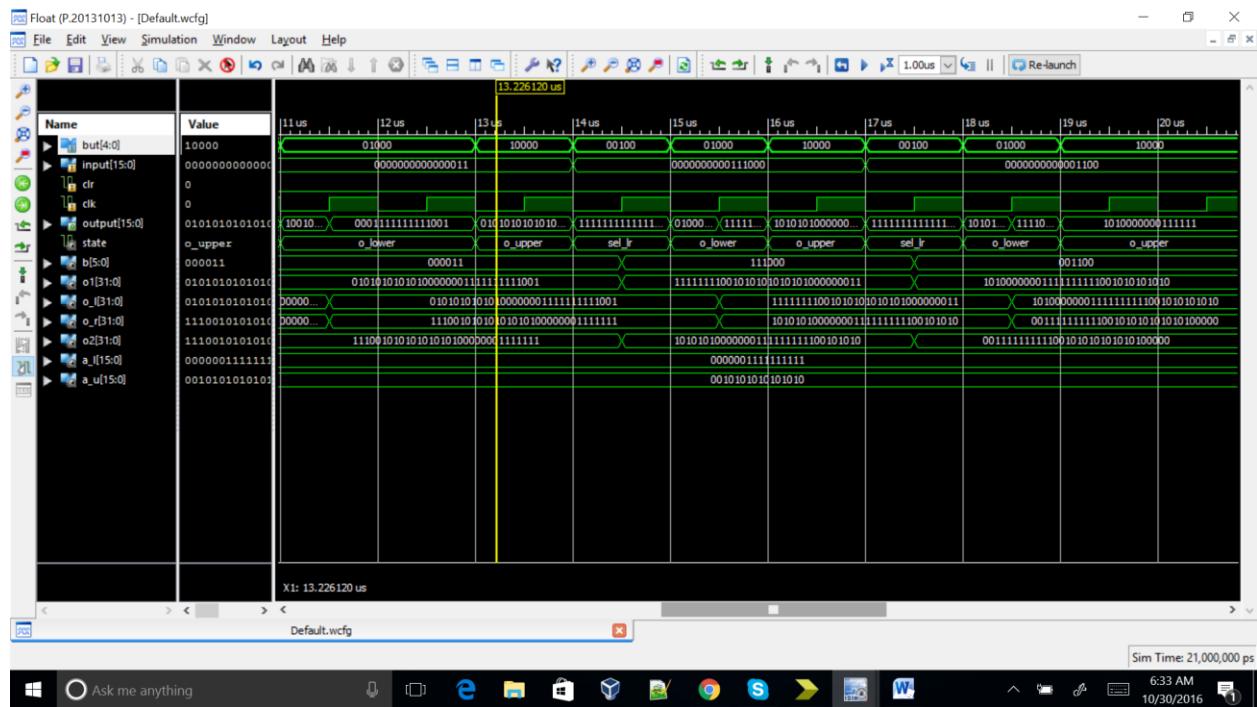
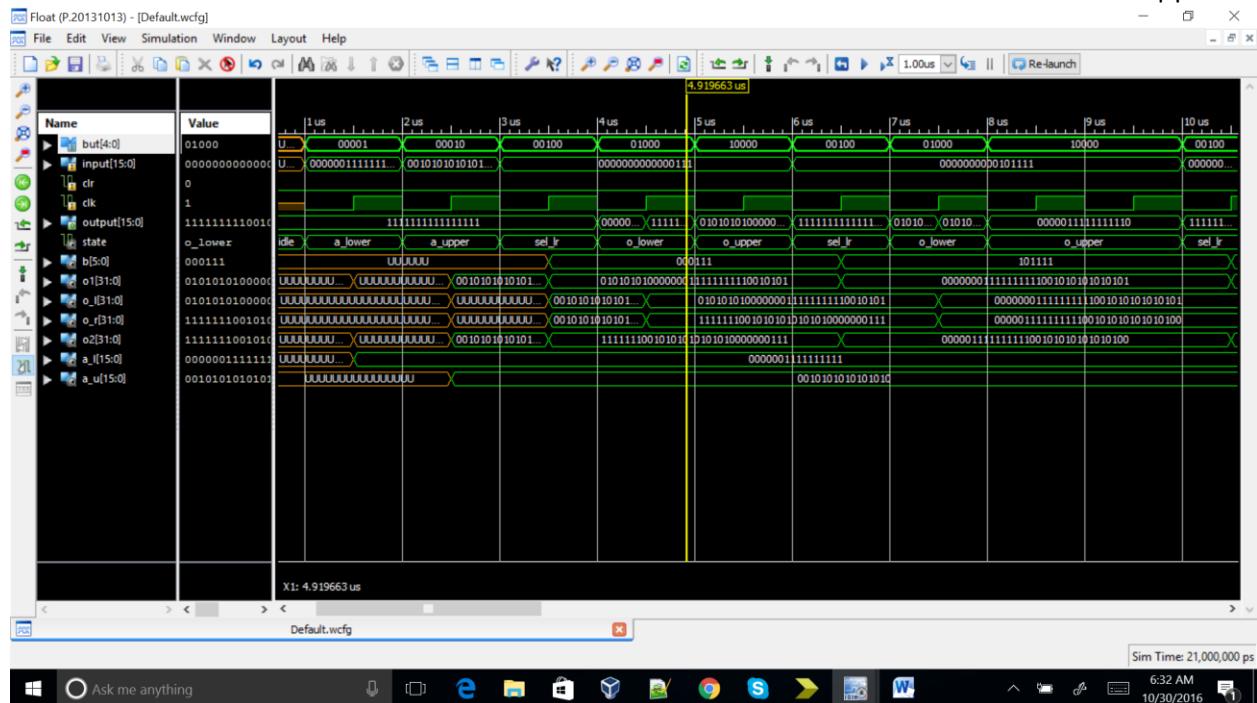


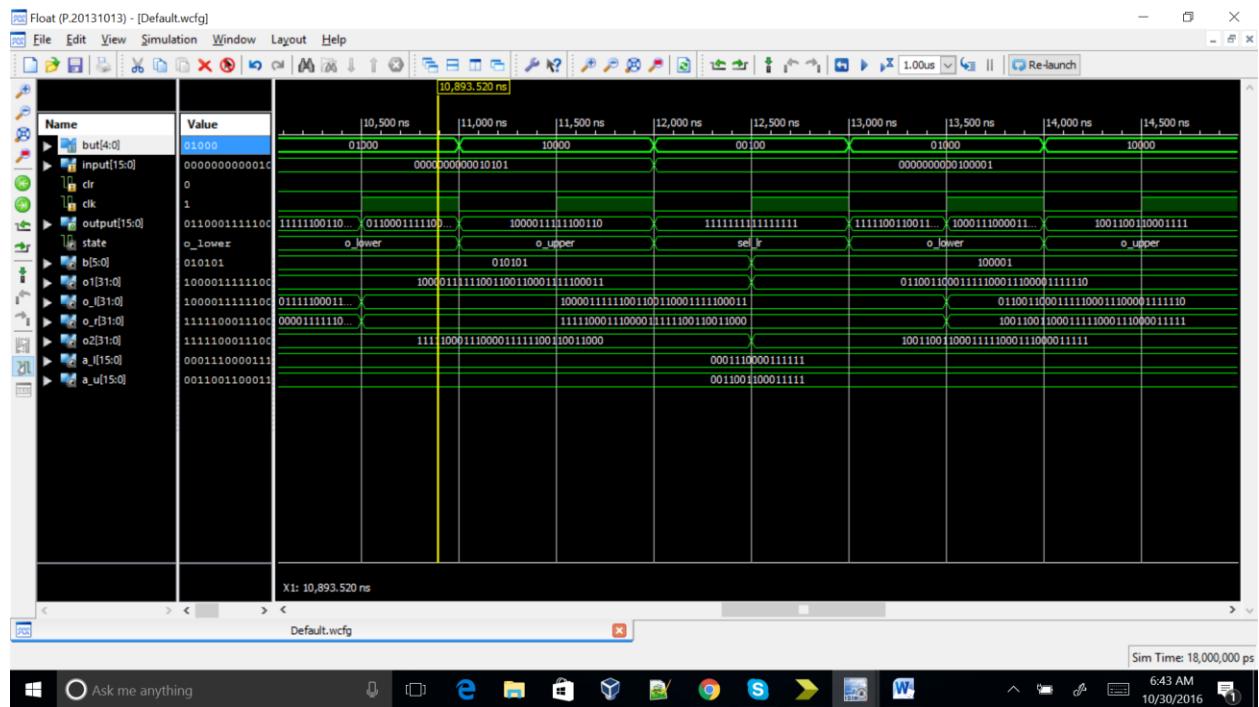
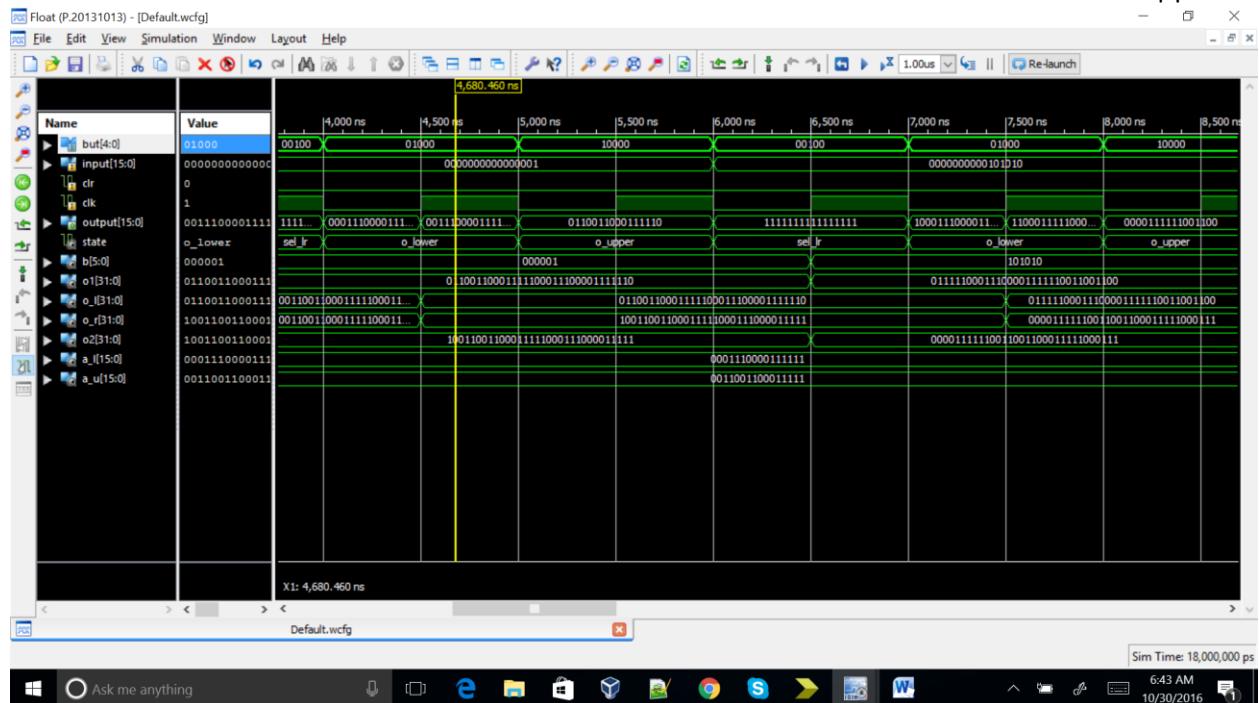
Lab 4

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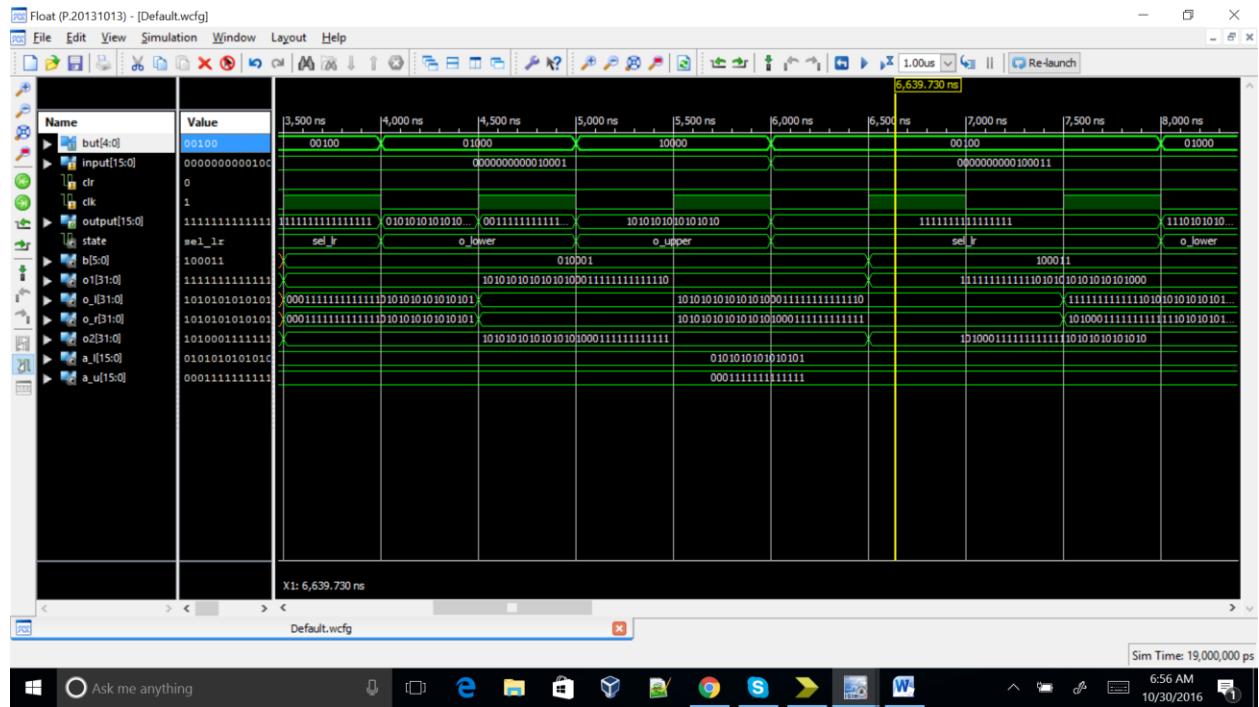
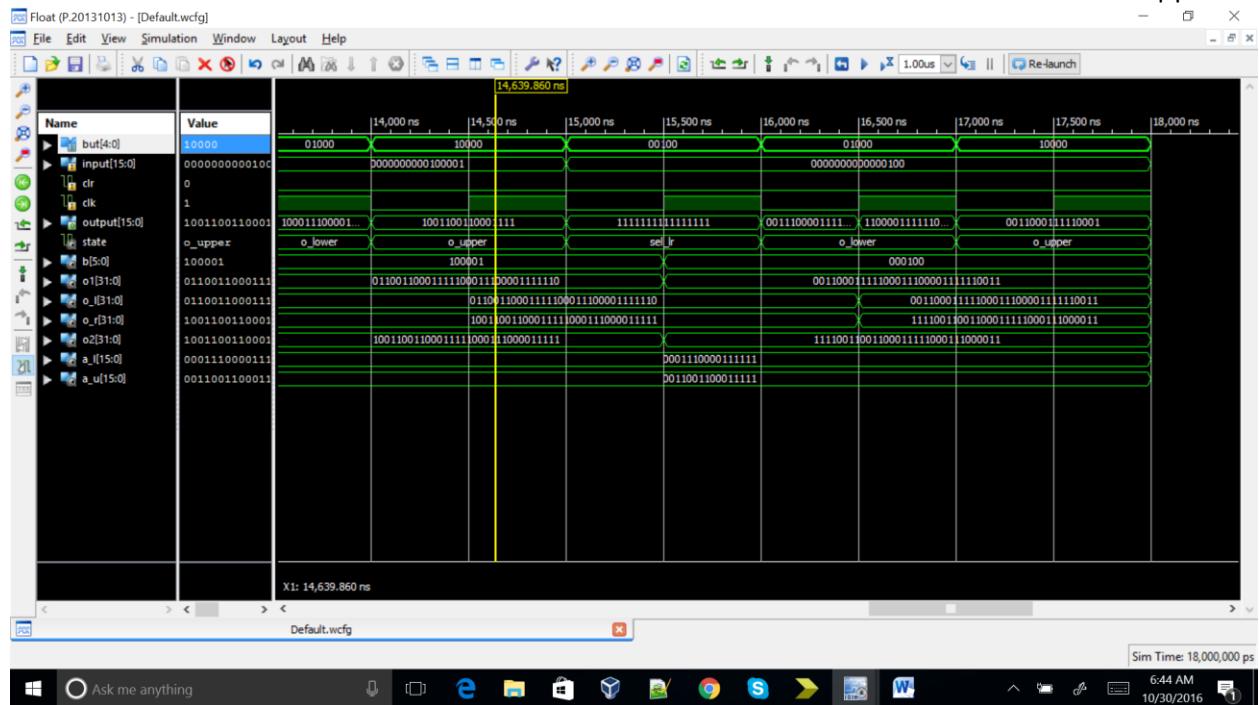
## Lab 4

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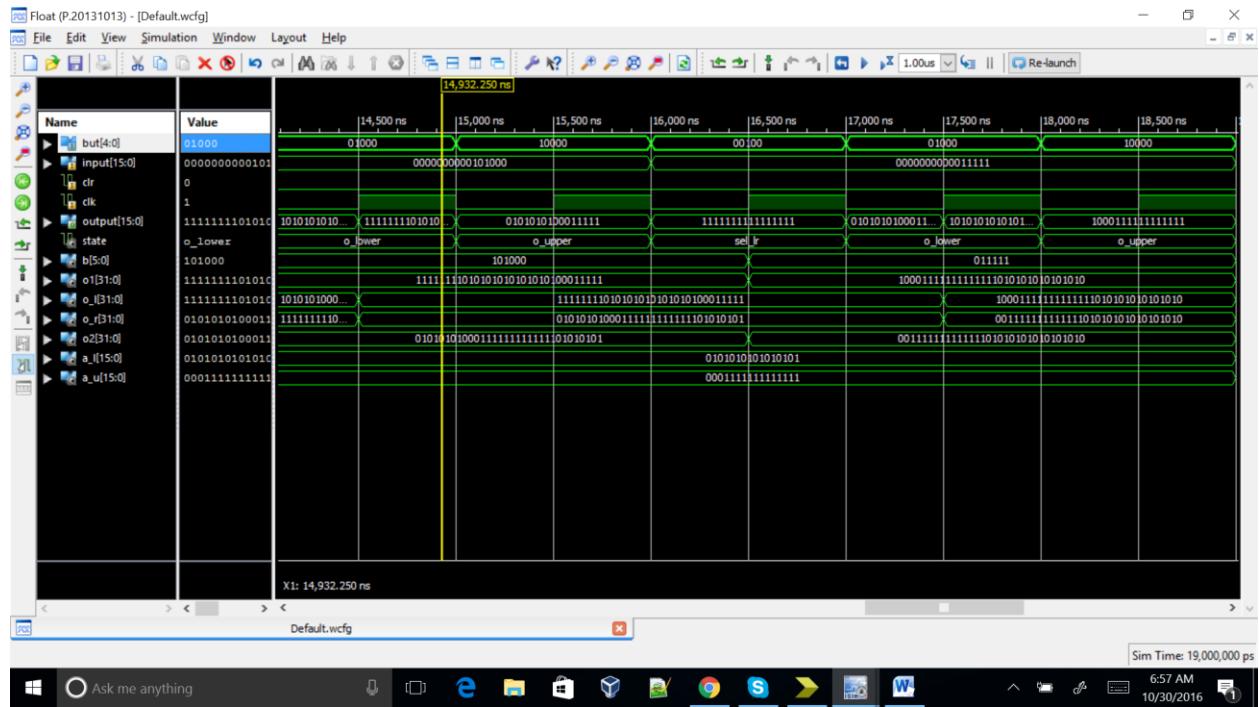
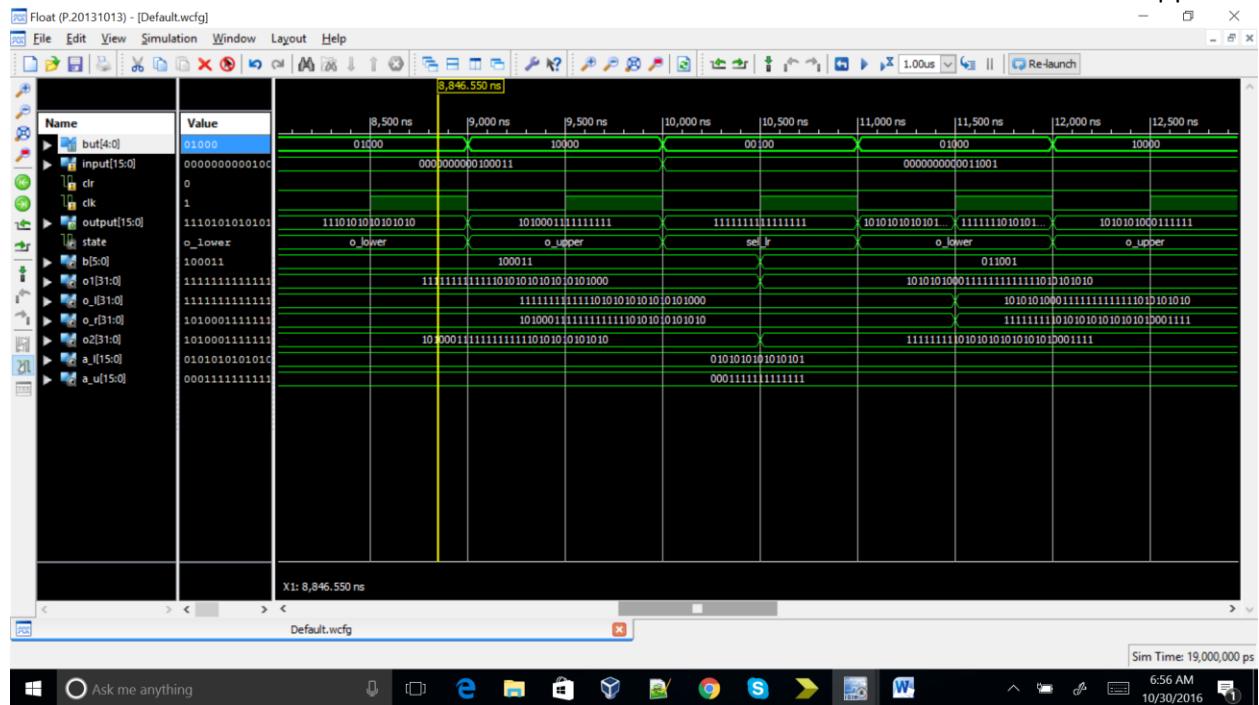
## Lab 4

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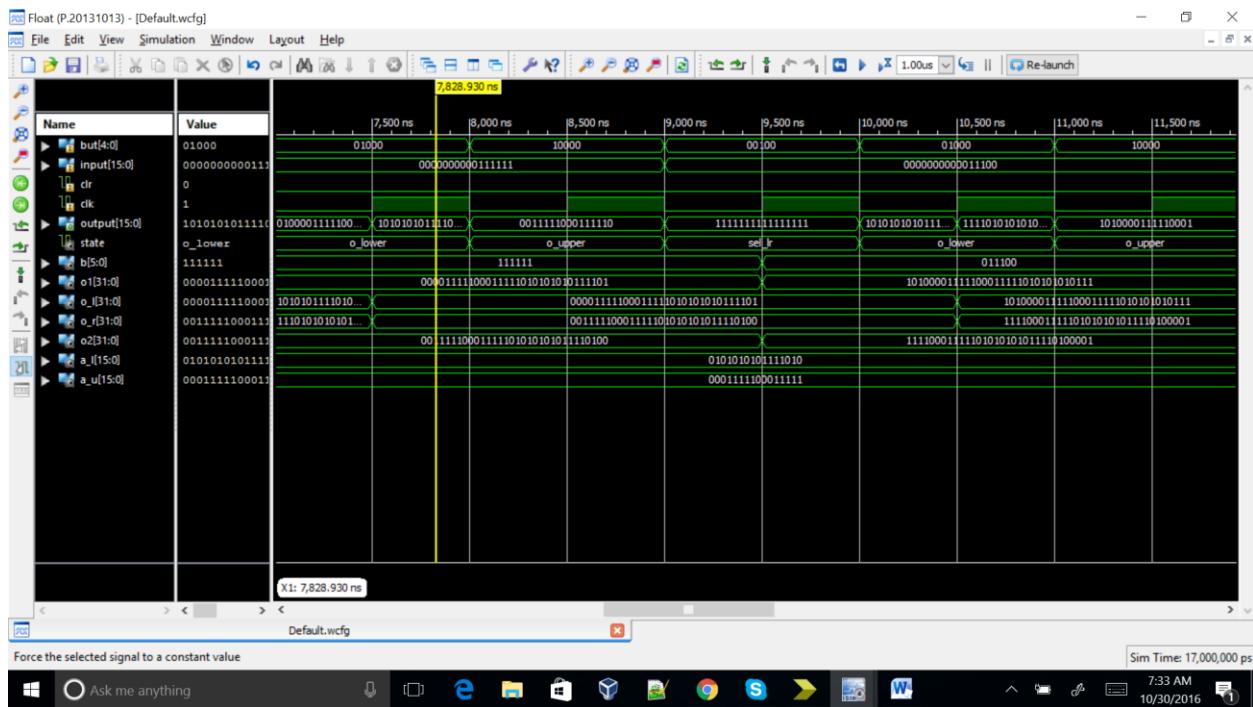
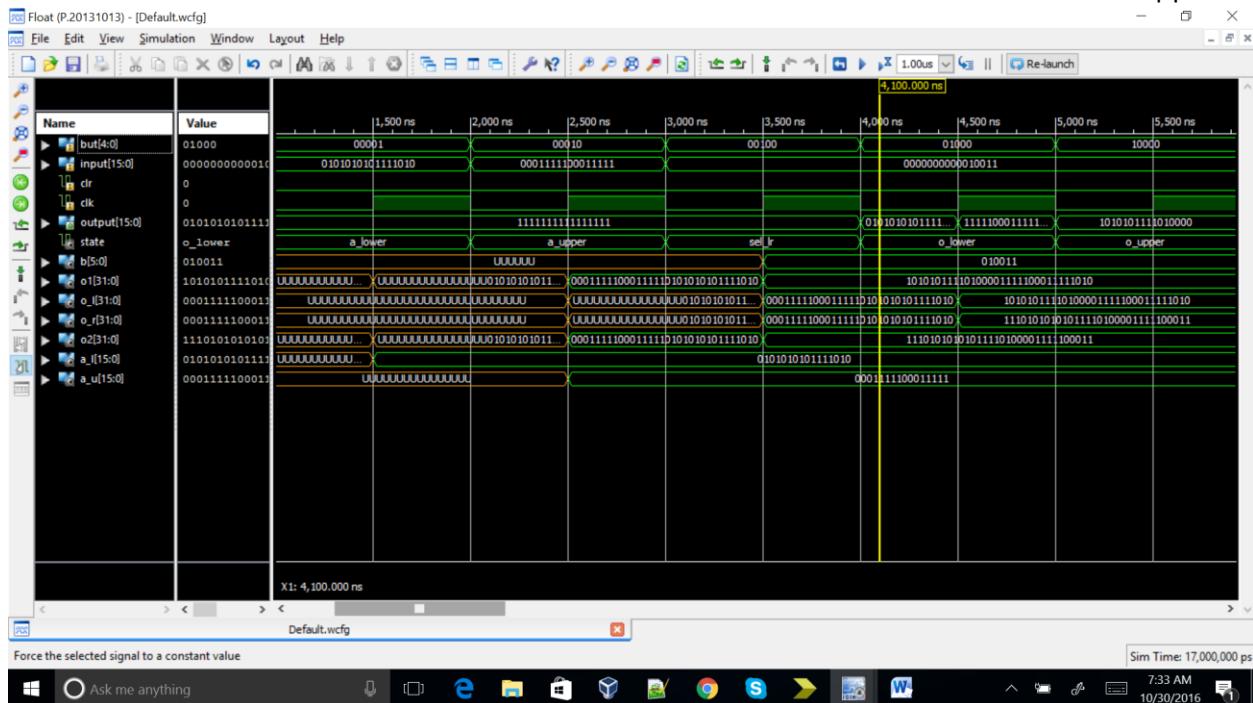
## Lab 4

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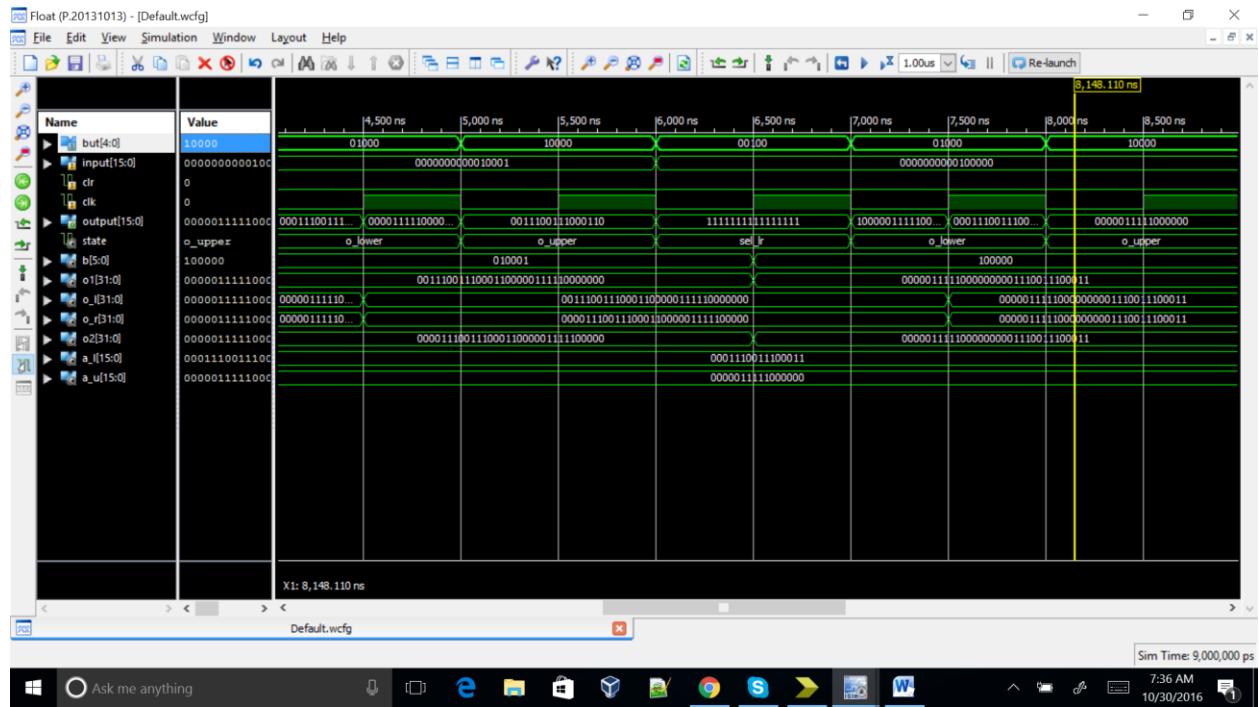
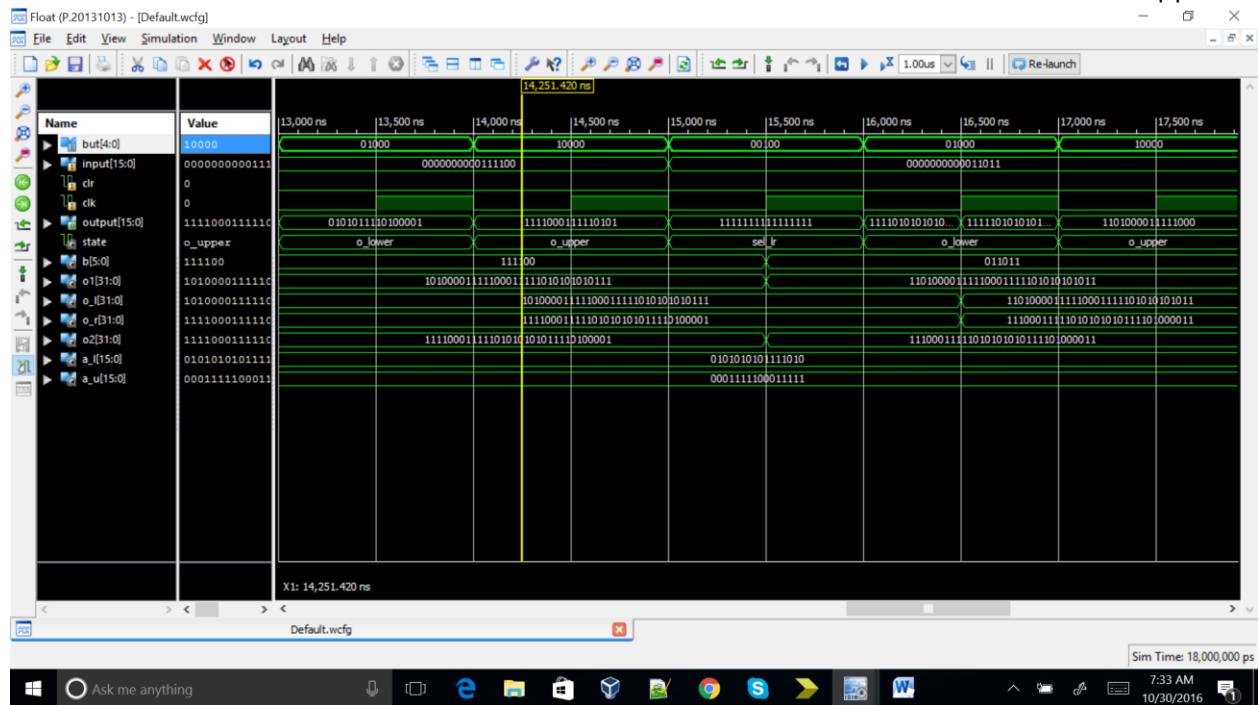
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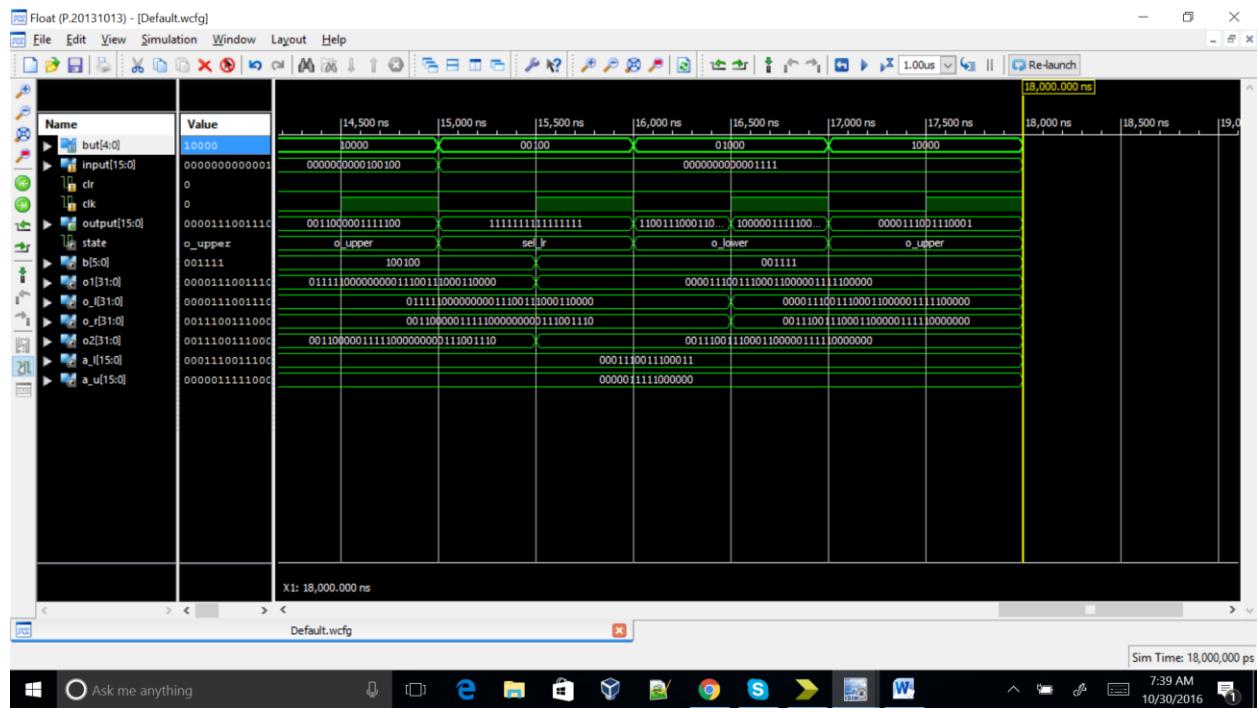
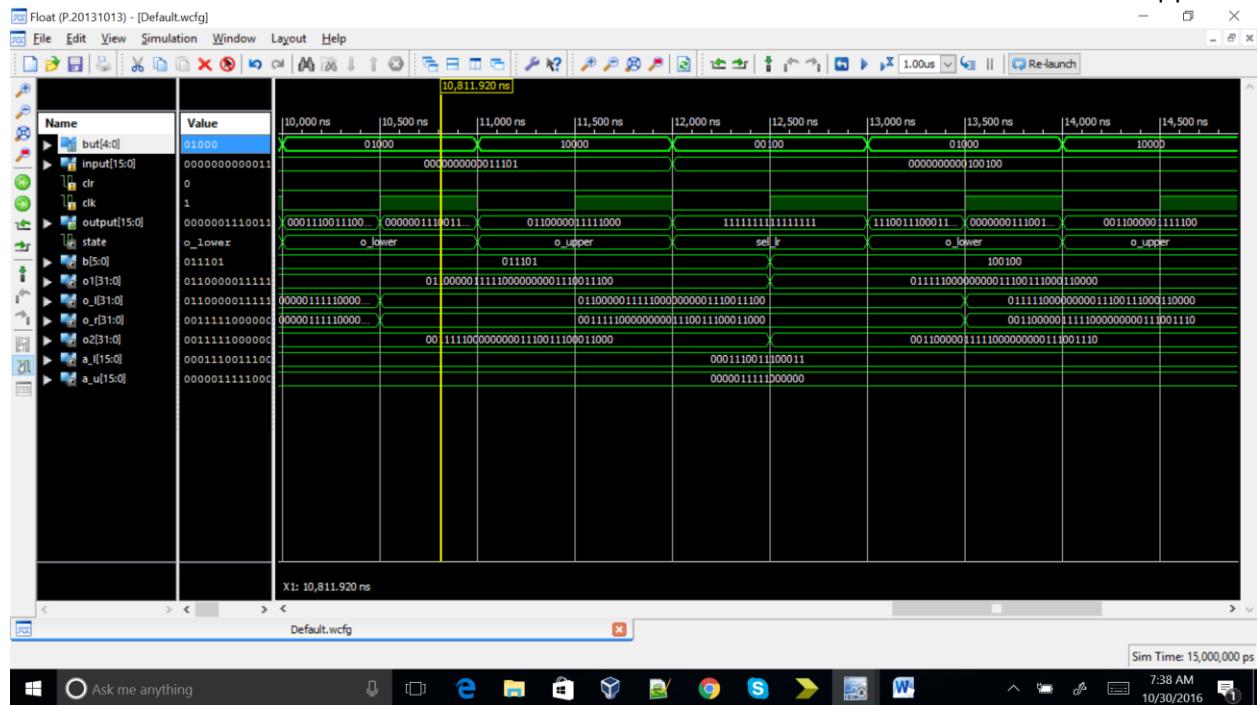
## Lab 4

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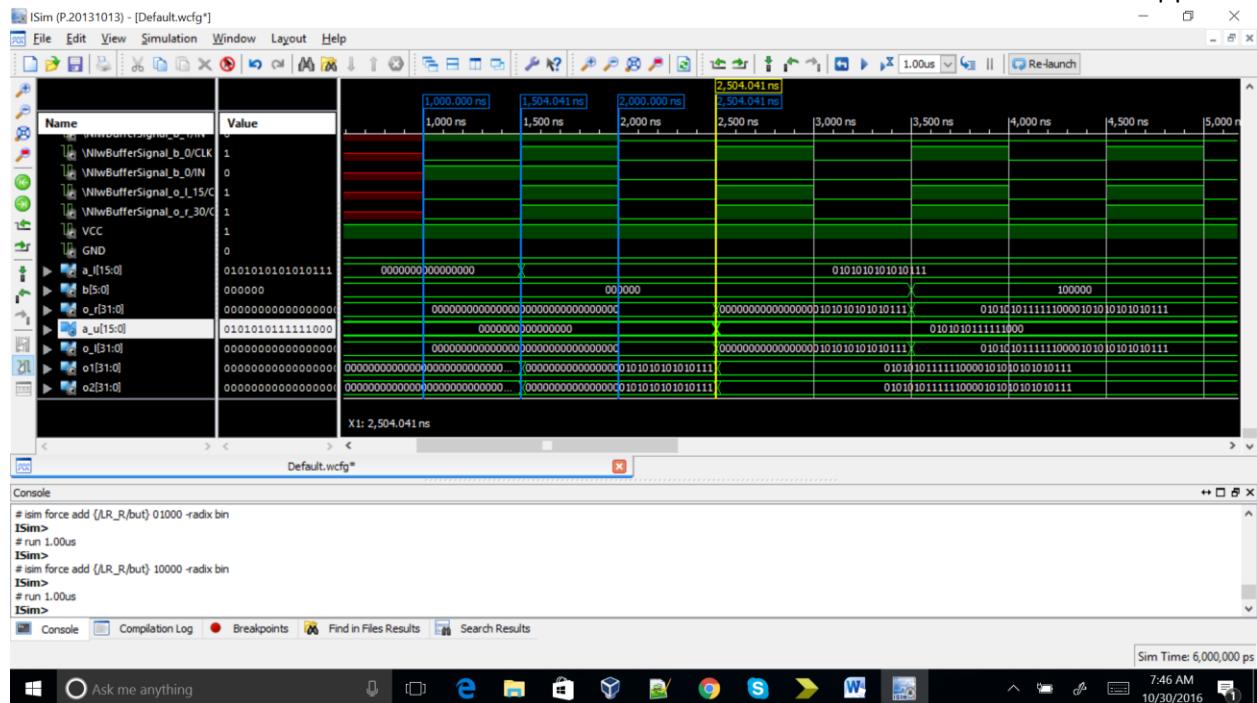
## Lab 4

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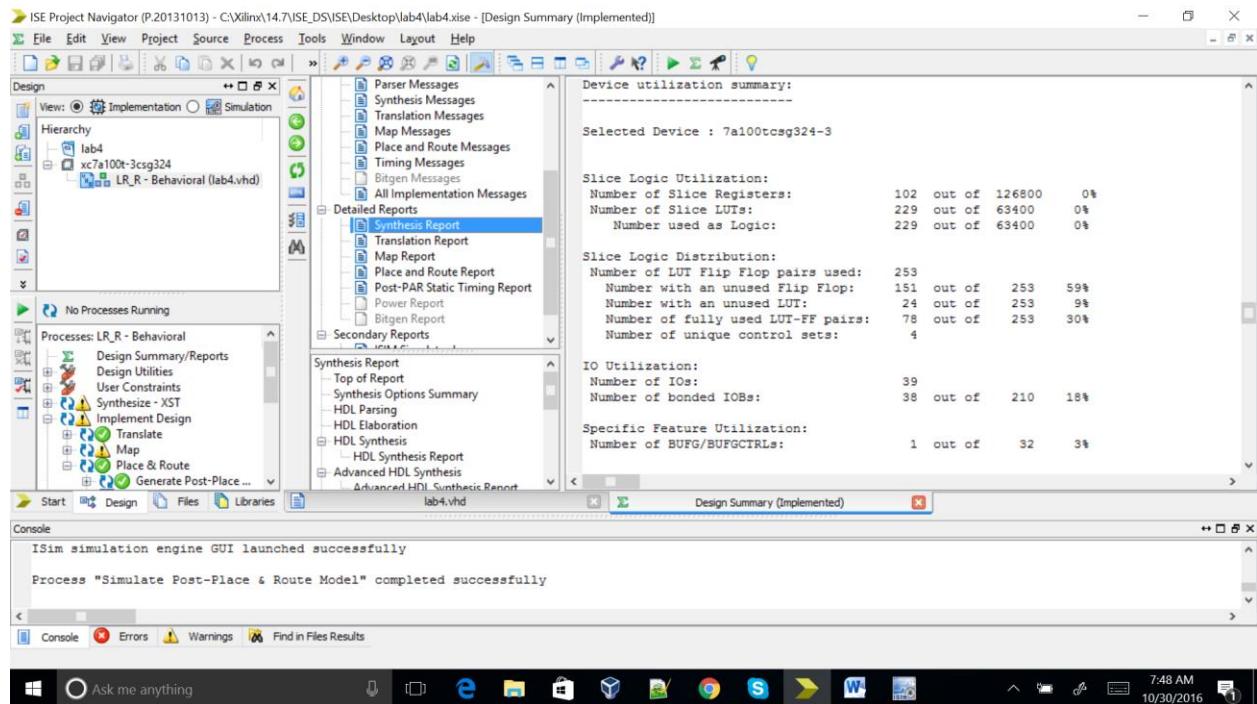
## Lab 4

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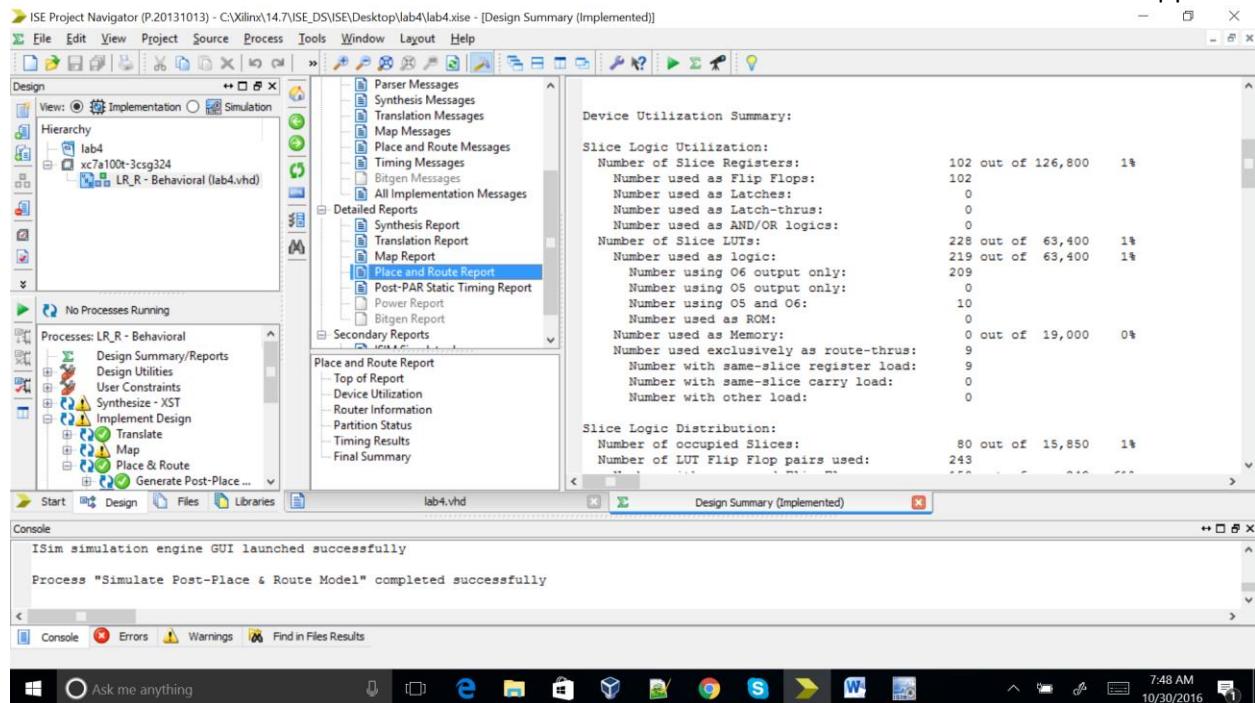
The critical path delay is 3.138ns

The propagation delay of the circuit is 15.65ns

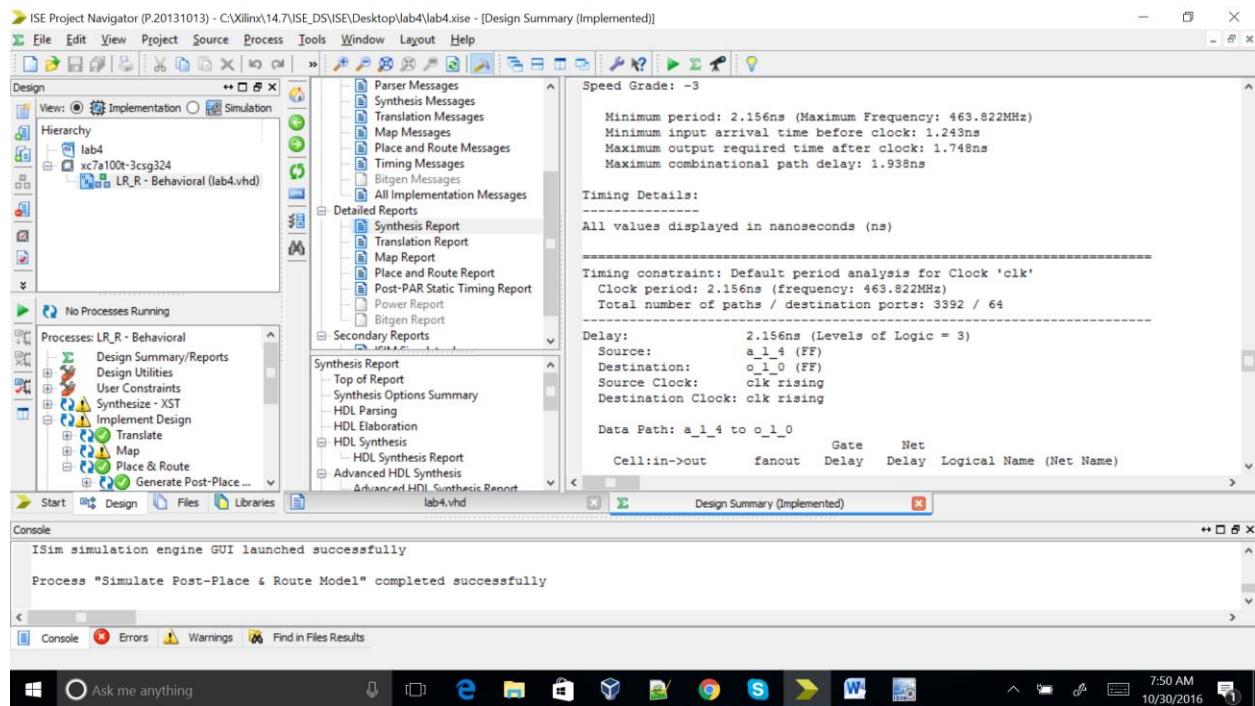


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Above is the device utilization summary report. The amount of resources used in post route phase is less as only required resources are used unlike in synthesis report.



The design can run as fast as 463.82 MHz.

## Lab 4

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Link to the youtube video :

<https://youtu.be/qwfBzTK0tJA>