Lab 5

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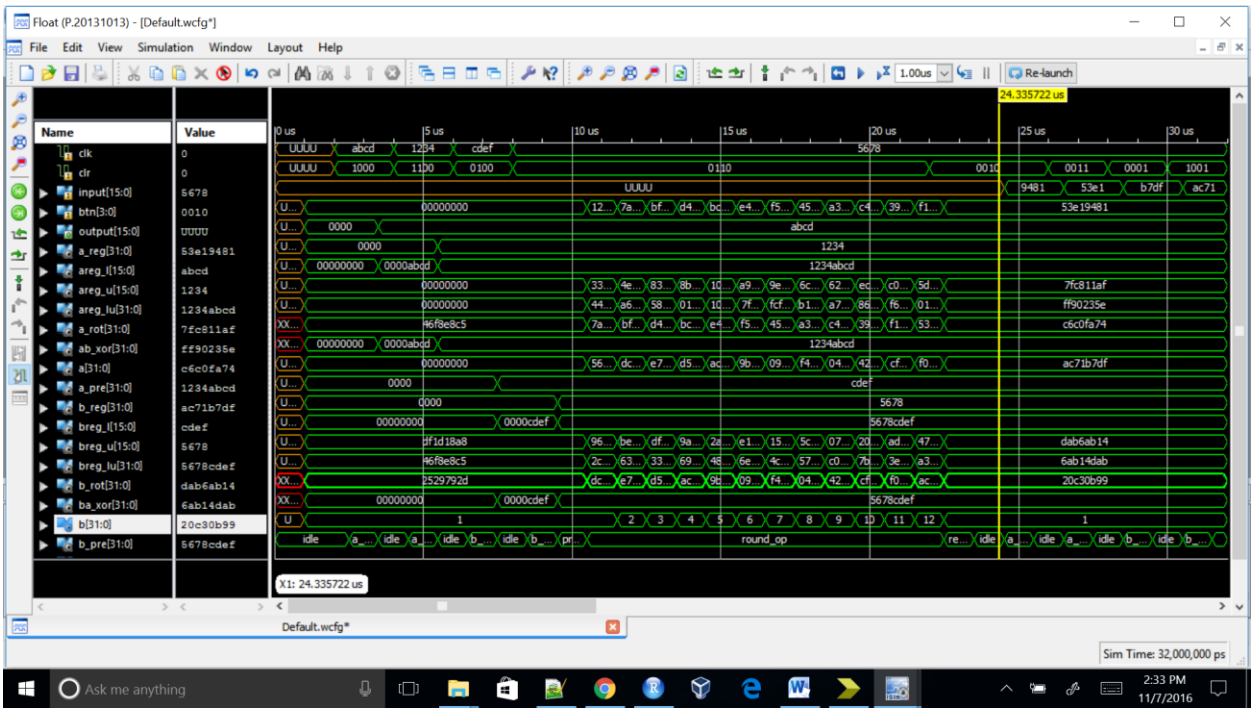
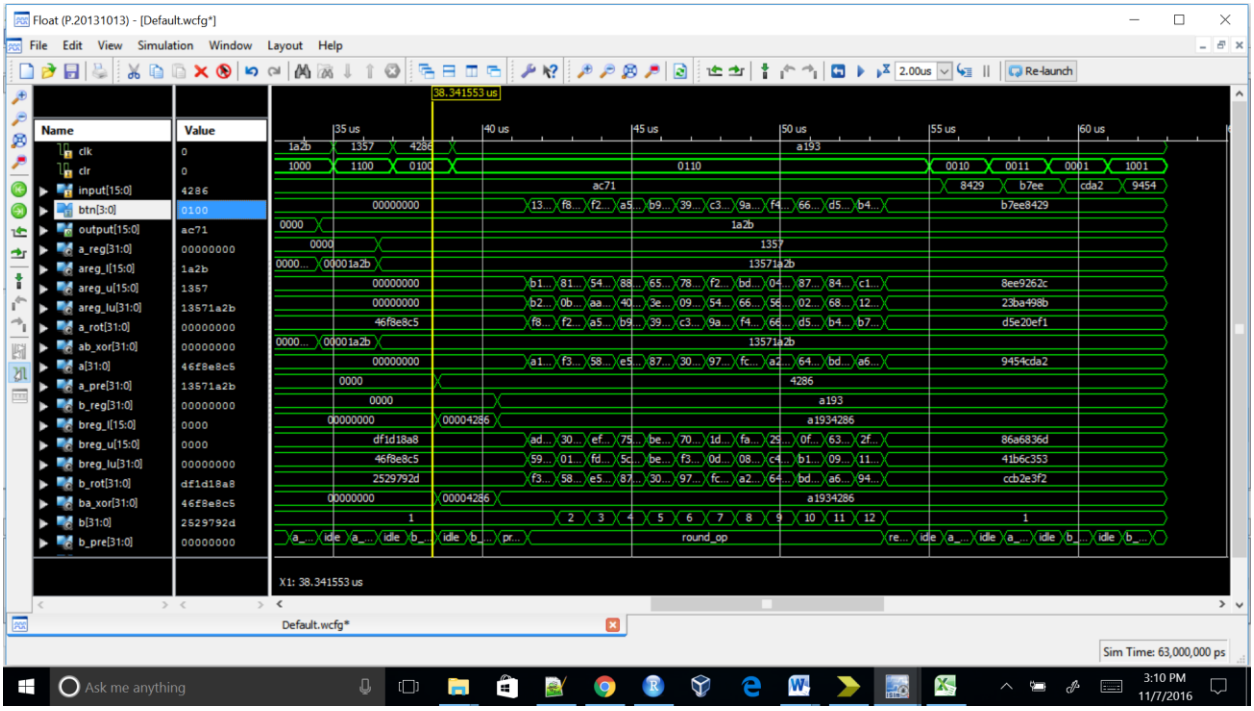
Functional Simulations :





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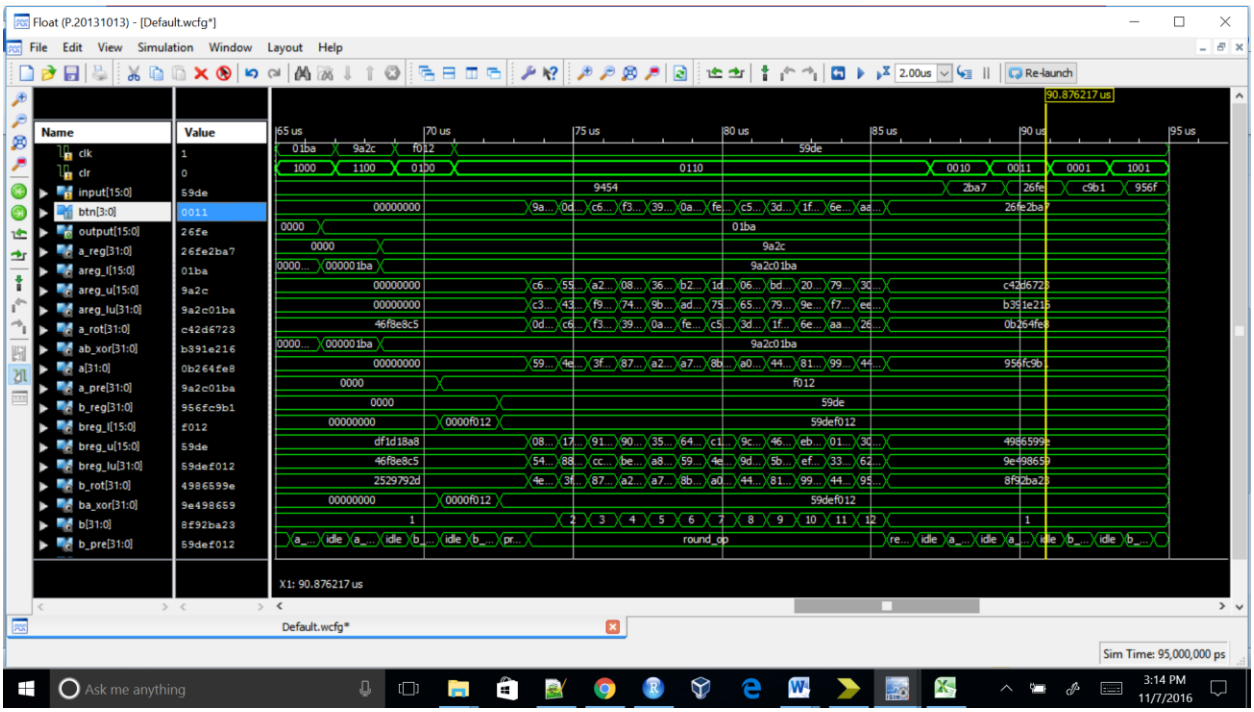

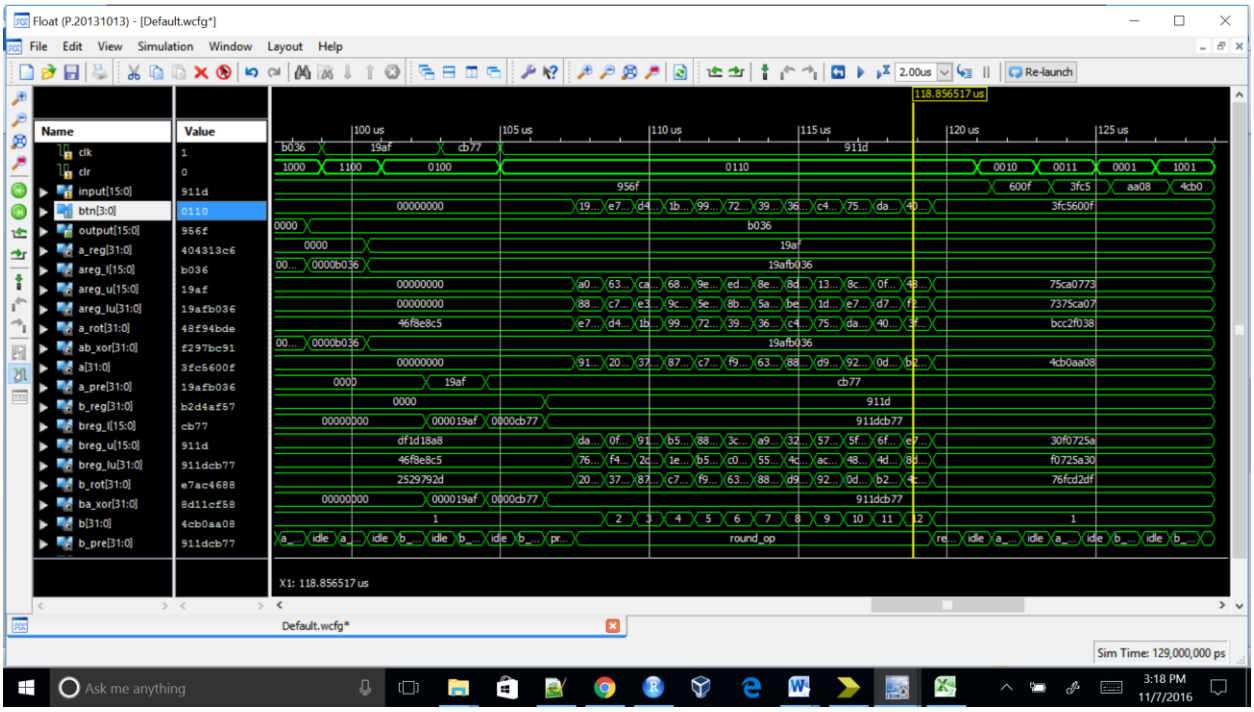

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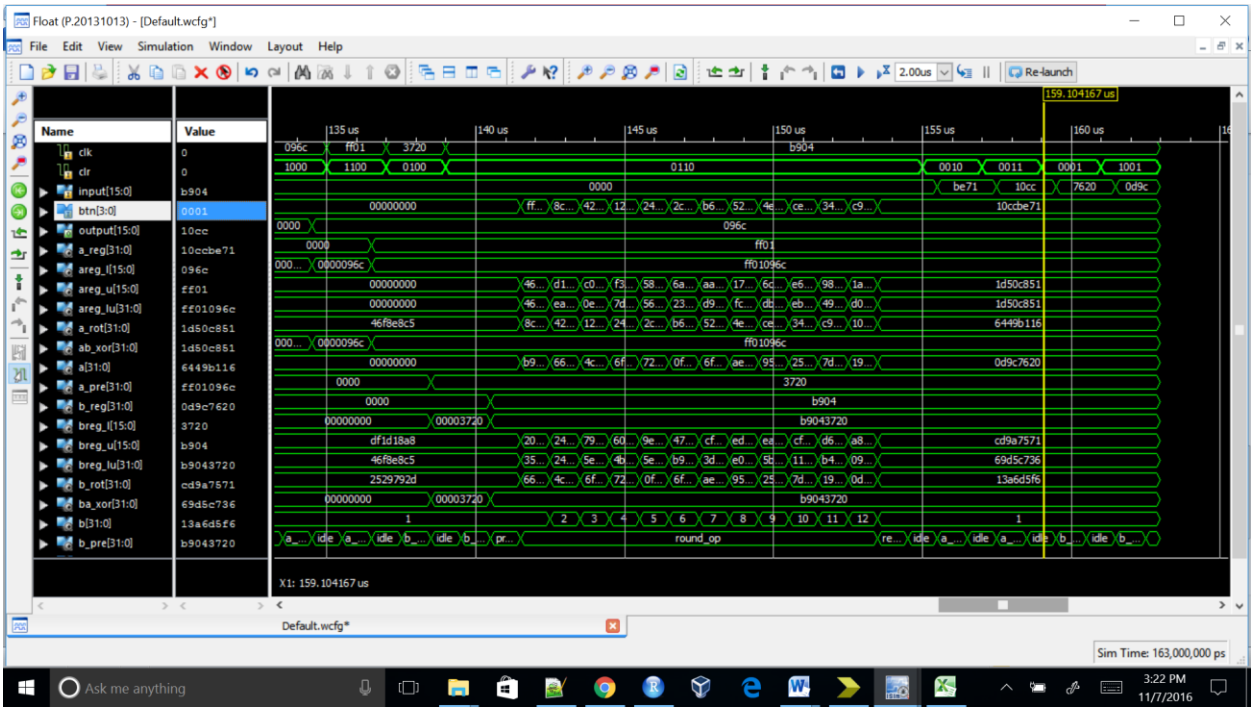
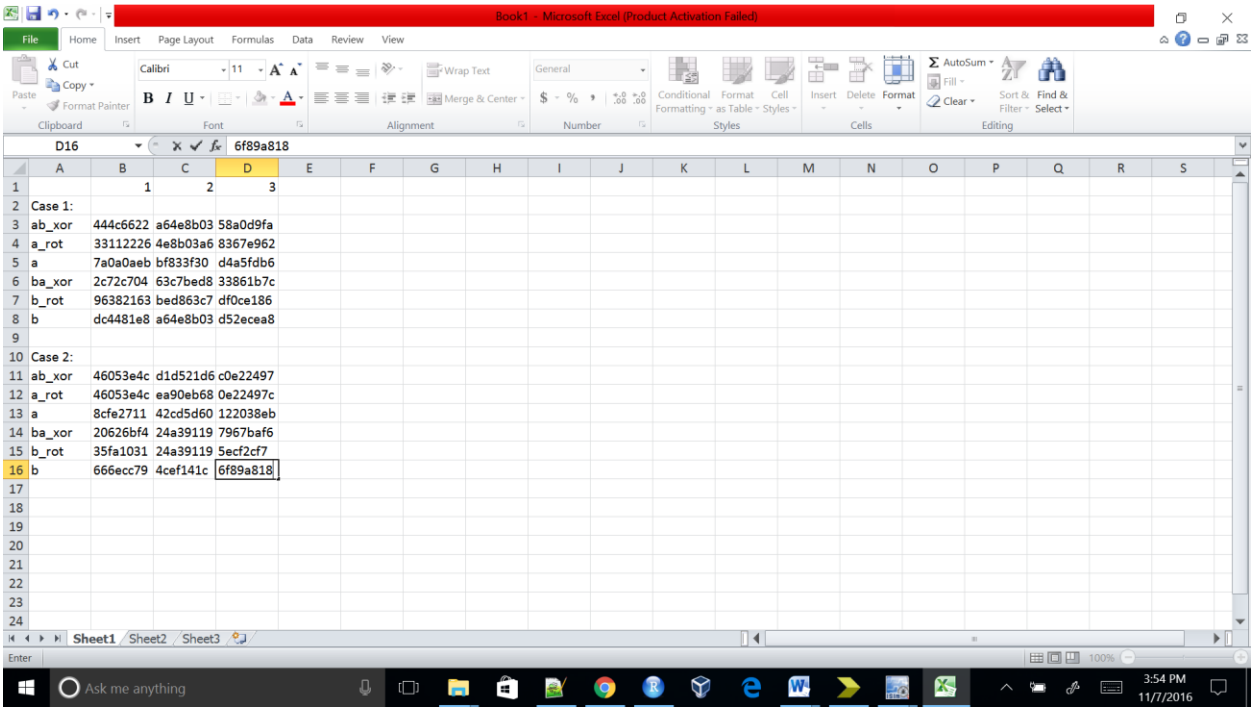


Hand Calculations :



	A	B	C	D
1		1	2	3
2	Case 1:			
3	ab_xor	444c6622	a64e8b03	58a0d9fa
4	a_rot	33112226	4e8b03a6	8367e962
5	a	7a0a0aeb	bf833f30	d4a5fdb6
6	ba_xor	2c72c704	63c7bed8	33861b7c
7	b_rot	96382163	bed863c7	df0ce186
8	b	dc4481e8	a64e8b03	d52ecea8
9				
10	Case 2:			
11	ab_xor	46053e4c	d1d521d6	c0e22497
12	a_rot	46053e4c	ea90eb68	0e22497c
13	a	8cfe2711	42cd5d60	122038eb
14	ba_xor	20626bf4	24a39119	7967baf6
15	b_rot	35fa1031	24a39119	5ecf2cf7
16	b	666ecc79	4cef141c	6f89a818

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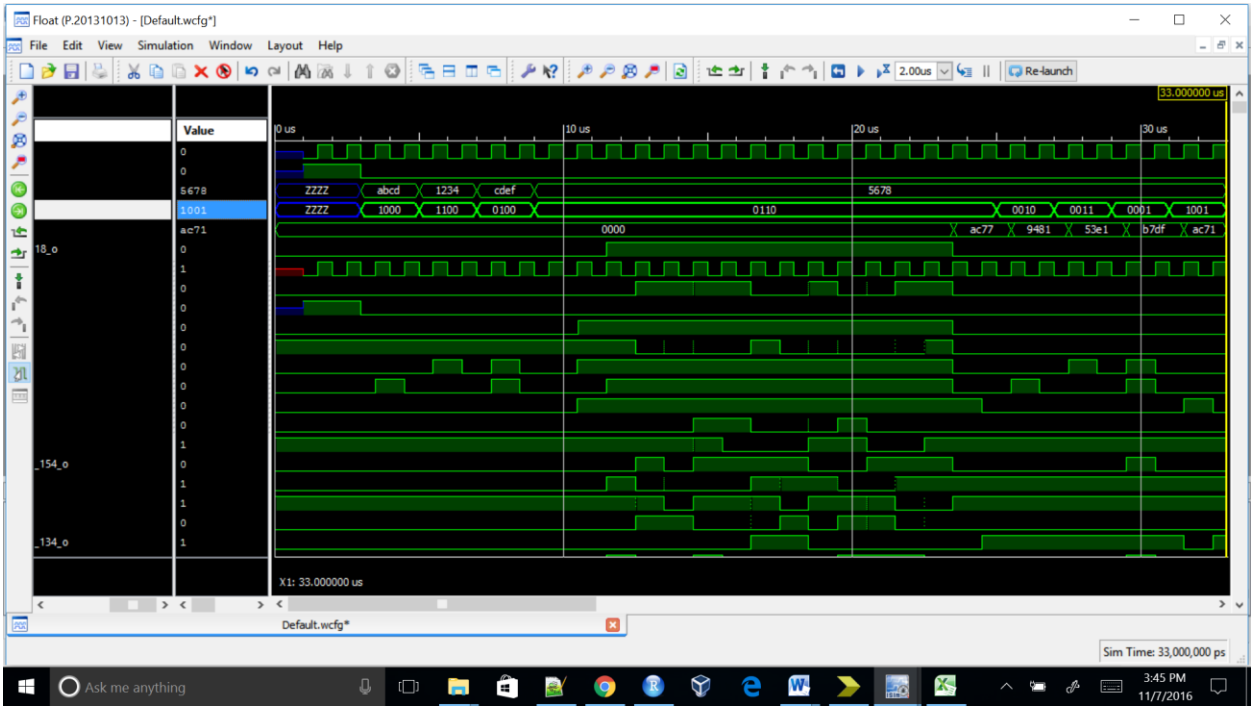
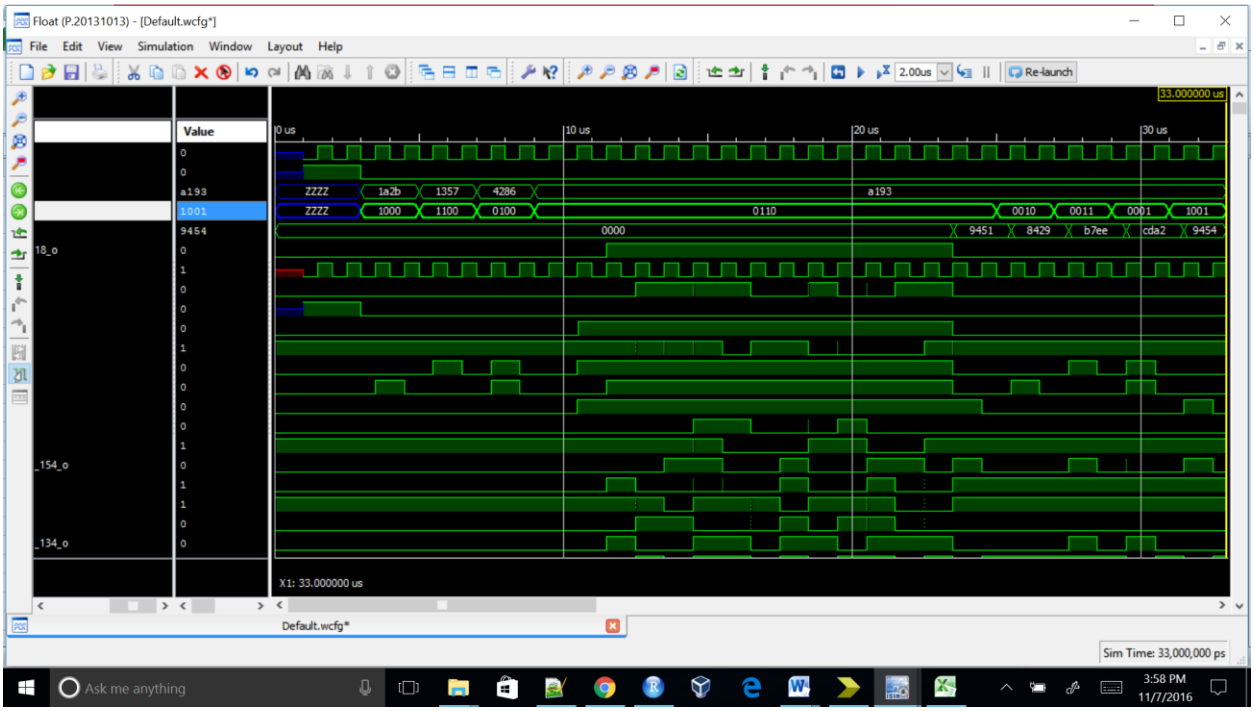
Timing Simulations:





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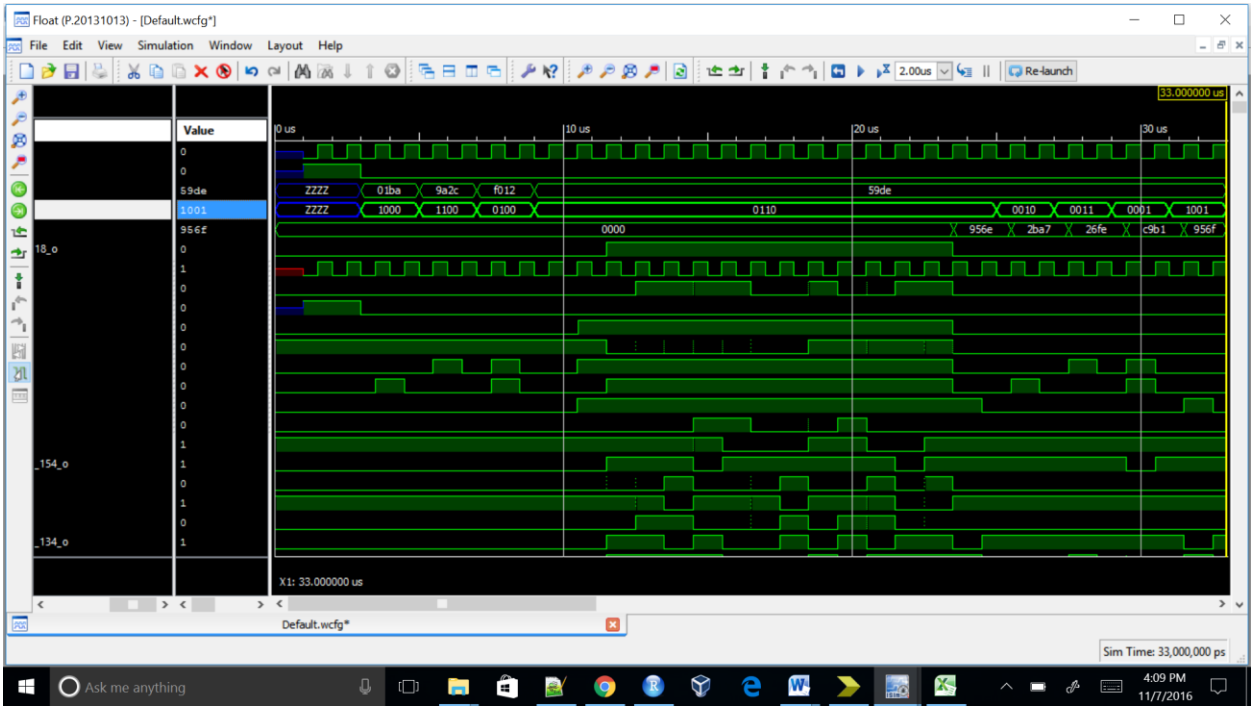

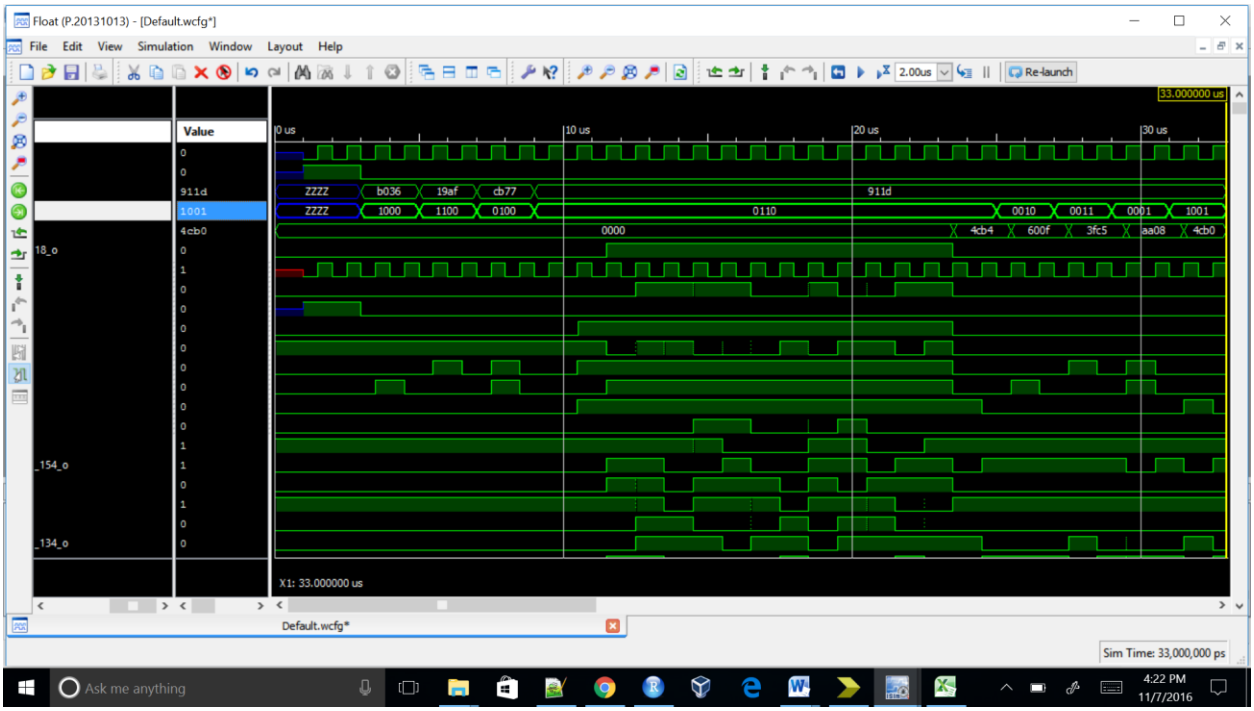

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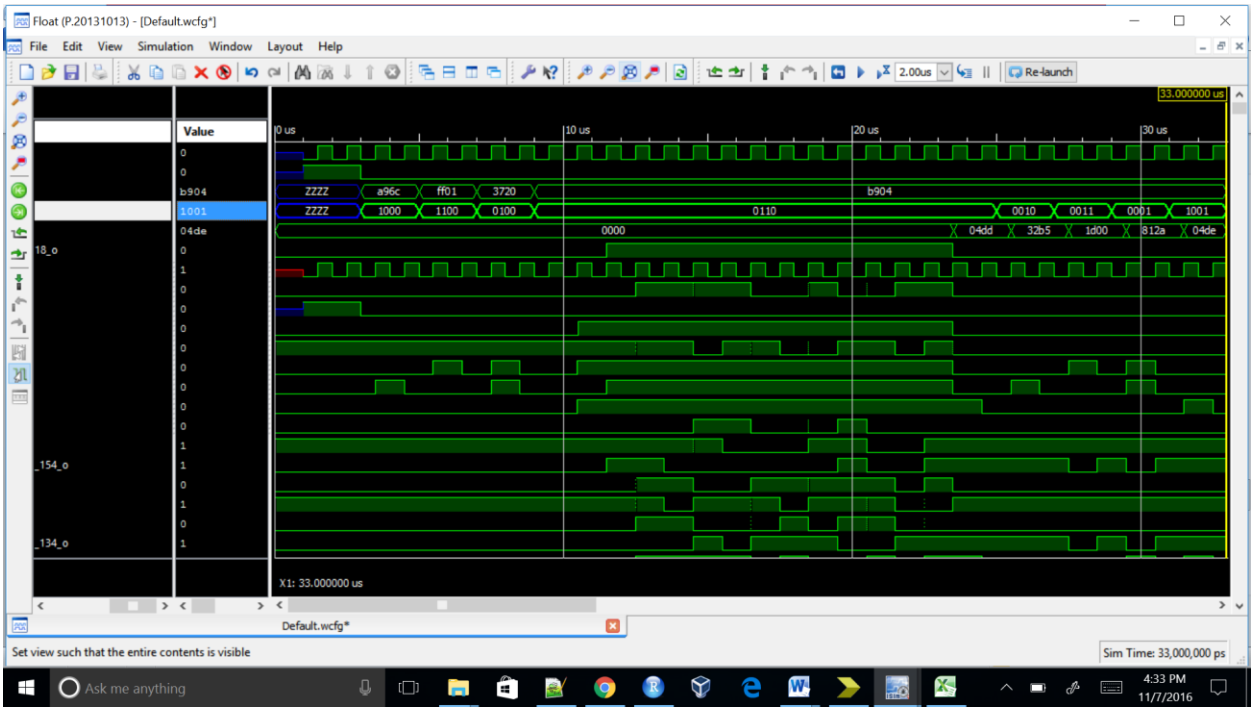

Calculations :

Critical path delay is 7.772ns

Latency of the design is 30 clock cycles

Propagation delay is 233.26 ns

Maximum speed of design is 129.53 Mhz

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Methodology:

Input:

Start with clr by using button N17.Use button M18 to give lower 16bits of A as input. Use M18 and M17 to give the upper 16 bits of A as input. Use M17 to give the lower 16 bits of B as input. Use M17 and P18 to give the upper 16 bits of B as input.

Process:

As soon as upper 16bits of B is given as input the state changes to pre_round in the next clock cycle and then to round_op in the following clock cycle. In round_op state, the counter starts counting from 1 and starts encrypting the input data. The count is reset to 1 after it reaches 12, which is indicated by the ready state. This means that the data has been encrypted and is ready.

Output:

The LEDs are used to display the output. Use P18 to display the lower 16 bits of A. Use P18 and P17 to show the upper 16 bits of A. Use P17 to show the lower 16 bits of B. UseP17 and M18 to show the upper 16 bits of B.

Youtube video Link:

https://youtu.be/qc-R8BRIreM

FSM:

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