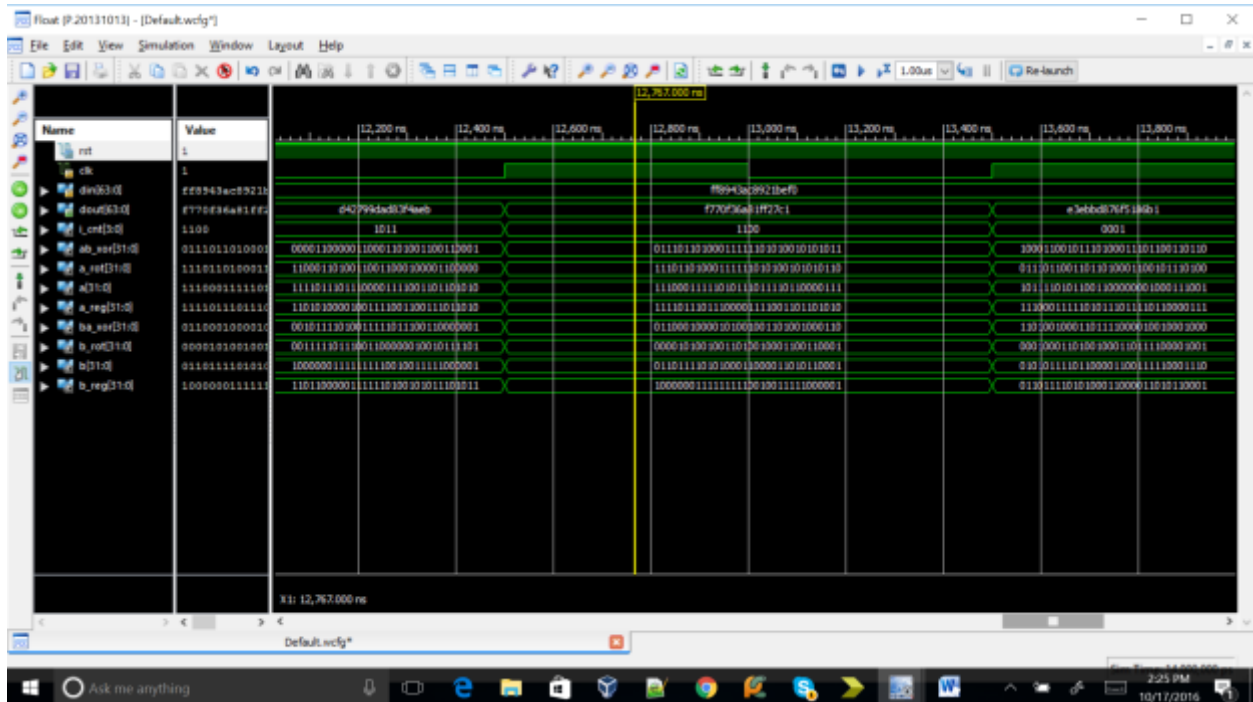
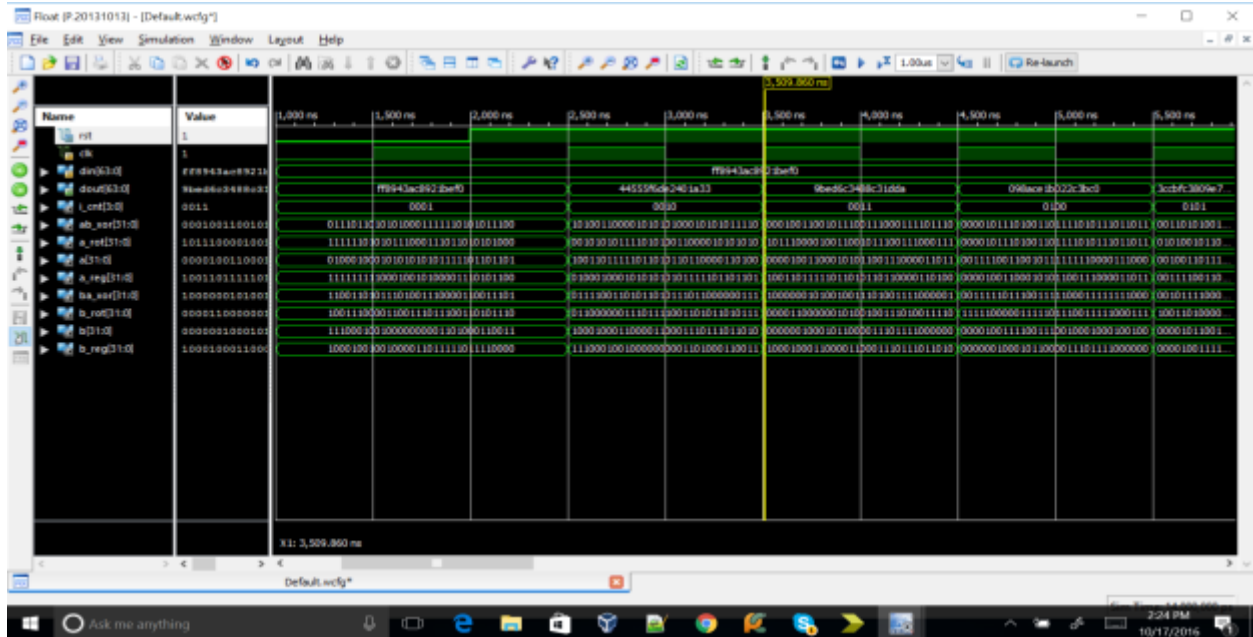
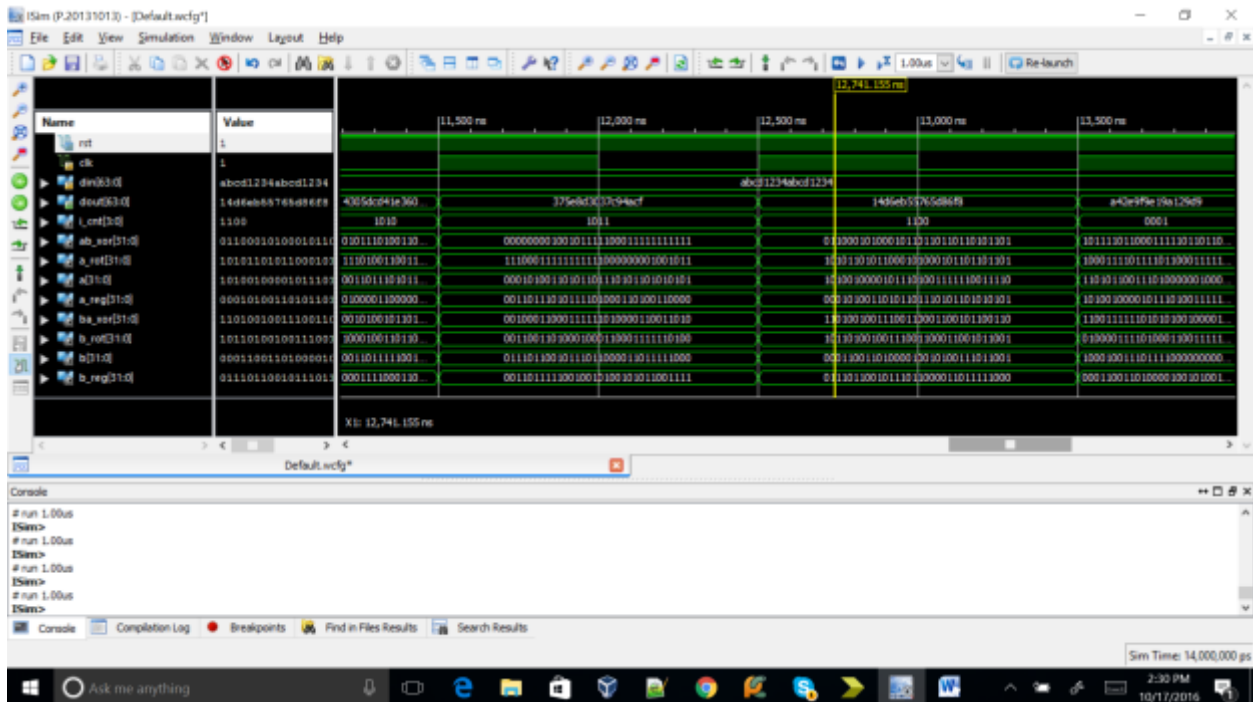
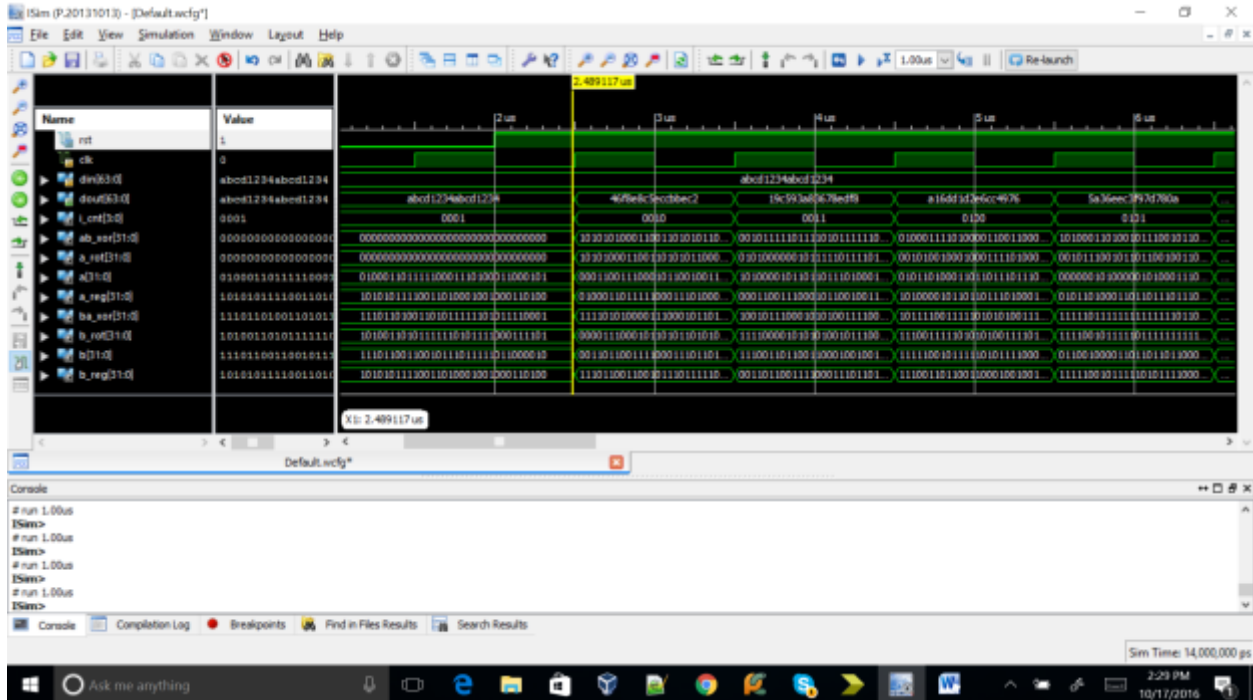


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1 function



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The screenshot displays the Intel Quartus Prime IDE interface during a timing simulation. The top window shows a logic analyzer view with a table of signal names and values, and a corresponding timing diagram. The bottom window shows the console output of the simulation.

Logic Analyzer Table:

Name	Value
rst	1
clk	0
div[3:0]	FF67aed432abcdF
div[3:0]	FF67aed432abcdF
cont[3:0]	0001
ab_sel[3:0]	10111100011111001100011000110010
a_sel[3:0]	01011110001111100110001100011001
a[3:0]	101001010011011010010111011110
a_reg[3:0]	11111110101010100111101101101101
ba_sel[3:0]	11100110000111011111011100000001
b_sel[3:0]	01111001100000111011111100000000
b[3:0]	10111111000100111011110010001010
b_reg[3:0]	010000110010101010101100111111

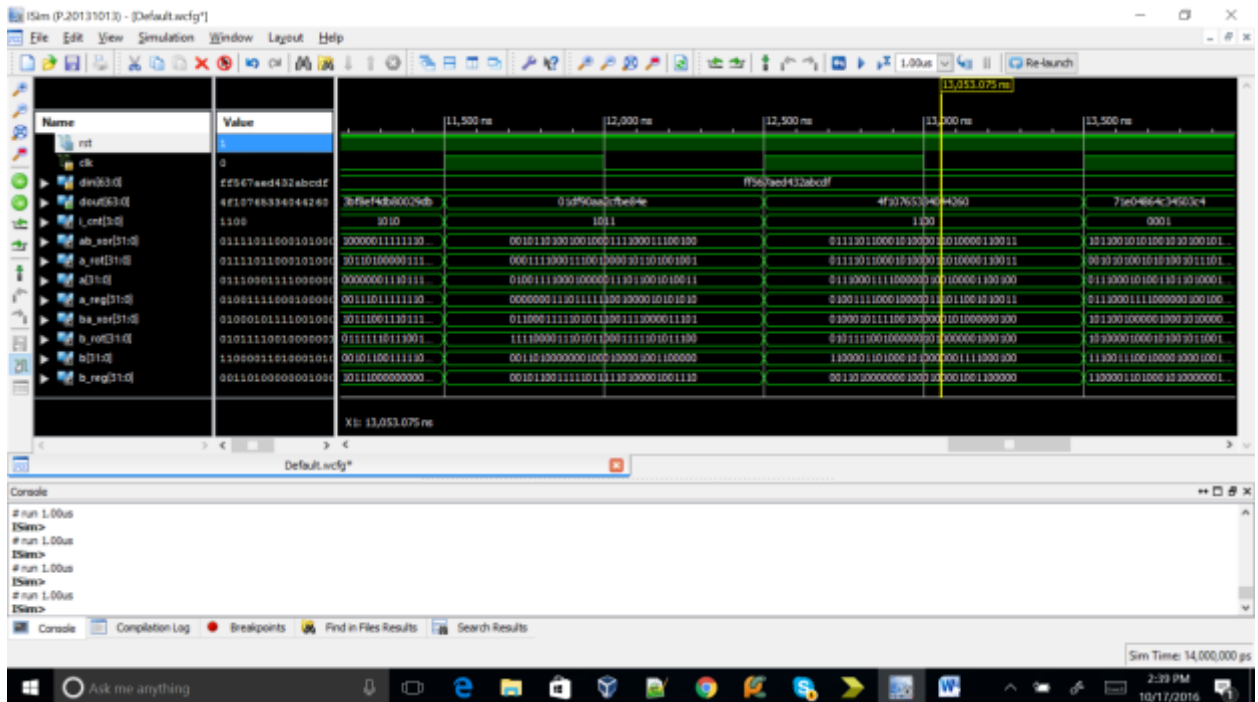
Timing Diagram: The diagram shows the timing of the signals over time. The x-axis represents time in microseconds (us), with markers at 2 us, 3 us, 4 us, 5 us, and 6 us. The y-axis represents the signal values. The signals are color-coded: green for 'rst', blue for 'clk', and various shades of green and yellow for the other signals.

Console Output:

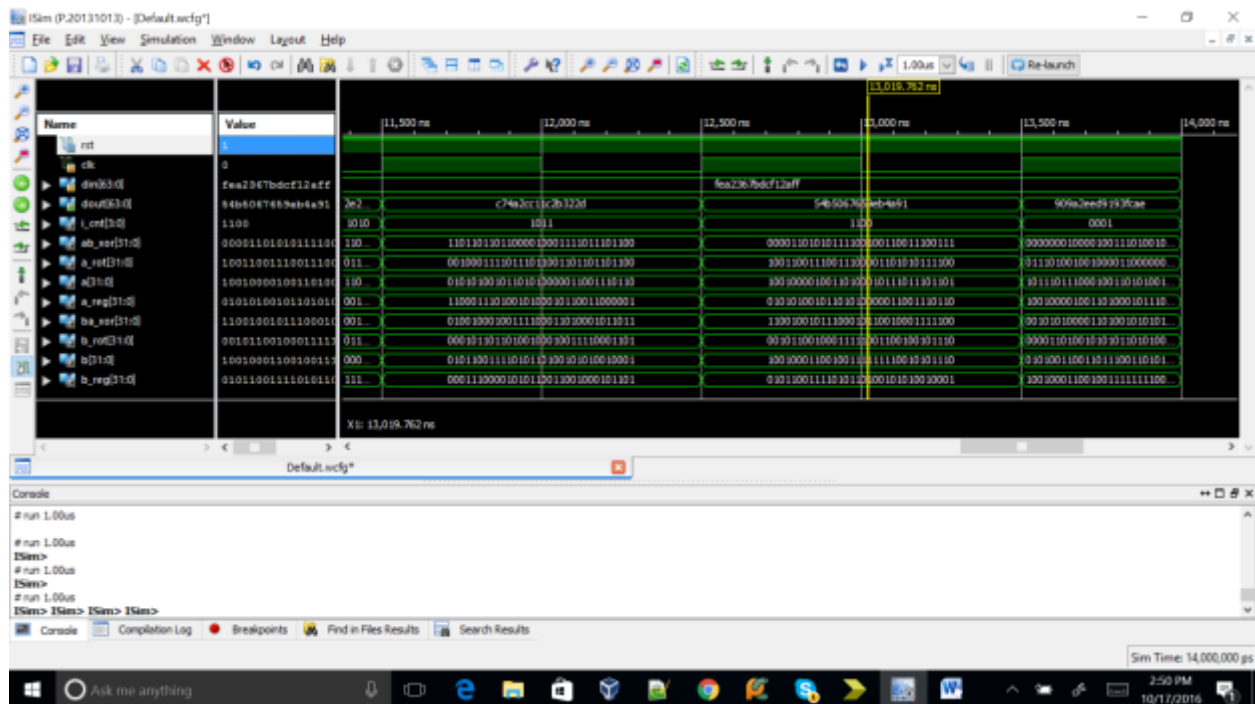
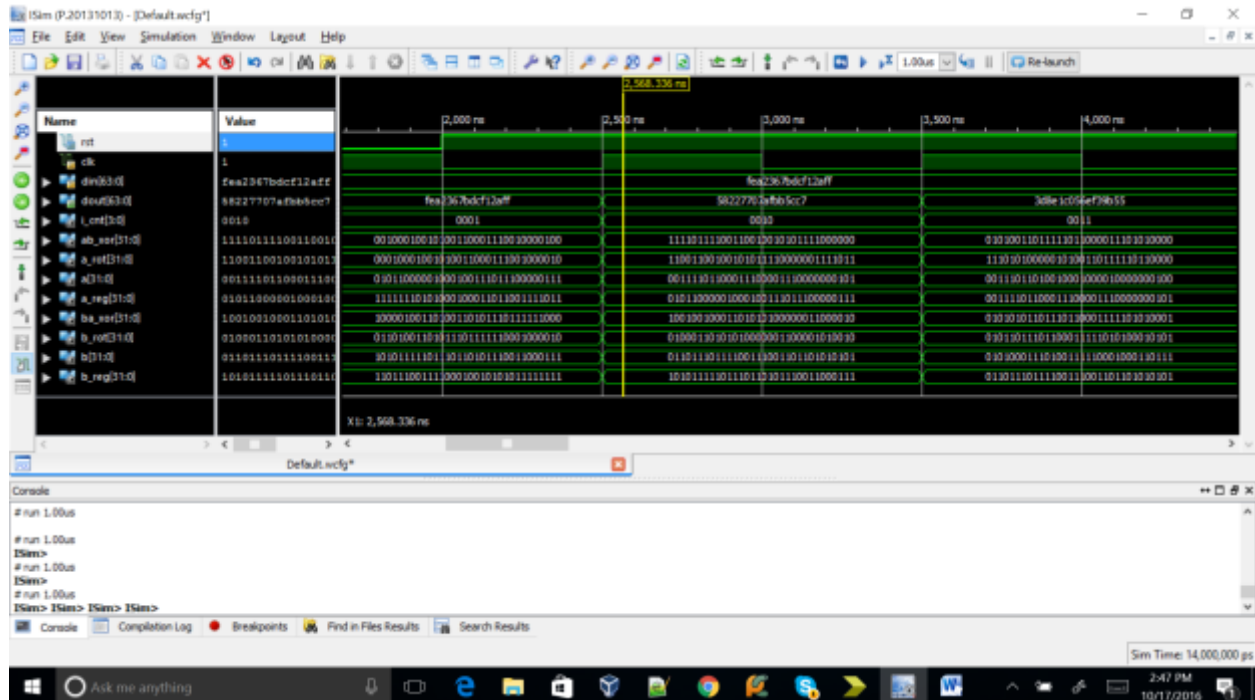
```

# run 1.00us
$Sim>
# run 1.00us
$Sim>
# run 1.00us
$Sim>
# run 1.00us
$Sim>
# run 1.00us
$Sim>
# run 1.00us
$Sim>

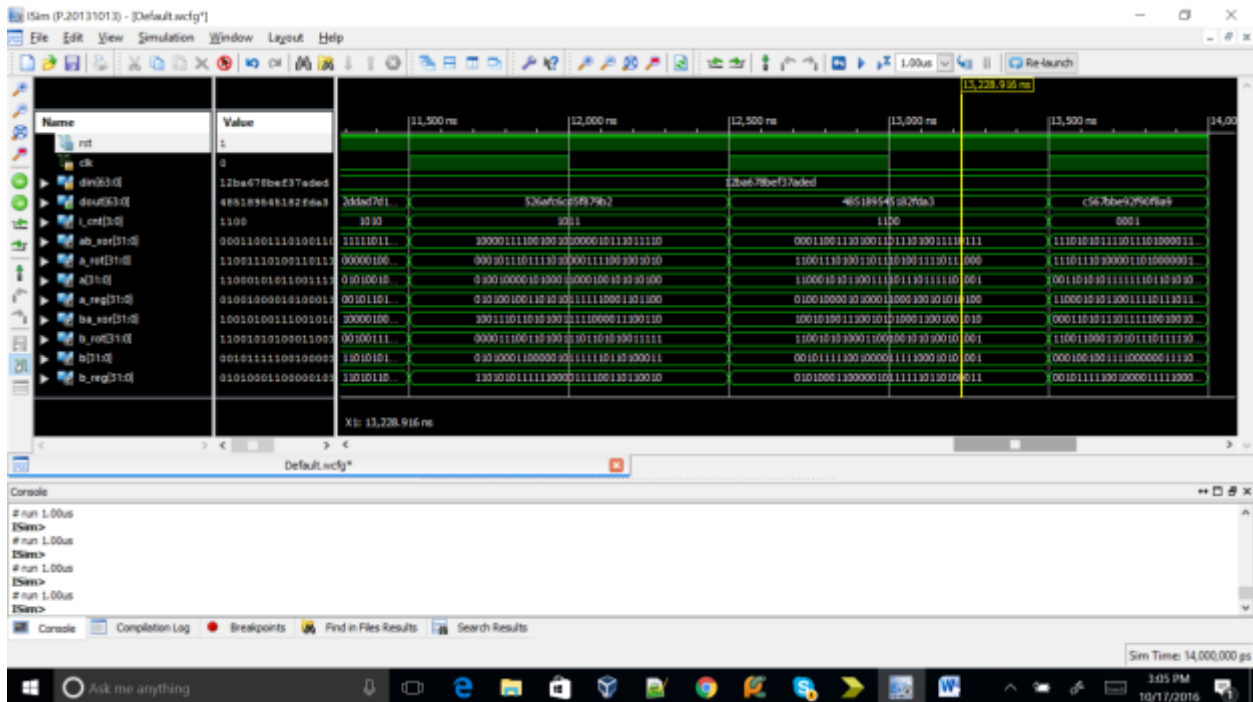
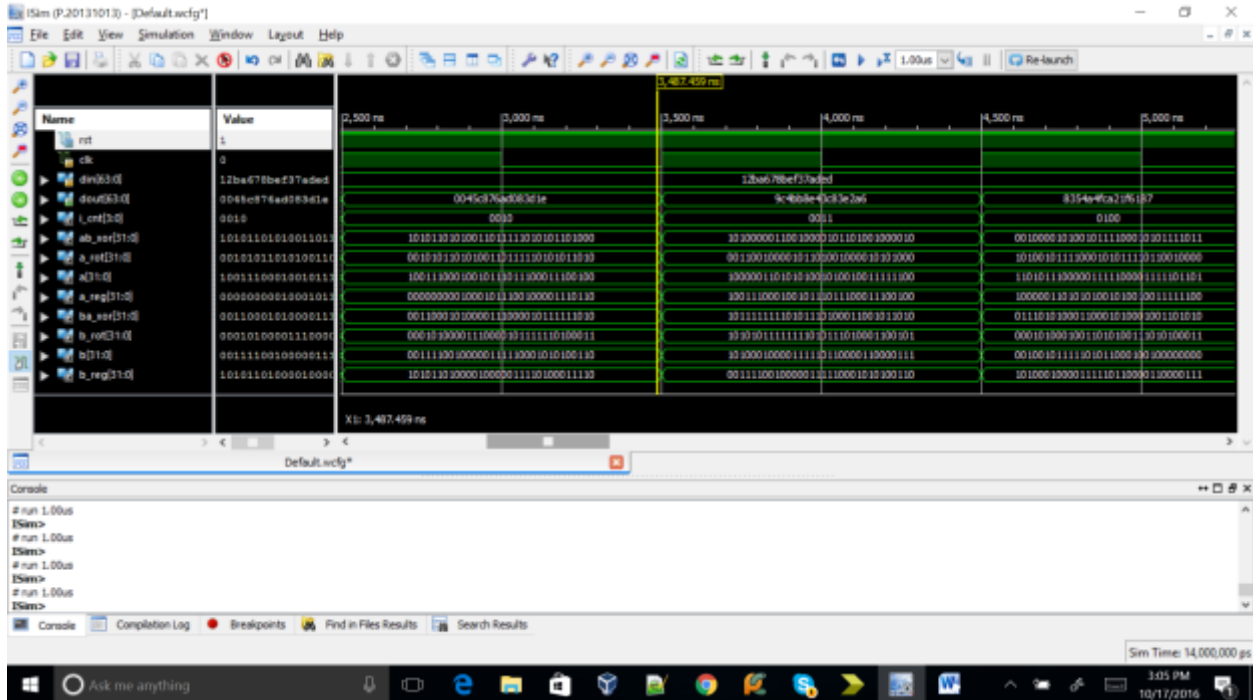
```



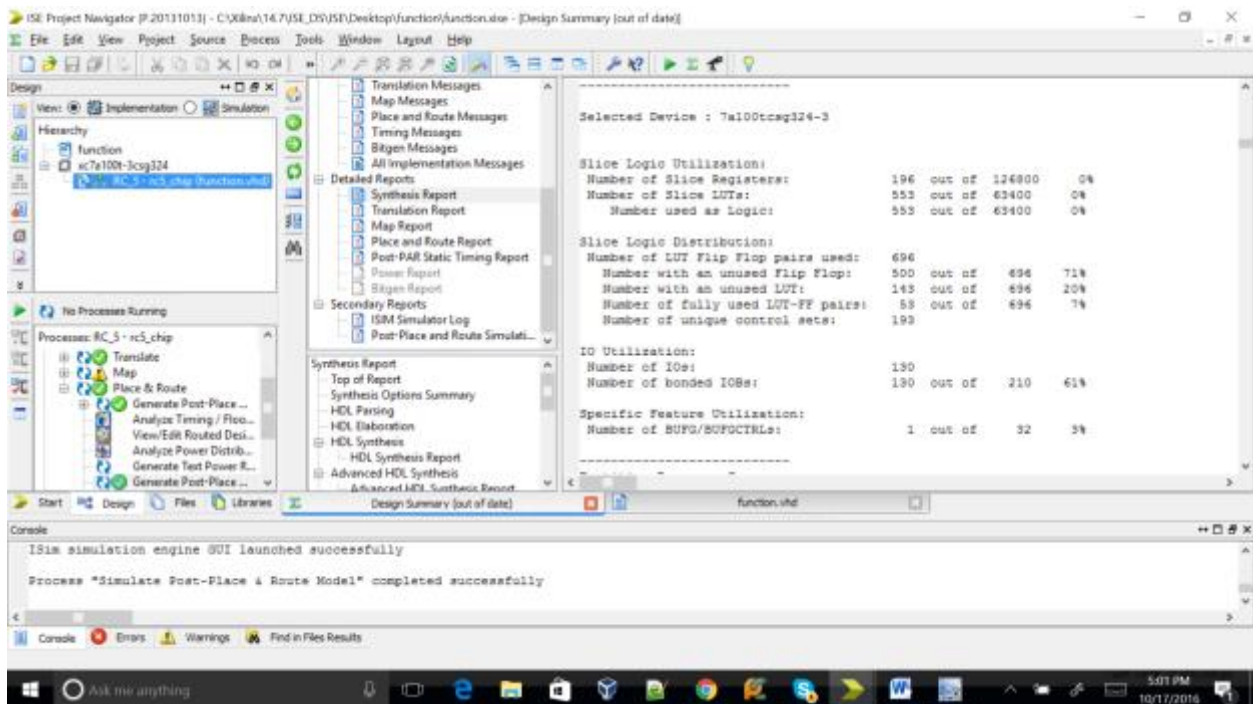
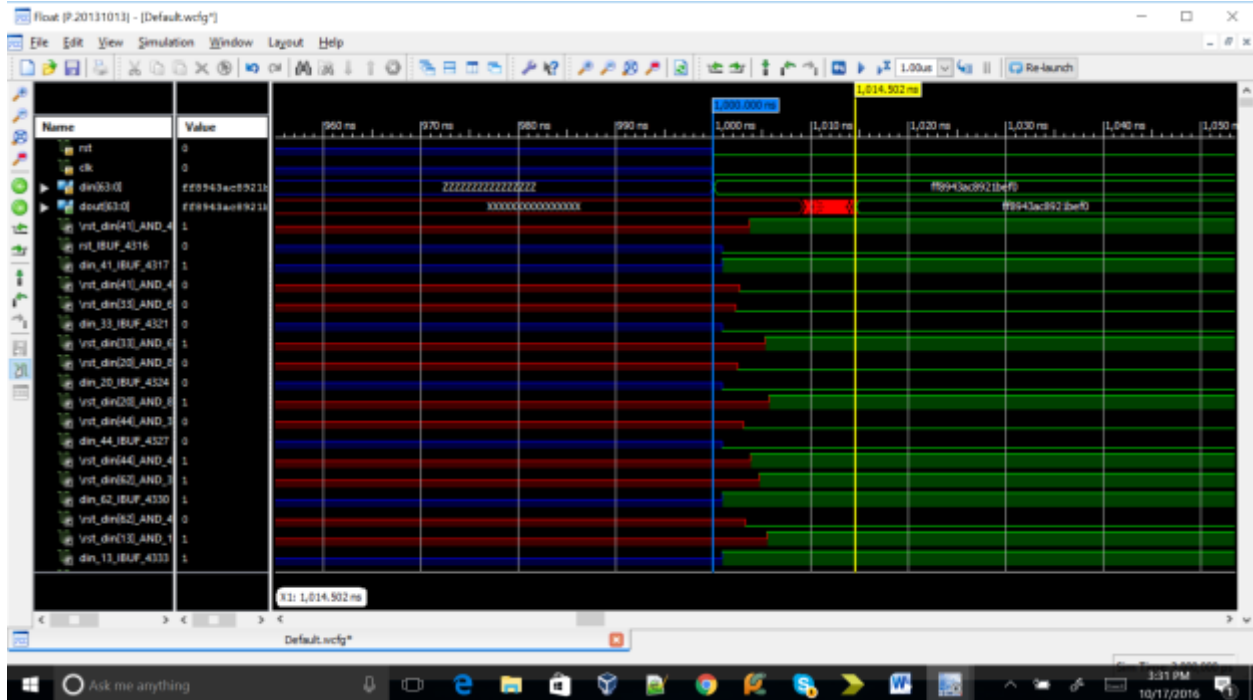
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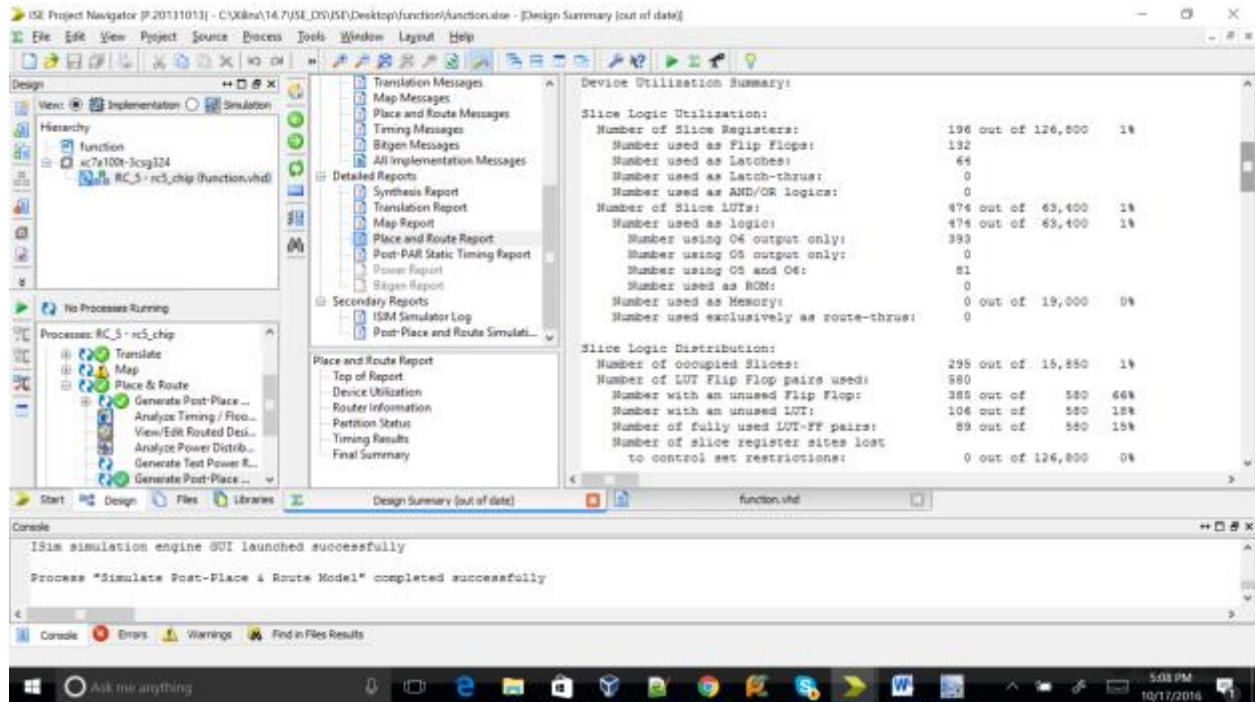


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The device utilization in post place route phase is less as only required number of gates and circuit is used as compared to the synthesis report.

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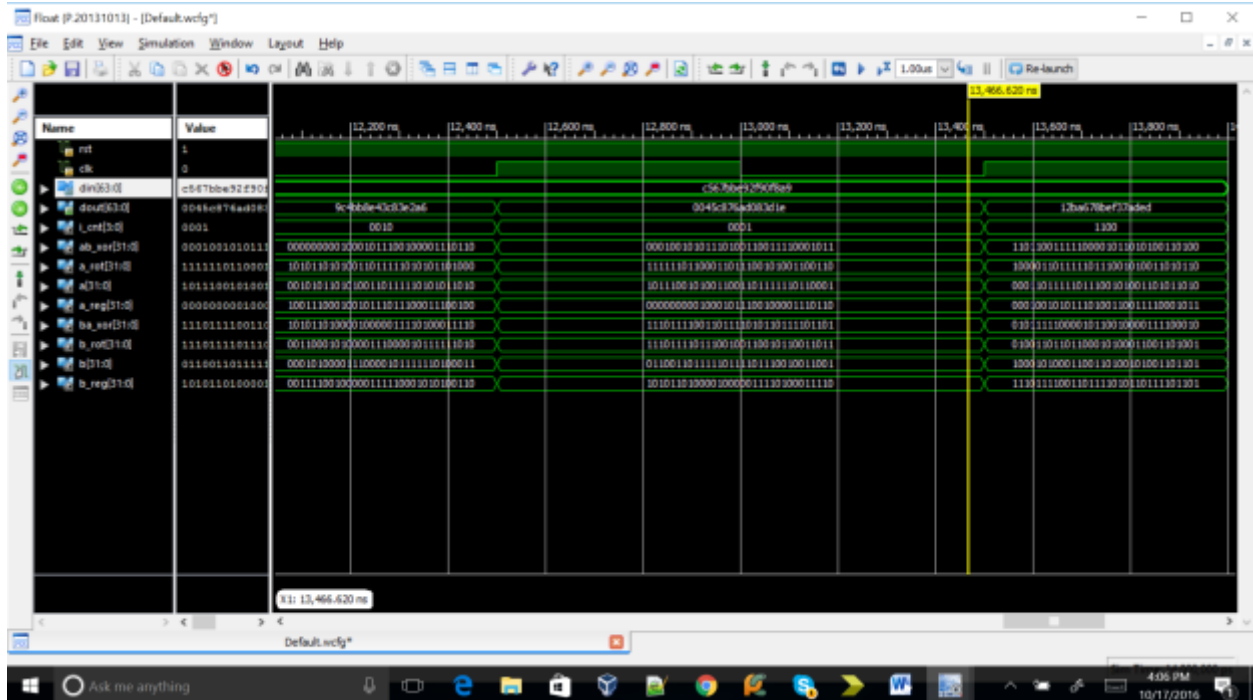
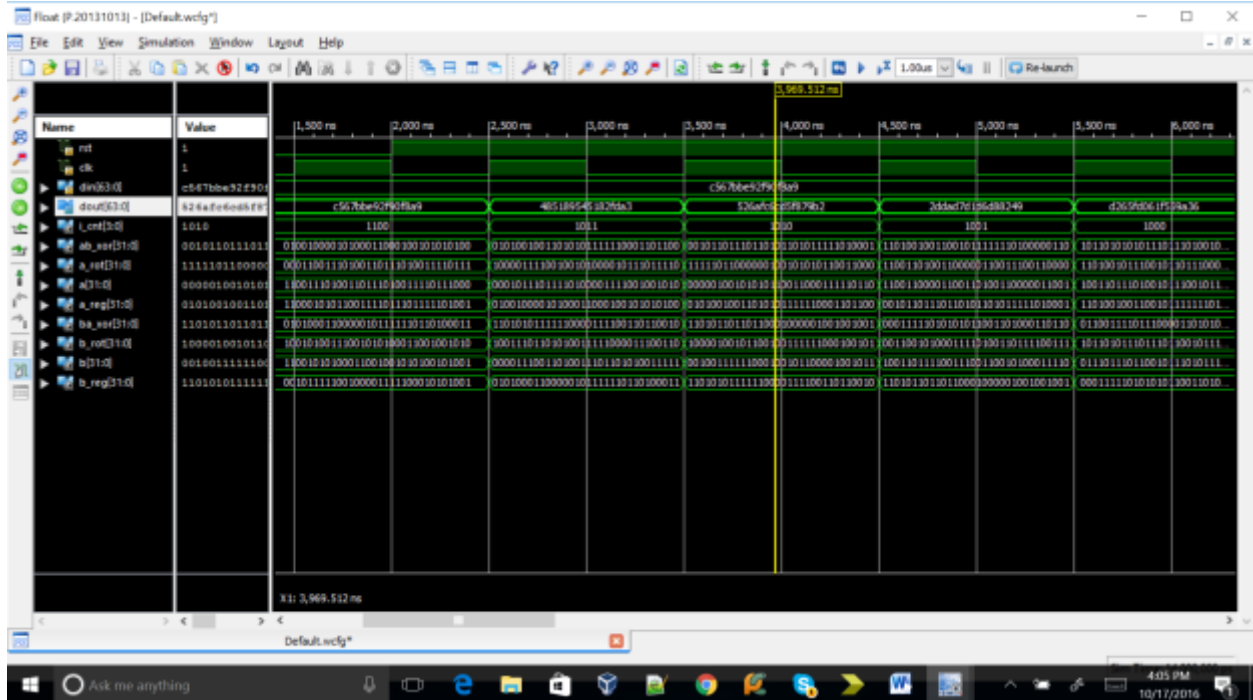
Total delay is 14.502 ns.

Latency is 13 clock cycles

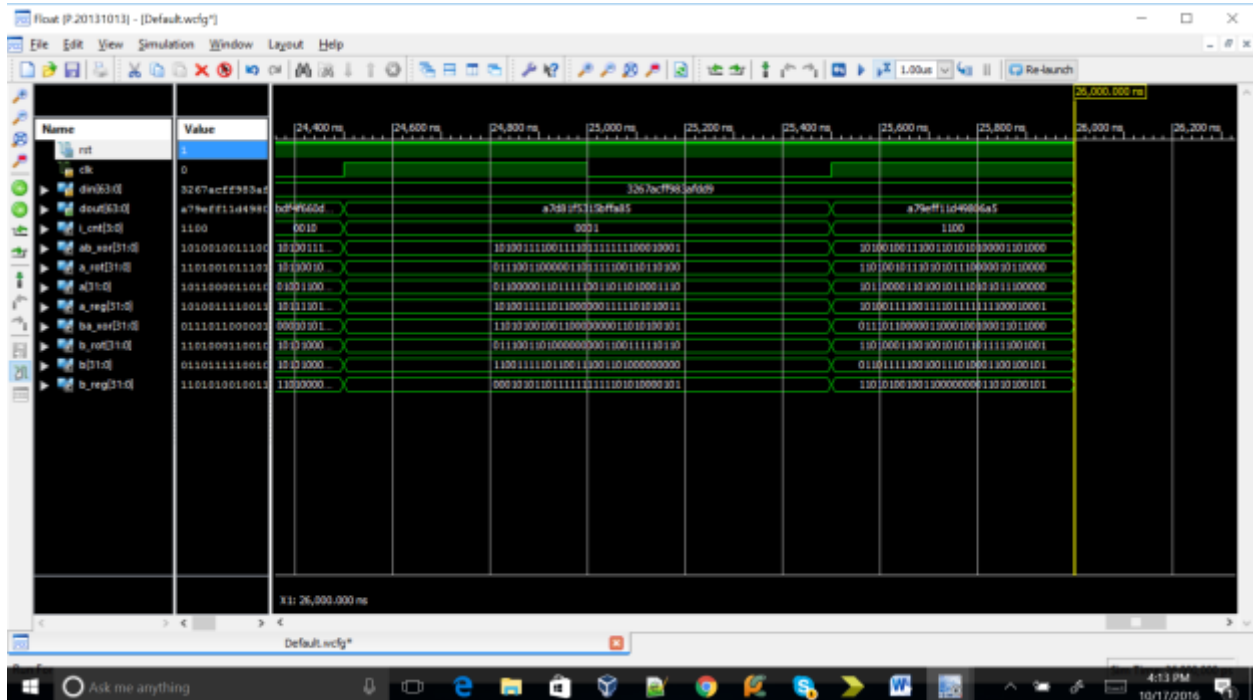
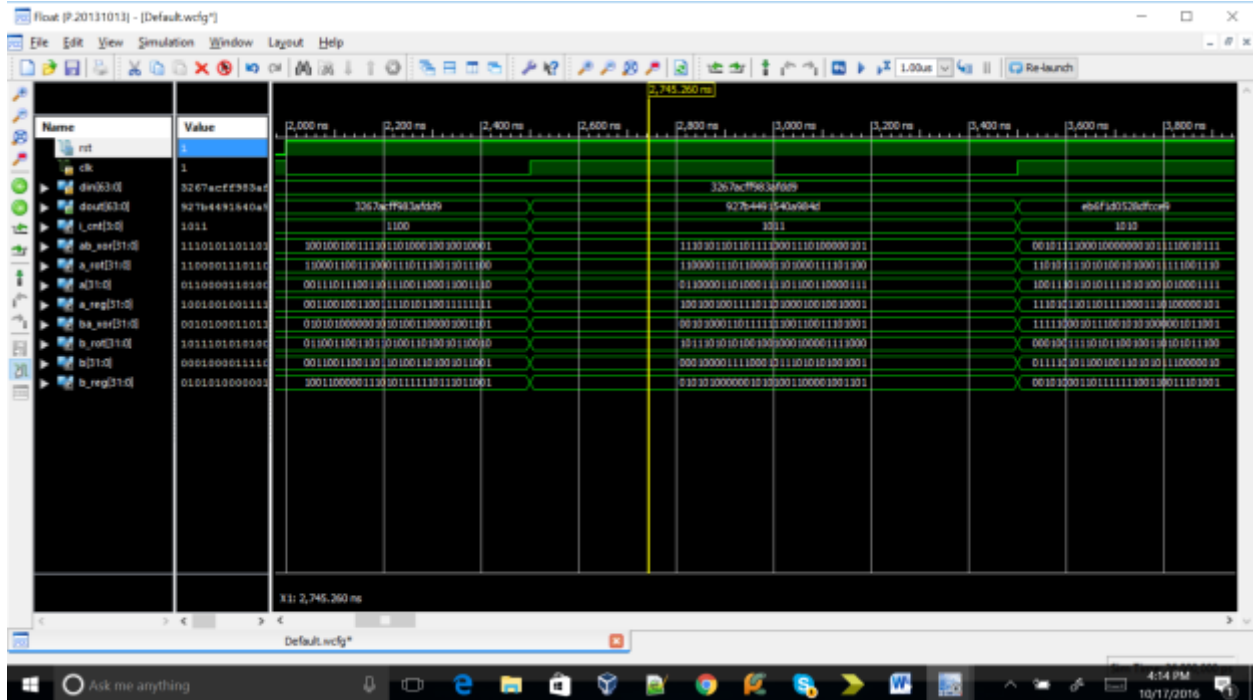
Max clock frequency 127.087MHz

Critical path delay is 1.123 us

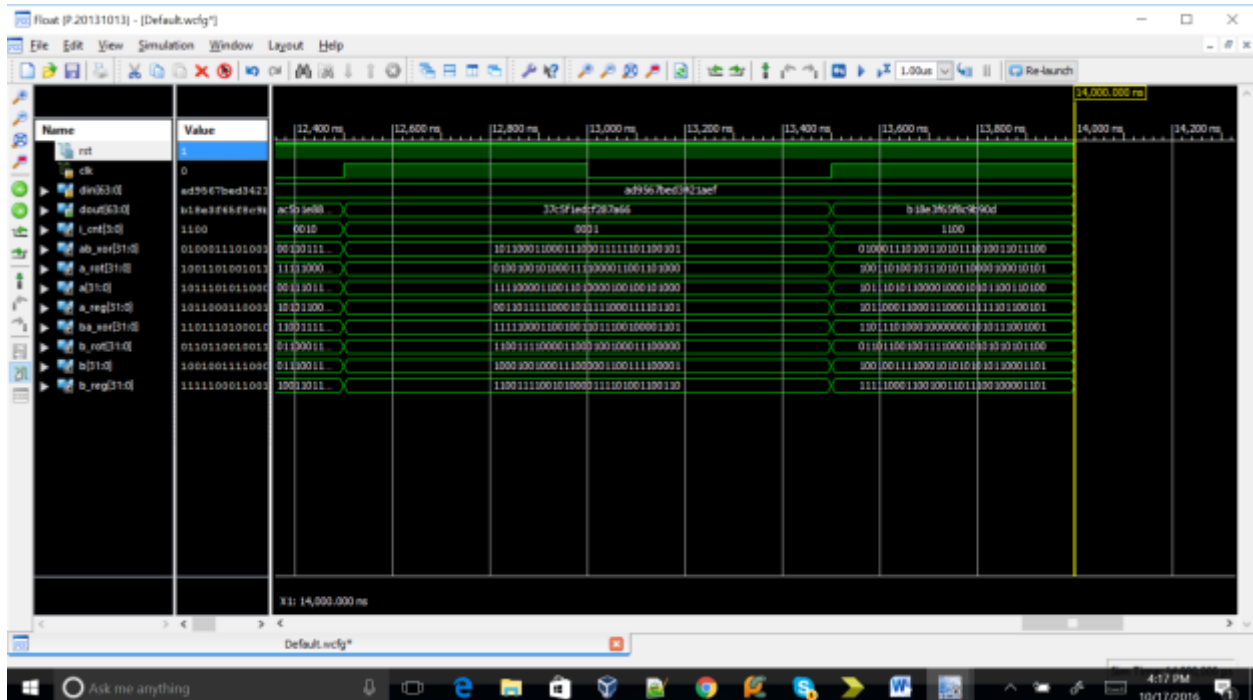
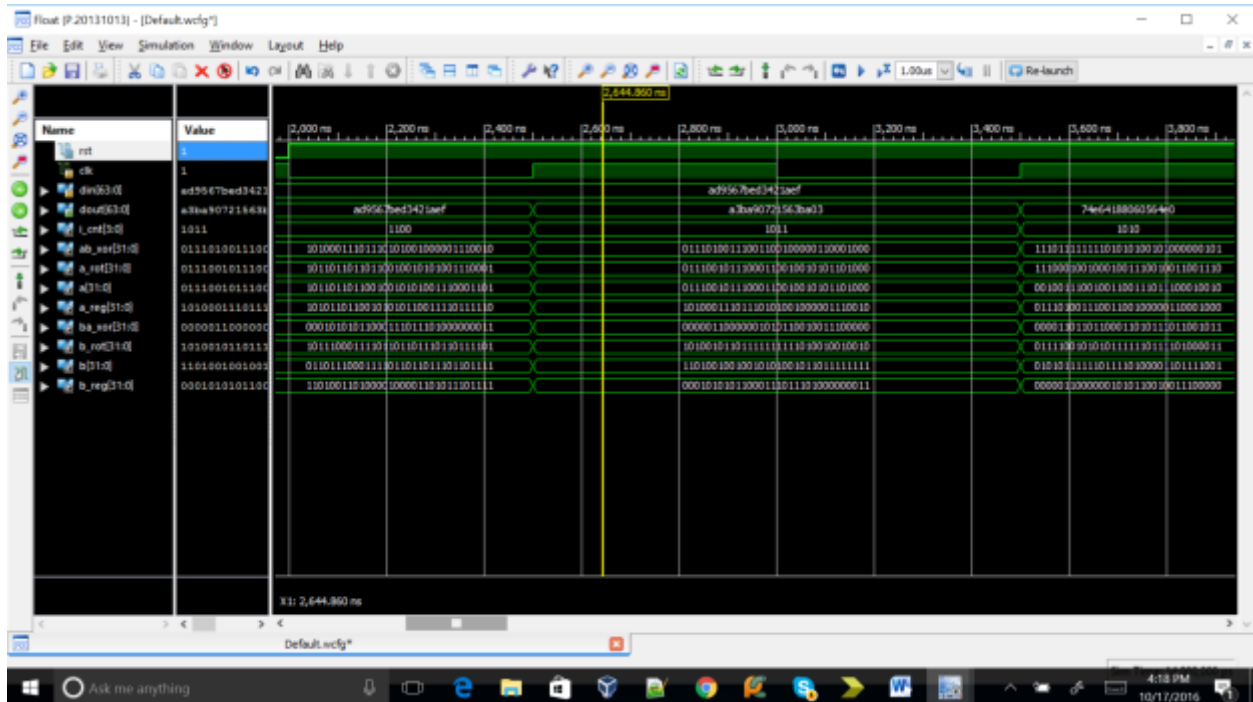
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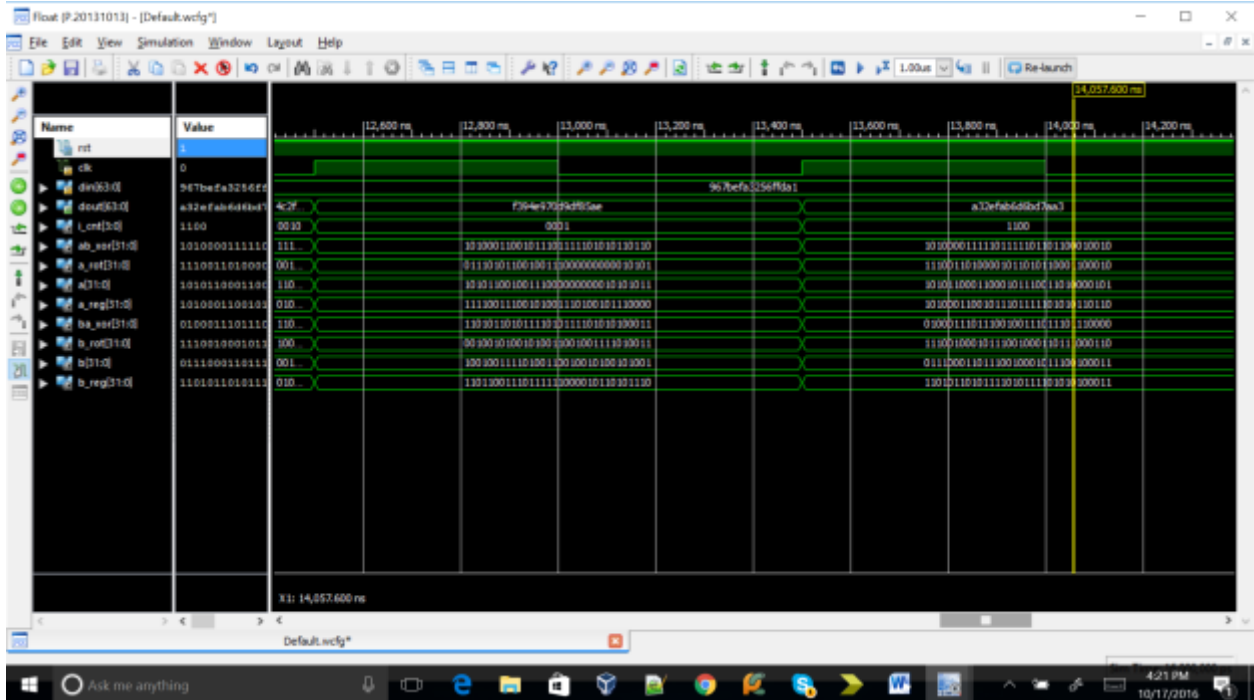
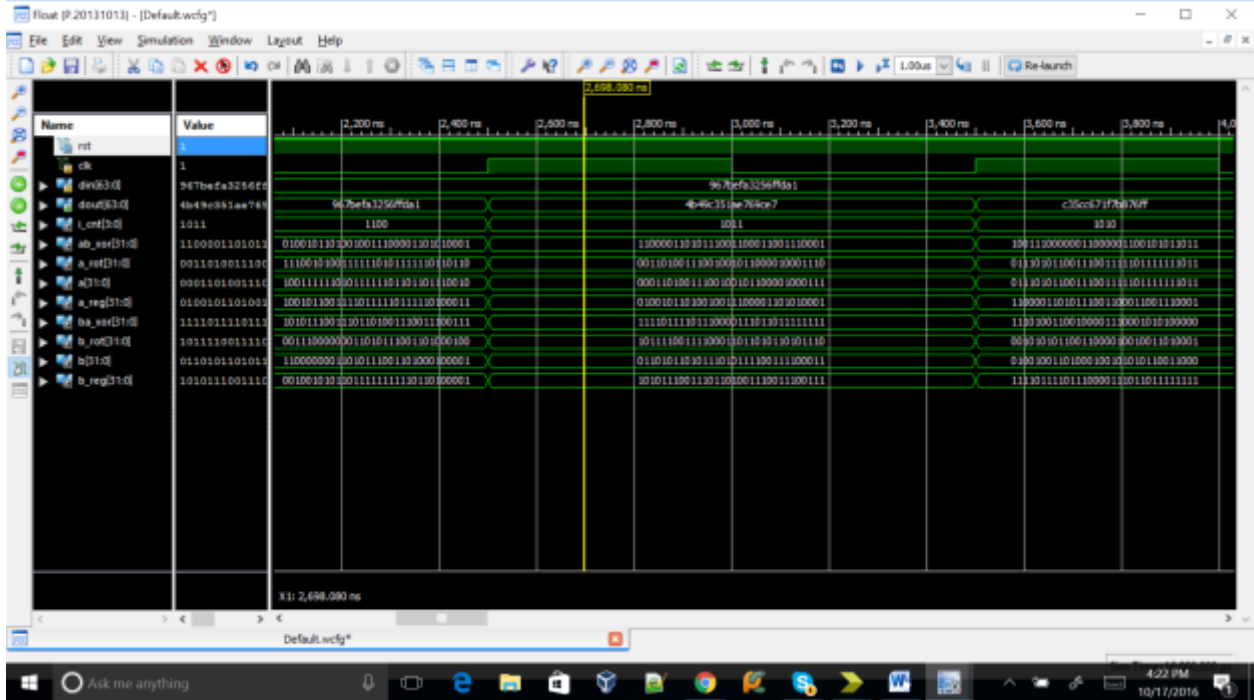
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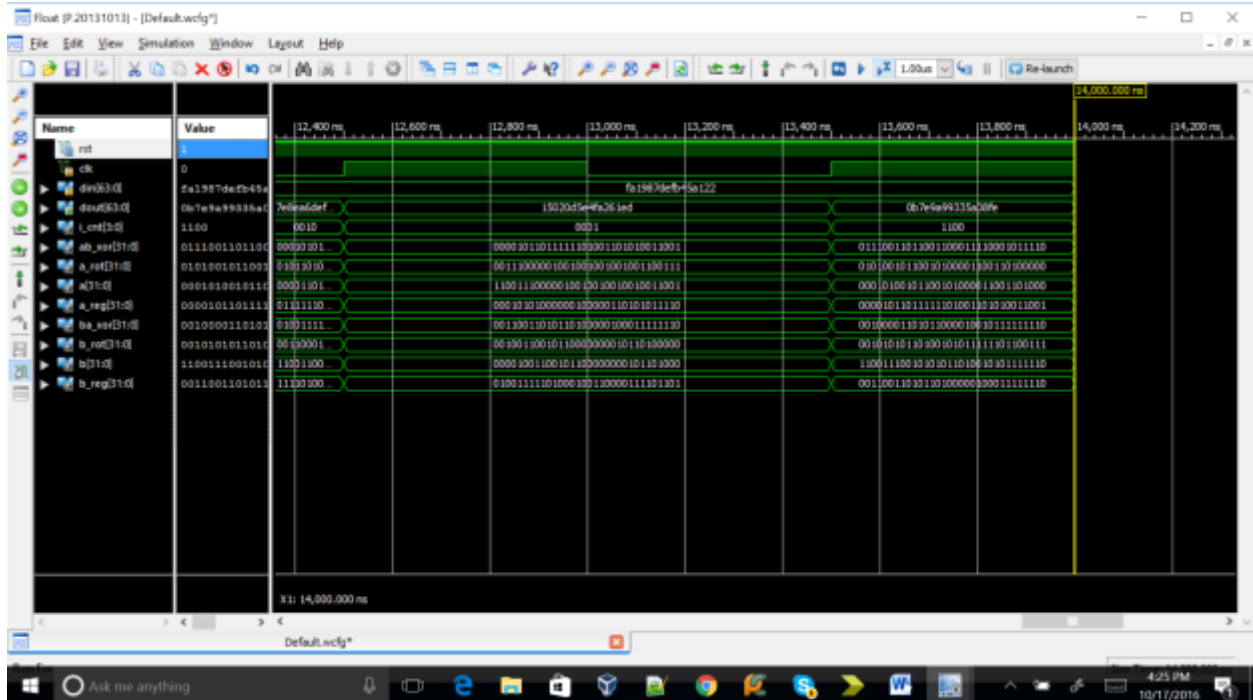
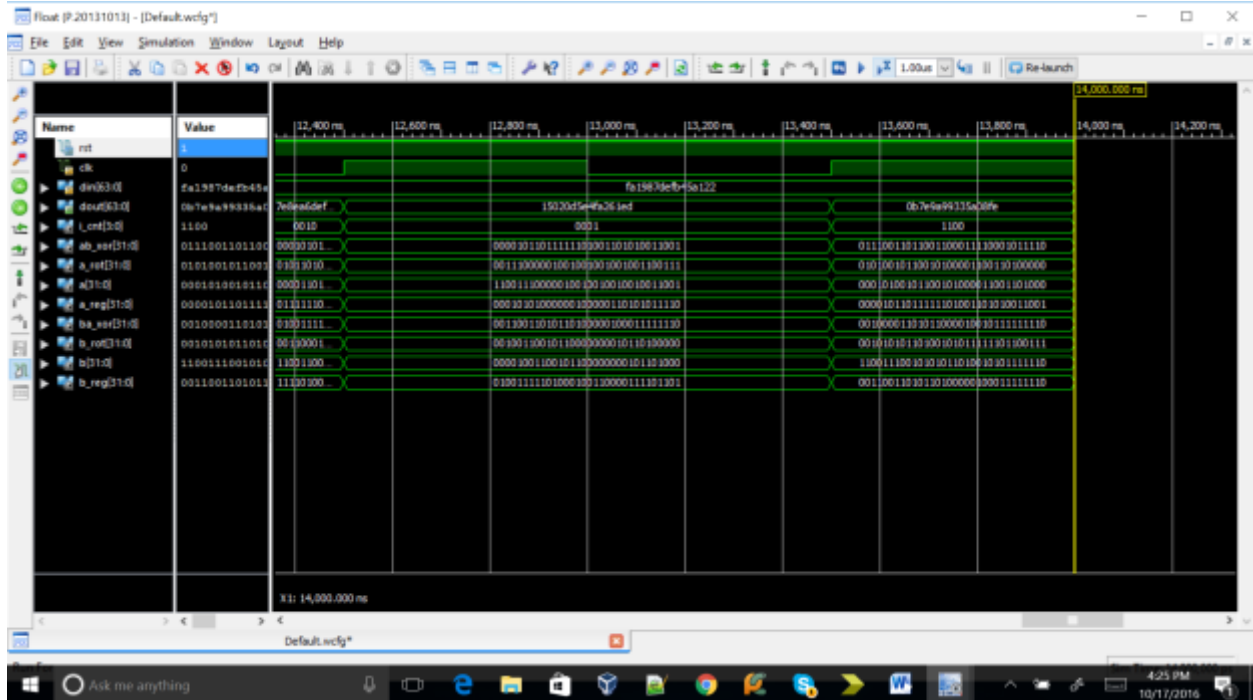
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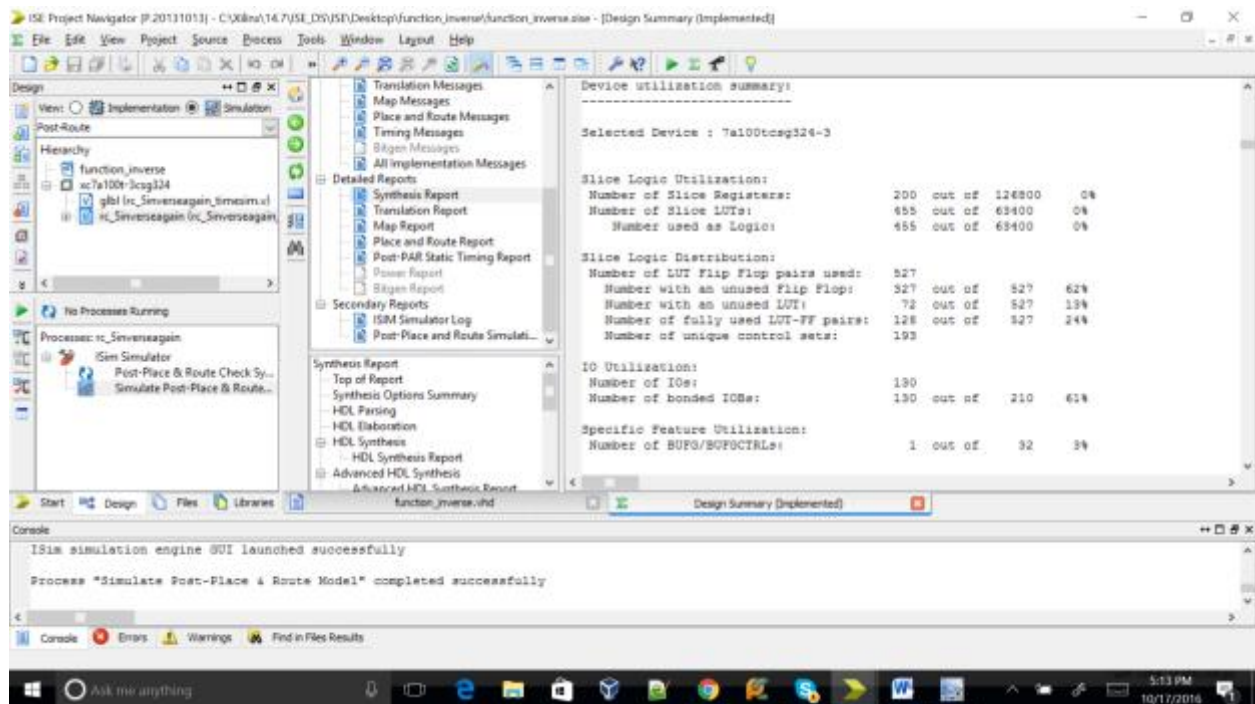
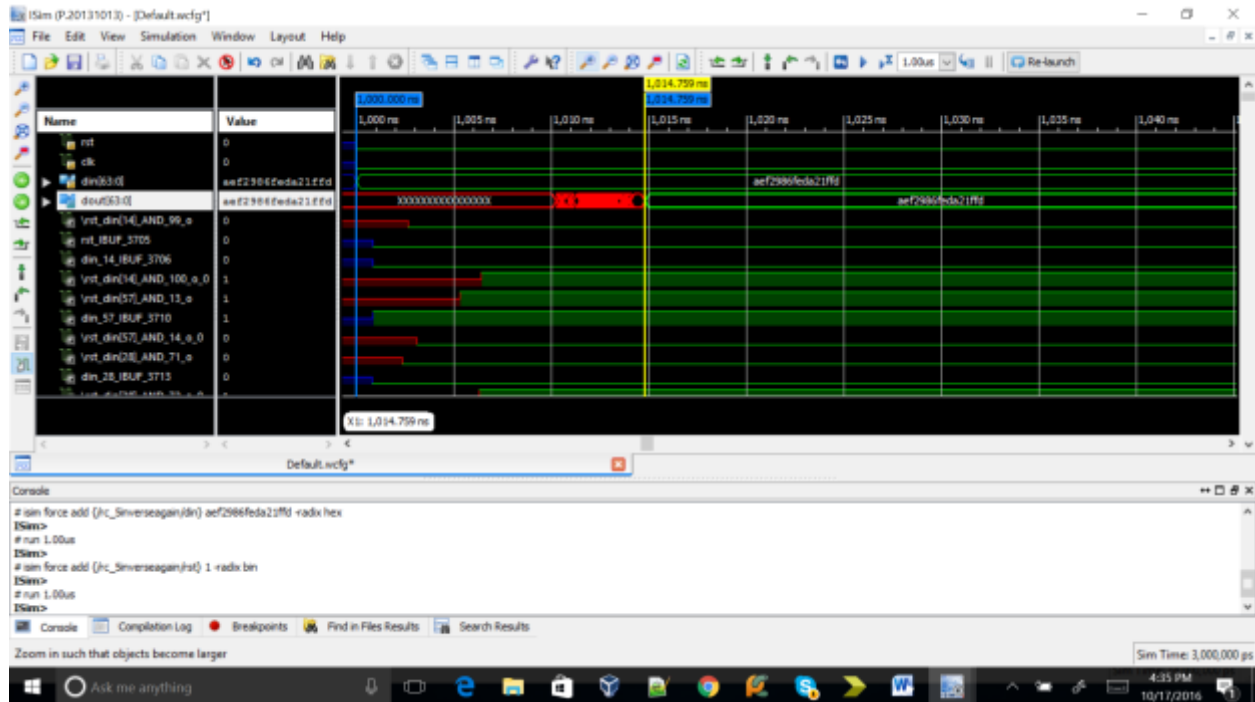
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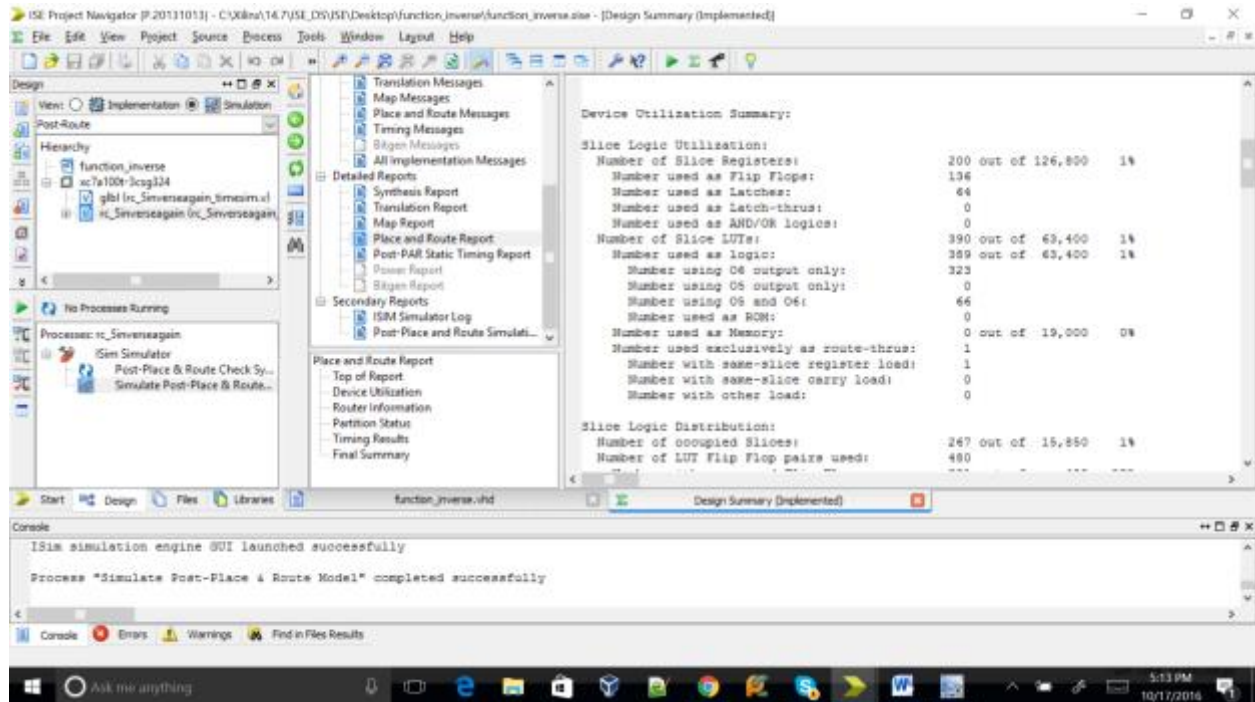


The device utilization in post place route phase is less as only required number of gates and circuit is used as compared to the synthesis report.

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Total delay is 14.759 ns.

Latency is 13 clock cycles

Max clock frequency 172.454 MHz

Critical path delay is 1.241 us

<https://youtu.be/-tOYTFvQCXk>