EE 709 - Take Home exam.

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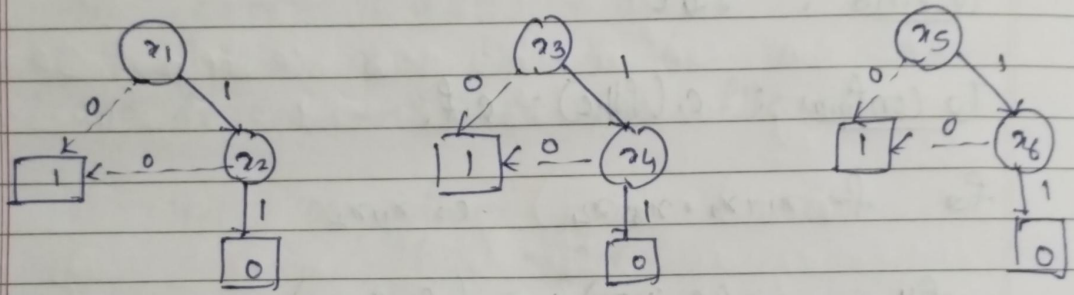
Q.1 Building blocks.

1] ROBDD ⇒

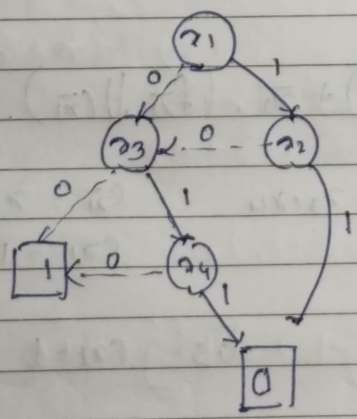
$f(x_1, x_2, x_3, x_4) = (\sim(x_1 . x_2)) . (\sim(x_3 . x_4)) . (\sim(x_5 . x_6))$

f_1 f_2 f_3

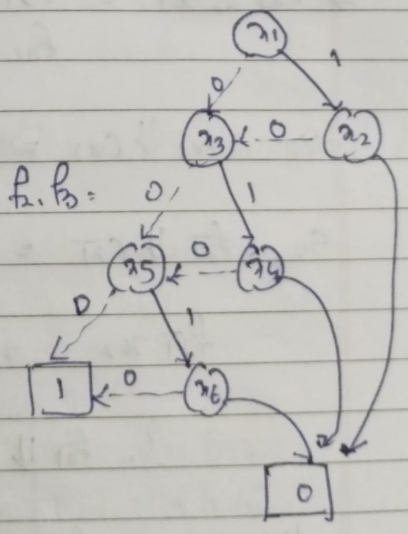
$f_1 = \sim(x_1, x_2)$ $f_2 = \sim(x_3, x_4)$ $f_3 = \sim(x_5 . x_6)$



$f_1 . f_2 = (\sim(x_1, x_2)) . (\sim(x_3, x_4))$



$f = f_1 . f_2 . f_3 =$



Ans ⇒

Building Block.

2] The IF-else ROBDD and the ROBDD obtained in part ① both are same.

3] Given : $f = x_1 + x_2 + x_3 + x_4$ $\quad c = x_1 + x_2$

$c \neq 0$

To find : $f \Downarrow c$

To confirm : $c.(f \Downarrow c) = c.f$

for $f = x_1 + x_2 + x_3 + x_4 \quad c = x_1 + x_2$

$$f \Downarrow c = x.(f_x \Downarrow \bar{x}) + \bar{x}.(f_{\bar{x}} \Downarrow c_{\bar{x}})$$

$x = x_1$

$$f \Downarrow c = x_1.(f_{x_1} \Downarrow c_{x_1}) + \bar{x_1}.(f_{\bar{x_1}} \Downarrow c_{\bar{x_1}}).$$

$\Rightarrow f_{\bar{x_1}} \Downarrow c_{\bar{x_1}}$ ∘ $f_{\bar{x_1}} = x_2 + x_3 + x_4 \quad c_{\bar{x_1}} = x_2$

$f_{x_1} = 1 \quad c_{x_1} = 1$

So $f_{x_1} \Downarrow c_{x_1} = f_{x_1} = 1$ as $c_{x_1} = 1$

So $f_{\bar{x_1}} \Downarrow c_{\bar{x_1}} = f_{\bar{x_1} x_2} \Downarrow c_{\bar{x_1}} c_2$ as $c_{\bar{x_1}} \bar{x_2} = 0$

$f_{\bar{x_1}} x_2 = 1 \quad c_{\bar{x_1}} c_2 = 1$

$\therefore f_{\bar{x_1}} \Downarrow c_{\bar{x_1}} = 1$

Hence $f \Downarrow c = x_1.1 + \bar{x_1}.1 = 1$

Ans $\boxed{f \Downarrow c = 1}$

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$c.(f \| c) = 0$ for $c = 0$

$= f \| c$ for $c \neq 0$

$c.f = 0$ for $c = 0$

f for $c = 1$

so for $f = x_1 + x_2 + x_3 + x_4$ and $c = x_1 + x_2$

for $c = 0$ $\quad c.(f \| c) = c.f$

and for $c = 1 \rightarrow f = 1$ and $f \| c = 1$

Here. We confirm

$$c.(f \| c) = c.f$$

8.4 Building Blocks

CNF representation :-

$j = a + g \quad g = \bar{f} \quad f = b.c \quad i = \overline{g + h}$

$h = \overline{f.(d.e)}$

$j = a + g = a + \bar{b}.\bar{c} = a + \bar{b} + \bar{c}$ ← demorgan's law

$h = \overline{b.c.d.e} = \bar{b} + \bar{c} + \bar{d} + \bar{e}$

$i = b.c.d.e$

$i = b.c.d.e$	$f = b.c$
$j = a + \bar{b} + \bar{c}$	$g = \bar{b} + \bar{c}$
$h = \bar{b} + \bar{c} + \bar{d} + \bar{e}$	

Q.5 Building Blocks.

as we can clealy see that. we can't find any input combination for which.

$$j = i = h$$

as $i = \bar{h} \cdot bc \cdot d \cdot e$

we can confirm this with the help of SAT package. by writing a CNF for.

$$(h = i) \wedge (i = j).$$

CNF $(h \Leftrightarrow i) \wedge (i \Leftrightarrow j) \wedge (h \Leftrightarrow \overline{b \cdot c \cdot d \cdot e}) \wedge (i \Leftrightarrow bc \cdot d \cdot e) \wedge (j \Leftrightarrow (a + b\bar{c}))$.

$(h + \bar{i}) \cdot (\bar{i} + \bar{h}) \cdot (i + \bar{j}) \cdot (\bar{i} + j) \cdot (\bar{h} + \bar{b} + \bar{c} + \bar{h} + \bar{e})$.
$(b + h) \cdot (h + c) \cdot (h + d) \cdot (h + e)$
$(\bar{c} + b) \cdot (\bar{i} + c) \cdot (\bar{i} + d) \cdot (\bar{i} + e)$.
$(i + \bar{b} + \bar{c} + \bar{d} + \bar{e})$
$(j + a + \overline{b \cdot c}) (\bar{j} + a + \bar{b} + \bar{c})$.

$(j + \bar{a}(b + c)) \Rightarrow (j + \bar{a}) \cdot (j + b + c)$

and with the help of SAT package we can see that the output is

UNSATISFIABLE

i.e. the output is always = 0 i.e. no input combination exists for

$$h = i = j$$

Q.2 Verification of combinational circuit.

Specification	Implementation
$e = u_3 + \bar{u_3}u_2 + \bar{u_3}\bar{u_2}u_1 + \bar{u_3}.\bar{u_2}.\bar{u_1}.u_0$	$e = u_3 + u_2 + u_1 + u_0$
$c_0 = u_3 + \bar{u_3}.\bar{u_2}u_1$	$c_0 = u_3 + u_1$
$c_1 = u_3 + \bar{u_3}.u_2$	$c_1 = u_3 + u_2$

input combinations. (at most input is 1).

u_3	u_2	u_1	u_0	case condn
0	0	0	0	
0	0	0	1	$c = \sim u_3.\sim u_2.\sim u_0 +$
0	0	1	0	$\sim u_0.\sim u_1.\sim u_2 +$
0	1	0	0	$\sim u_2.\sim u_3.\sim u_1 +$
1	0	0	0	$\sim u_0.\sim u_1.\sim u_3.$

⇒ 1] We can check the implementation is equivalent to specification by checking ROBDD's of

(speci).c == (impl).c. (using == operator).

or we can directly (xor) both the ROBDD's and we will get ROBDD 'zero' if they are same.

⇒ 2] We can check the Implementation is equivalent to specification by checking the SAT output.

We can make a CNF for.

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(e_imp XOR e_spec) . C
(C0 imp XOR espec) . C
(C1 imp XOR espec) . C

for any imp ≠ spec and the input is core (c) the output is 'one'.

So for SAT solver we can say that if we get 'UNSATISFIABLE' i.e. there is no input combination for

(eimp XOR espe) . C = 1

i.e. eimp = espec for c = 1

We can make the CNF by making new variables to the product term and writing the equivellance relation ship for the new variable and the corresponding product term.

for example

$C = \bar{v}_3 . \bar{v}_2 . \bar{v}_1 + \bar{v}_3 . \bar{v}_2 . \bar{v}_0 + \bar{v}_3 . \bar{v}_0 . \bar{v}_1 + \bar{v}_0 . \bar{v}_2 . \bar{v}_1$

new var: d_1 d_2 d_3 d_4

$(d_1 + d_2 + d_3 + d_4)\ (d_1 \Leftrightarrow \bar{v}_3 . \bar{v}_2 . \bar{v}_1)\ (d_2 \Leftrightarrow (\bar{v}_3 . \bar{v}_2 . \bar{v}_0$
$(d_3 \Leftrightarrow \bar{v}_3 . \bar{v}_0 . \bar{v}_1)\ (d_4 \Leftrightarrow (\bar{v}_0 . \bar{v}_2 . \bar{v}_1$

and further expanding $(d_1 \Leftrightarrow \bar{v}_3 . \bar{v}_2 . \bar{v}_1)$ to POS as

$(\bar{d}_1 + \bar{v}_3 . \bar{v}_2 . \bar{v}_1) . (d_1 + v_3 + v_2 + v_1)$.

distributive law $(\bar{d}_1 + \bar{v}_3) . (\bar{v}_1 + \bar{v}_2) . (\bar{d}_1 + \bar{v}_1)$.

In the similar manner we can find the CNF of all the imp and spec and check whether the output is always '0'

i.e. UNSATISFIABLE, & SAT output.

Q.3 Verification of sequential circuits.

Q1 Using ROBDD.

as we need to inform that this machines give same output i.e. z=0 upto k=6

We can consider 4 input (x) and 4 input (y)
⇒ x(k) and y(k) are in-put for t=k.

Now for each state t=k we have its inputs and its corresponding states with the help of this we can construct an ROBDD of the output for t=k.

and finally we need to chek whether the outputs of state machin A and machine B for all k= are same.

i.e. f(k) ⇒ output state machine A or 1
g(k) ⇒ output state machine B or 2

it should satisfy.

$$(F(0) \oplus g(0)) + (F(1) \oplus g(1)) + (F(2) \oplus g(2))$$
$$+ (F(3) \oplus g(3)) + (F(4) \oplus g(4)) = 0$$

Q.2 Using SAT

We want to check for $k = 4$

$f_1 \oplus g_1$ ∴ $f_2 \oplus g_2$ $f_3 \oplus g_3$ $f_4 \oplus g_4$

Should be '0' as f_- and g_- should be same.

So we can build the BMF for $f_k \oplus g_k$ and check whether it is '0' always for all the inputs.

We should get the output of SAT Package as 'UNSATISFIABLE' if $f_k = g_k$.

We check the $f_k \oplus g_k$ iteratively and we got $f_1 \neq g_1$ it gets satisfied.

The machine ① and machine ② are ~~not~~ different. because of

$$S_3(k+1) = x(k) \;?\; 0 : (x(k) \;?\; S_2(k) : S_0(k))$$

The machine ① matches machine ②.

for $S_3(k+1) = x(k) \;?\; (1 : x(k) \;?\; S_2(k) : S_0(k))$.

Q.6 Part (1) Building Blocks

a) The list of states corresponding to the binary structure representation of this machine.

x, d, q, y (q = y)

i) 0, 0, 0, 0
ii) 0, 0, 1, 1
iii) 0, 1, 0, 0
iv) 0, 1, 1, 1
v) 1, 0, 0, 0
vi) 1, 0, 1, 1
vii) 1, 1, 0, 0
viii) 1, 1, 1, 1

b) The state can be represented as q(k), y(k), x(k), d(k)