**ADDRESSING MODES**

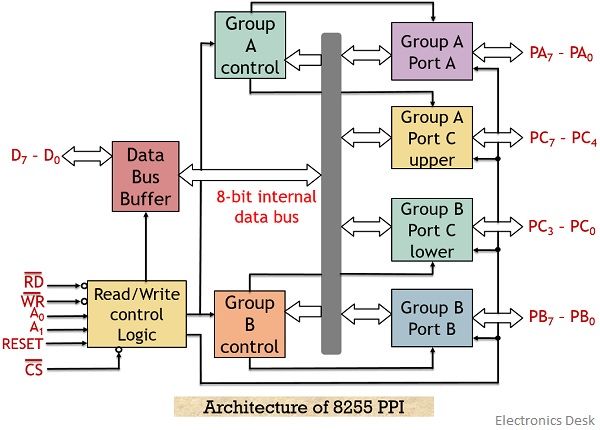
* **Register addressing mode**: MOV AL, CL (register, register)
* **Immediate addressing mode**: MOV AX, 2000 (register, data)
* **Direct addressing mode:** MOV CL, [4321] (register, offset)
* **Memory indirect addressing mode**: MOV AL, [SI/BX/DI] (register, offset in SI, BX or DI with DS or ES as default segments)
* **Memory based addressing mode**: MOV AL, [BX/BP] (, with offset in base register BX or BP with DS as default segment)
* **Memory indexed addressing mode**: MOV AL, [SI/DI] (register, offset in index register SI or DI with DS and ES as default segments respectively)
* **Based indexed addressing mode**: MOV CL, [BX, SI] (register, offset as sum of contents of base register and index register)
* **Relative based addressing mode**: MOV CH, [BX+ IMMEDIATE\_VALUE] (register, offset as sum of content of base register and some immediate value)
* **Relative indexed addressing mode**: MOV CH, [SI+ IMMEDIATE\_VALUE] (register, offset as sum of content of index register and some immediate value)
* **Relative base index addressing mode**: MOV CH, [BX+SI+IMMEDIATE\_VALUE] (register, offset as sum of contents of base and index registers and some immediate value)
* **Implicit addressing mode**: CMA (only opcode)

**INTERRUPT VECTOR TABLE**

* 1kb of memory of 8086 is reserved for interrupt vector table, which holds the desired addresses for various interrupt service routines.
* 4-bytes are required to store address of one routine, therefore, addresses to 256 such interrupt routines can be accommodated in the interrupt vector table.

**8255 PROGRAMMABLE PERIPHERAL INTERFACE (PPI)**

* 40 pin IC.
* Used for transmission of data between microprocessor and peripherals.



* The RD’ and WR’ signals configure the 8255 to read or write data.
* CS’ is the chip select signal.
* A0 and A1 together work in order to select which port is to be used.
* PORT A and B contain an 8-bit address and an 8-bit data buffer.
* PORT C is divided into 2 groups i.e., group A and group B, further known as C upper and C lower i.e., 4-bit upper address and data buffer and 4-bit lower address and data buffer.
* **Data Bus Buffer** is connected to the data bus of 8086. It is responsible for the transmission of data.
* **RESET** clears the control register and all the ports are configured for receiving input.

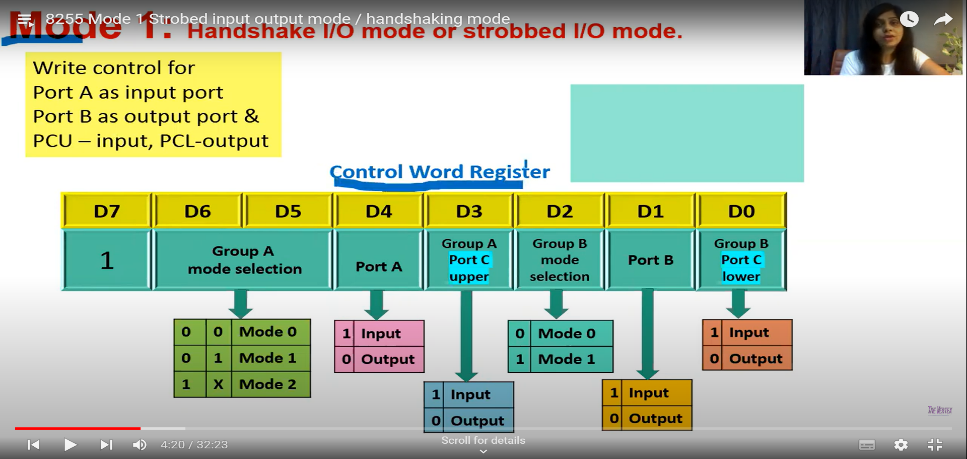
**MODES OF 8255**

* + Operates in two modes: BSR (Bit SET/RESET), and I/O mode.
  + D7 of control word register decides the mode that it operates in i.e., 0 for BSR and 1 for I/O.

**BSR MODE**

* + Only for PORT C.
  + D4-D6 are don’t care bits i.e., play no role.
  + D1-D3 bits decide which pin of PORT C is to be selected.
  + D0 bit decide if the selected pin is to be SET (1) or RESET (0).

**I/O MODE**

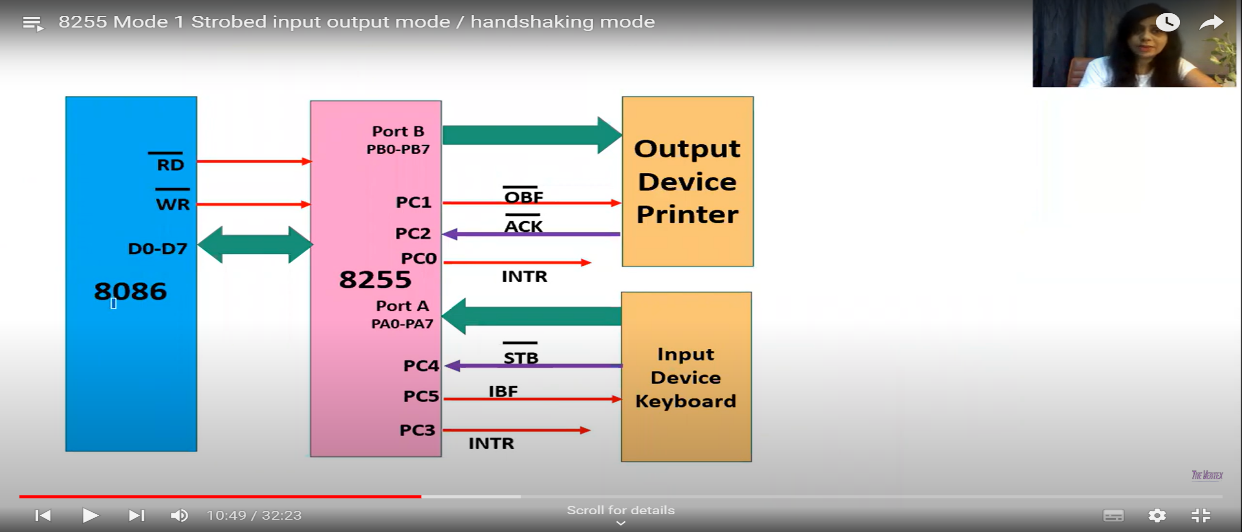
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**MODE 0**

* Simple I/O mode.
* Only output is latched.

**MODE 1**

* Both input and output are latched.

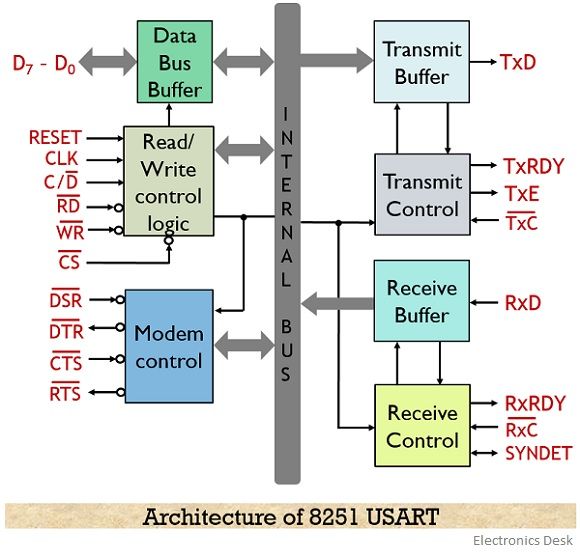
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**MODE 2**

* Only PORT A can be programmed in this mode.
* PORT C serves for handshaking signals.
* Both input and output are latched.
* PORT B can be configured either in mode 0 or 1.
* Transmission procedure stays the same as in Mode 1.

**USART (UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER)**

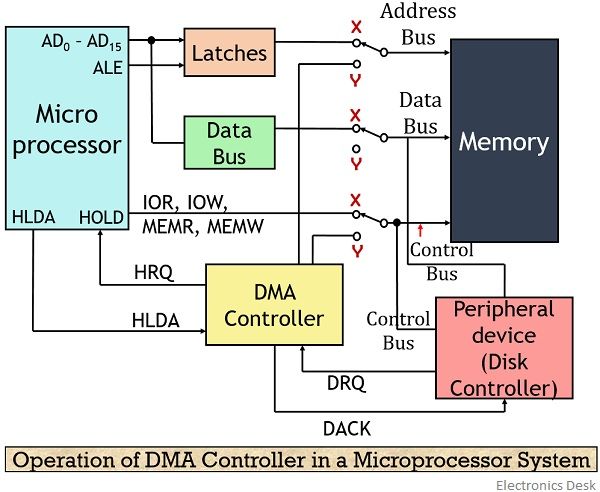
* 28 pin IC.
* Converts parallel data to serial and vice-versa.



* [**https://electronicsdesk.com/8251-usart.html**](https://electronicsdesk.com/8251-usart.html)

**8257 DMA CONTROLLER**

* 40 pin IC.
* It consists of 4 channels that can be utilized over 4 input/output devices.
* All of the 4 channels can be separately programmed.
* All the 4 channels hold the 16-bit address and 14-bit counters individually.
* The permissible data transfer is up to 64 KB.

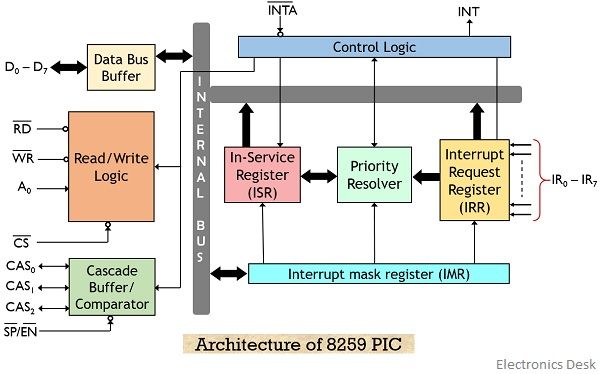


**MEMORY INTERFACING**

* Multiple memory chips can be connected with a microprocessor system. Hence, it becomes necessary to have a way as to select the right portion in memory. How the various memory chips are connected and how they are accessed by the microprocessor is what memory interfacing means.
* Microprocessor does so by sending a chip select signal to the required memory chip as some combinational output via a decoder.

**8259**

* Data buffer transfers and receives control word information and interfaces 8259 with the data bus of 8086.
* Read and write logic block generates control signals.
* Control logic register holds the control word.
* IMR contains bits which determine if an interrupt is to be masked or not.
* IRR contains bits which determine which interrupt requests are being made.
* ISR contains bits which determine which interrupt request is being served currently.
* Priority resolver checks and decides which interrupt request is to be served first.
* Cascade buffer/comparator displays its functionality when the 8259 is working in master-slave mode i.e., IRR rather than being connected to individual devices is connected further with other 8259s. This increases the interrupt handling capability.

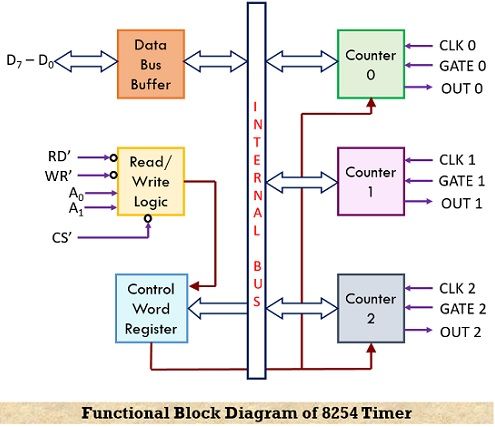


* [**https://electronicsdesk.com/8259-programmable-interrupt-controller.html**](https://electronicsdesk.com/8259-programmable-interrupt-controller.html)

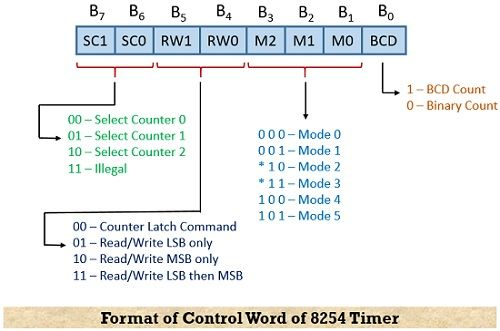
**PROGRAMABLE INTERVAL TIMER/COUNTER – 8254**

* 24 pin IC.
* Has three independent 16-bit counters each capable of handling clock inputs up to 10MHz.
* Operates in 6 modes.
* Has two inputs namely clock and gate, and 1 output i.e., counter.
* Work of 8254 begins with initialization of the control word register preceded by receival of the chip select signal.
* Then a count value is sent to the selected counter and the gate signal is SET.
* With every clock input received, the value of the counter is decremented.
* When the counter reaches 0, an output signal is generated the waveform of which is decided by the mode 8254 is operating in.
* Below is given the combinational inputs for the selection of counters and the CWR.

|  |  |  |
| --- | --- | --- |
| **A1** | **A0** | **DEVICE SELECTED** |
| 0 | 0 | Counter 0 |
| 0 | 1 | Counter 1 |
| 1 | 0 | Counter 2 |
| 1 | 1 | Control word register |



**CONTROL WORD REGISTER**

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* **MODES**

<https://www.youtube.com/watch?v=bvYv_P5Ayxo&list=PLd7ZnpYrrolq6T74tVCuhxlqX_627_Rhy&index=46>

* **INTERFACING WITH 8086**

<https://www.youtube.com/watch?v=qO7_tWY8dYQ&list=PLd7ZnpYrrolq6T74tVCuhxlqX_627_Rhy&index=47>

* **Applications**
  + Generates accurate time delay.
  + Serves as an event counter.s
  + Generates square waves.
  + Can be used as a rate generator.

**8085 addressing modes**

**Register addressing mode MOV A, H //data flow from srg reg to dst reg**

**Immediate addressing mode MVI B, 25 || LXI H, 2500 //data from src val to dst reg**

**Direct addressing mode LDA A, 2500 //src add to dest reg**

**Indirect addressing mode MOV A, M //from mem. add. to which src add points to dest reg**

**Implicit/Implied addressing mode CMA //just data manipulation with no operand specification**