

Reference Manual

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Version

0.1 of 2019/06/13

This is a reference manual for the FPGA system developed for the 32-bit processor named AJIT at IIT Bombay.

Setup Host Machine

Name: AJIT3

IP: 10.107.90.63

VLSI Lab

Directory structure

Directory map of /home/praton/DDP

```
.  
|-- ahir_git  
|-- ahir_release  
|-- AJIT_Linux  
|-- Codes  
|-- level_1.tree  
|-- Trash  
`-- Vivado_Projects
```

VIVADO_PROJECT_PATH = /home/praton/DDP/Vivado_Projects

===== Introduction =====

Current setup is on machine number 63 i.e. AJIT3 in VLSI Lab.

PROJECT_PATH =

Directory structure