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Booting Linux on an FPGA system of AJIT Processor

PRATHU BARONIA , D.Deg, 19, 73 pp.
Department of Electrical Engineering
Indian Institute of Technology Bombay, Powai, Mumbai 400 076.
Supervisor(s): Madhav Desai
External Supervisor(s):

Abstract

This work revolves around developing a FPGA system around AJIT cores and integrating HPC peripherals designed though inhouse and industry standard HLS tools into the system to increase performance of computationally expensive operations. The goal of this project is to boot a custom built OS on the AJIT core and this system will act as the test bed for this. In the first part of the document we focus on the development cycle of the FPGA system where we first describe the processor itself, detailed need of such a system, our setup choices, a telescopic system view, individual block designs and respective design choices made, and the test procedures for the system. In second part of the document we start the discussion on development of a Convolution core using the inhouse HLS tools. Here we discuss the the need of such peripherals which we later on justify through performance metrics also. Later on we discuss how we began designing the peripheral, the design of the internal architecture and subsystems, the choice of design tools and also our test setup. Finally we compare the performance between the hardware and software counterparts of convolutions.

Supervisor's Signature