VLSI Design Project Report
Individual Contribution

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1 HDMI Core

The display of Android 5 screen was shown on the television screen using the ADV7511 HDMI interface in the Zynq evaluation board. A video was also clicked to be as proof. Different specifications and working behind the interfacing is given below.

Display of Android 5 screen :

The audio and the video interface for Android 5 display has been done using the ADV7511 which is a part of the Zynq evaluation board. The ADV7511 is a 225 MHz High-Definition Interface transmitter. The video uses a 16bit YCbCr interface (except VC707 which uses 36bit 444 RGB interface) and the audio uses a single bit SPDIF interface.

It is DVI 1.0-compatible. Since SPDIF is supported, it can carry compressed audio including Dolby Digital, DTA and THX. There is an independent DPDIF input and output.

The HDMI transmitter has 25 connections to Bank 35 (3.3V) of the Zynq-7000 AP SoC.

The needed software is Xilinx and a UART terminal (Tera Term/Hyperterminal) of baud rate 115200 and the required hardware is an HDMI Monitor and the appropraite Zedboard (AC701/KC705/VC707/ZC702/ZC706/Zed board).
Now, we go in depth with the explanation of how the video and audio interfacing is done.

1. The video part consists of a Xilinx VDMA interface and the ADV7511 video interface. The ADV7511 interface consists of a 16bit YCbCr 422 with separate synchorinzation signals. The VDMA streams frame data to this core. The internal buffers of this pcore are small (1k) and do NOT buffer any frames as such. Additional resources may cause loss of synchronization due to DDR bandwidth requirements. The video core is capable of supporting any formats through a set of parameter registers (given below). The pixel clock is generated internal to the device and must be

configured for the correct pixel frequency. It also allows a programmable color pattern for debug purposes. A zero to one transition on the enable bits trigger the corresponding action for HDMI enable and color pattern enable.

2. The audio part consists of a Xilinx DMA interface and the ADV7511 spdif audio interface. The audio clock is derived from the bus clock. A programmable register (see below) controls the division factor. The audio data is read from the DDR as two 16bit words for the left and right channels. It is then transmitted on the SPDIF frame. The sample frequency and format may be controlled using the registers below. The reference design defaults to 48KHz.

The interfacing is shown in detailed labeled block diagram as given below :

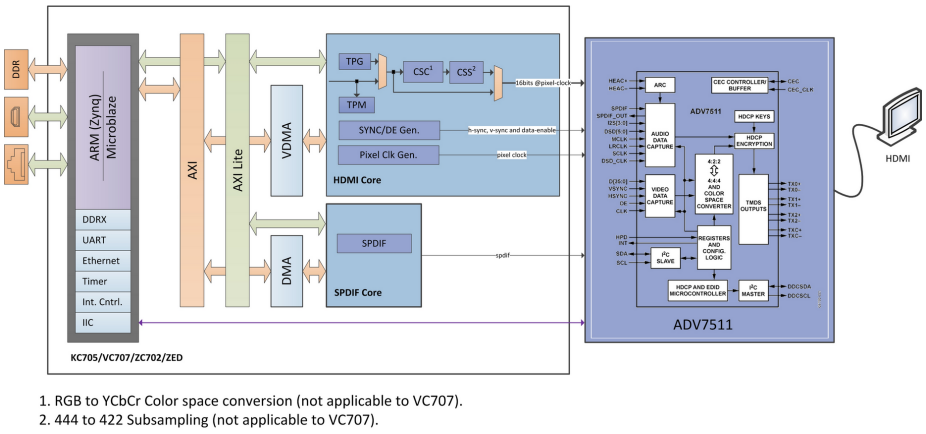


Figure 1: Block Diagram of HDMI transmitter ADV7511

The video mode is 1080p by default (the pixel frequency for 1080p is 148.5MHz) and can be changed by the user by programming the following registers :

1. HSYNC count: is the total horizontal pixel clocks of the video, for 1080p this is 2200.

2. HSYNC width: is the pulse width in pixel clocks, for 1080p this is 44.

3. HSYNC DE Minimum: is the number of pixel clocks for the start of active video and is the sum of horizontal sync width and back porch, for 1080p this is 192 (44 + 148).

4. HSYNC DE Maximum: is the number of pixel clocks for the end of active video and is the sum of horizontal sync width, back porch and the active video count, for 1080p this is 2112 (44 + 148 + 1920).

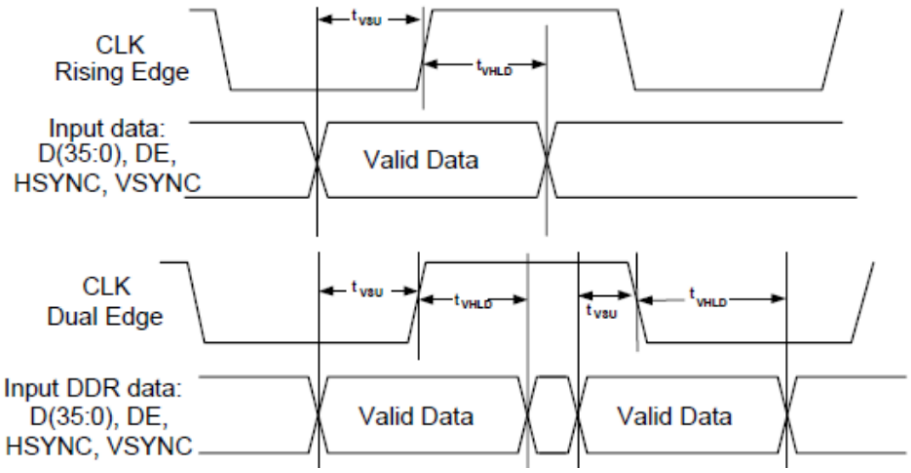
5. VSYNC count: is the total vertical pixel clocks of the video, for 1080p this is 1125.

6. VSYNC width: is the pulse width in pixel clocks, for 1080p this is 5.

7. VSYNC DE Minimum: is the number of pixel clocks for the start of active video and is the sum of vertical sync width and back porch, for 1080p this is 41 (5 + 36).

8. VSYNC DE Maximum: is the number of pixel clocks for the end of active video and is the sum of vertical sync width, back porch and the active video count, for 1080p this is 1121 (5 + 36 + 1080).

The HDMI Video Interface Timing is given in the below diagram.



The reference design reads 24bits of RGB data from DDR and performs color space conversion (RGB to YCbCr) and down sampling (444 to 422). If bypassed, the lower 16bits of DDR data is passed to the HDMI interface as it is. A color pattern register provides a quick check of any RGB values on the monitor. If enabled, the register data is used as the pixel data for the entire frame.

To run program in the HDMI monitor, we connect an HDMI cable between the board HDMI out and the HDMI monitor.

2 Arch Linux on Zedboard

ARM Arch Linux was booted on the Zedboard successfully.

There were 2 major steps to follow. One was to install it to a SD card and the second was to configure the U-Boot. The first was completed but the second step did give some errors explained next.

There were some errors faced in the initial boot and hence, the SBBoot parameters was edited with the correct boot addresses to boot it successfully.

Booting Arch Linux was the first basic step and gave us an insight on how to go about with the further steps in the projects. It couldn't have been possible without a few guidelines that was provided by the Zedboard Arch Linux Project website.