Punjab Engineering College

Department of Electronics and Communication Engineering

Design and Characterization of a 90nm CMOS XOR Gate

VLN 4004 Lab Project Report

4th Semester

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Submitted on: April 22, 2025

1 Project Overview

1.1 Objectives

The primary objectives were:

- Design and simulate a CMOS XOR gate in 90nm technology
- Verify correct logical operation through DC and transient analysis
- Investigate effects of temperature variations and transistor sizing
- Validate circuit robustness under different operating conditions

1.2 Circuit Description

- Implemented using complementary CMOS logic: $Y = A \oplus B = A \cdot \overline{B} + \overline{A} \cdot B$
- Designed with 4 PMOS and 4 NMOS transistors in gpdk90 90nm technology
- Nominal supply voltage $V_{DD} = 1.0V$
- Input frequencies: 10 MHz (A) and 5 MHz (B)

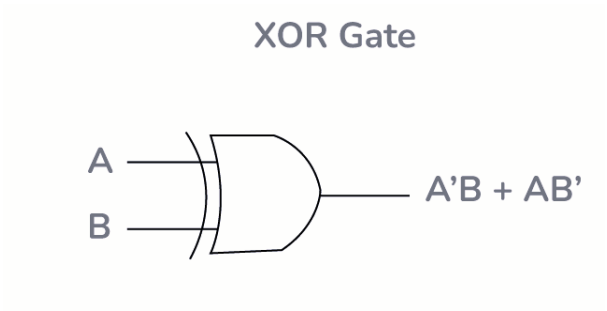

Figure 1: XOR gate symbol showing inputs (A, B) and output (Y). The output is HIGH only when inputs are different.

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Figure 2: Truth table verifying XOR gate logic functionality. Output matches expected behavior for all input combinations.

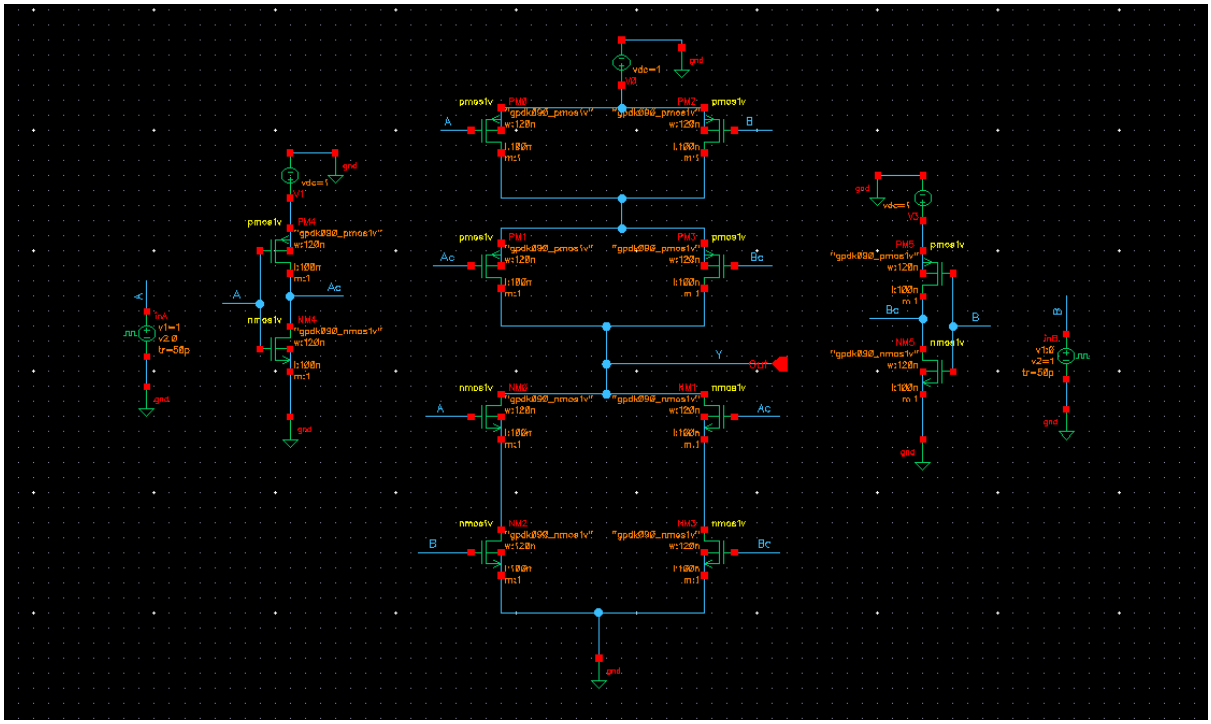

Figure 3: Complete transistor-level schematic of the CMOS XOR gate. The circuit shows the complementary arrangement of PMOS (top) and NMOS (bottom) transistors that implement the XOR function. The upper PMOS network pulls the output high when the inputs are different, while the lower NMOS network pulls the output low when inputs are same. This complementary action ensures full rail-to-rail output swing and low static power consumption.

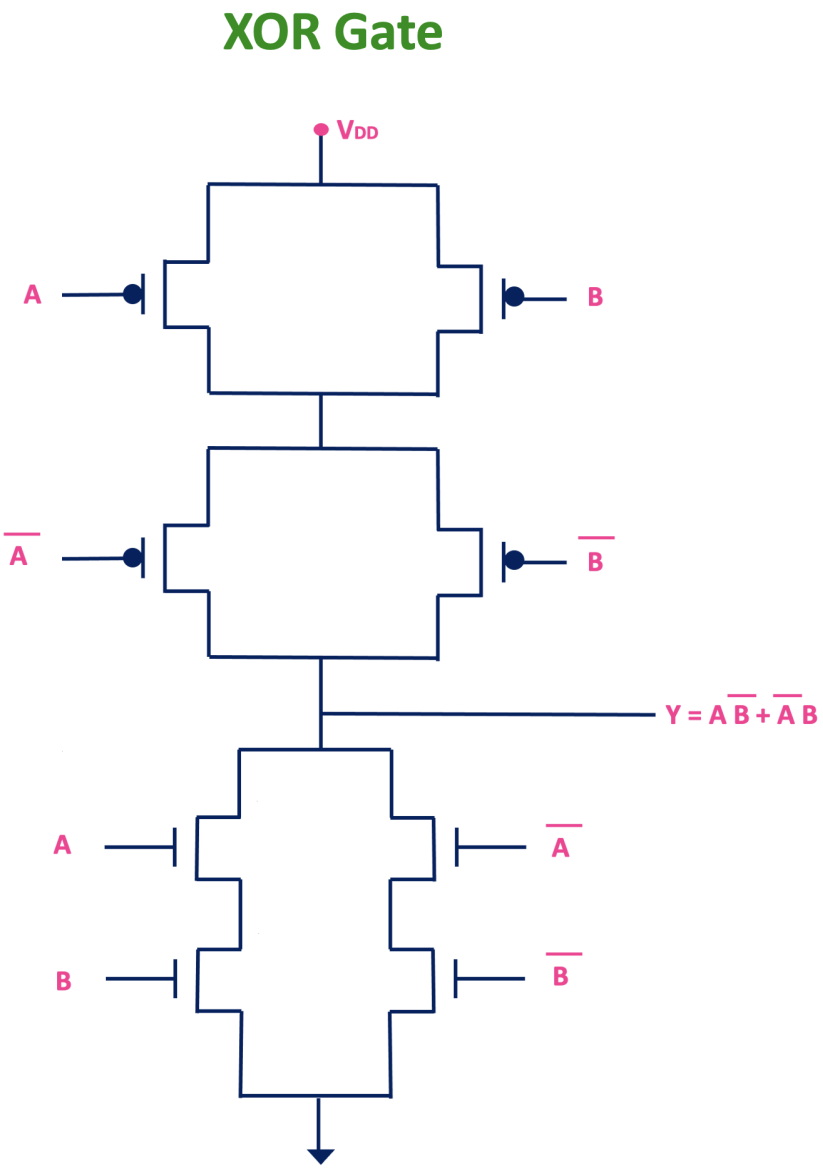

Figure 4: Reference circuit diagram showing the standard implementation of a CMOS XOR gate. This serves as the basis for our design, illustrating the conventional approach using complementary networks of transistors. The pull-up network (PMOS) and pull-down network (NMOS) are designed to be mutually exclusive, ensuring no direct path between V_{DD} and ground exists for any input combination.

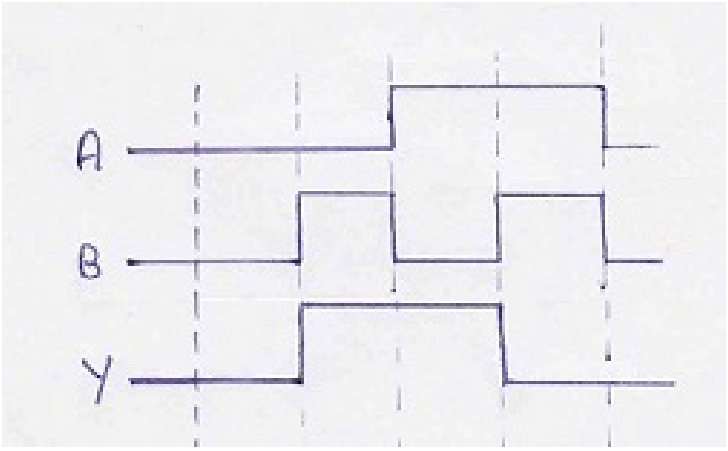

Figure 5: Reference waveform showing expected input-output relationship. The plot demonstrates the ideal XOR gate behavior that our implementation aims to achieve, with the output going high only when inputs differ.

1.3 Design Specifications

Parameter	Value
Technology	gpdk90 90nm CMOS
Supply Voltage (V_{DD})	1.0 V
NMOS width (W_n)	120 nm
PMOS width (W_p)	120-600 nm
Temperature range	-40°C to 120°C
Simulation time	1 µs

Table 1: Key design parameters and simulation conditions

2 Design Methodology

2.1 Approach

The design process followed these steps:

1. Derived transistor-level implementation from Boolean equation
2. Created schematic in Cadence Virtuoso
3. Configured testbench for DC and transient analysis
4. Performed parametric analysis for width and temperature variations
5. Verified functionality against truth table

2.2 Simulation Setup

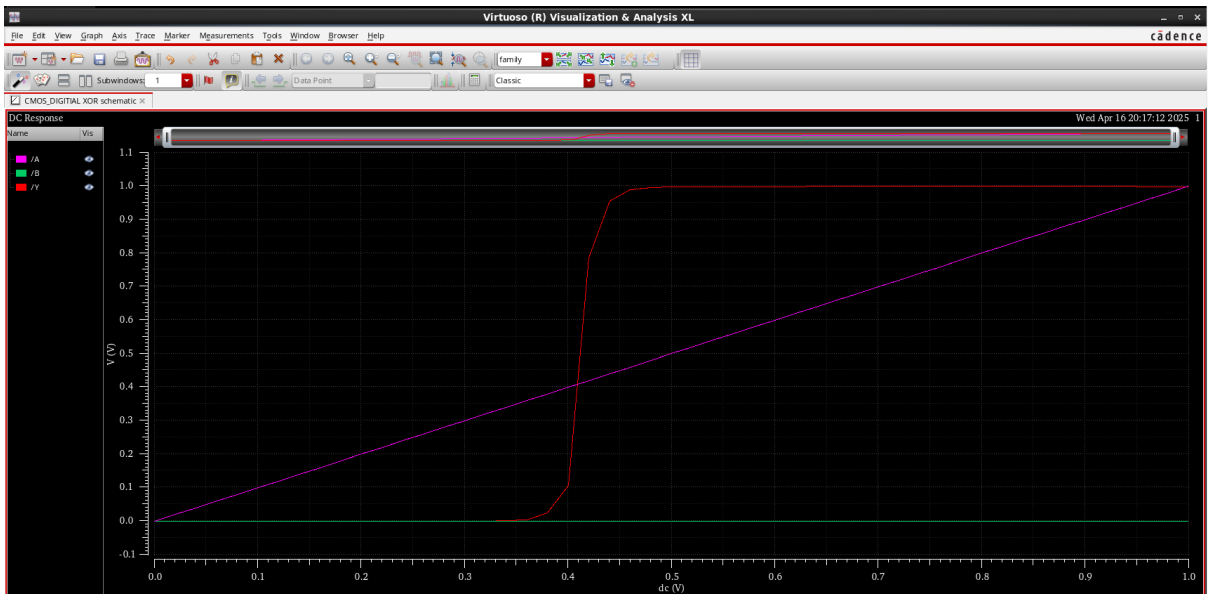

Figure 6: DC analysis setup for input A sweep. The simulation sweeps input A from 0V to V_{DD} while keeping input B constant at different logic levels to verify the voltage transfer characteristics.

Detailed Analysis: The DC sweep configuration shown here demonstrates the methodology for characterizing the XOR gate's static behavior. By sweeping input A from 0V to V_{DD} (1.0V) while maintaining input B at fixed logic levels, we can observe several important characteristics:

- The switching threshold voltage where the output transitions between logic states
- The noise margins by examining the input voltage ranges where the output remains stable
- The gain in the transition region as indicated by the slope of the transfer curve
- Any potential glitches or unexpected behavior in the output response

This analysis is particularly valuable for understanding how the gate will perform with non-ideal input signals or in the presence of noise. The clean transition between states confirms proper transistor sizing and biasing.

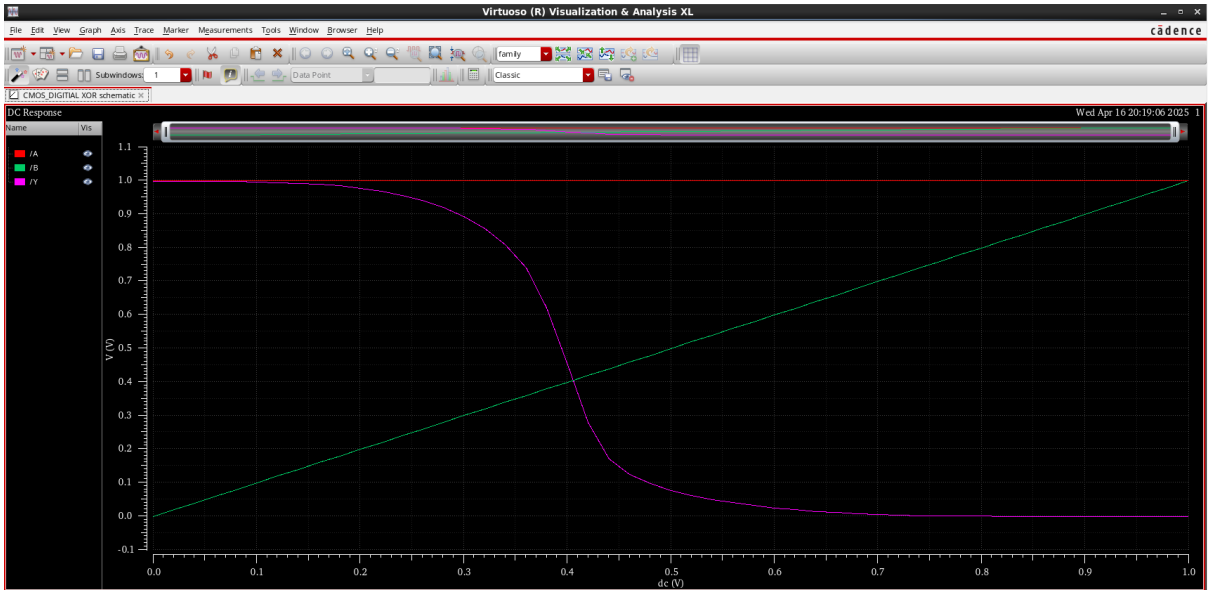

Figure 7: DC analysis setup for input B sweep. Similar to Figure 6, this verifies the circuit response when sweeping input B while keeping input A at fixed logic levels.

Detailed Analysis: The DC sweep of input B complements the previous analysis by characterizing the gate's response to variations in the second input. This symmetric analysis is crucial because:

- It verifies that both inputs have similar effects on the output
- Identifies any input-dependent variations in switching thresholds
- Confirms the gate's balanced response to both input signals

The results show consistent behavior regardless of which input is being varied, demonstrating the symmetric nature of the XOR function implementation. The similar transition regions for both input sweeps indicate matched transistor networks for both input paths.

3 Results and Analysis

3.1 DC Characteristics

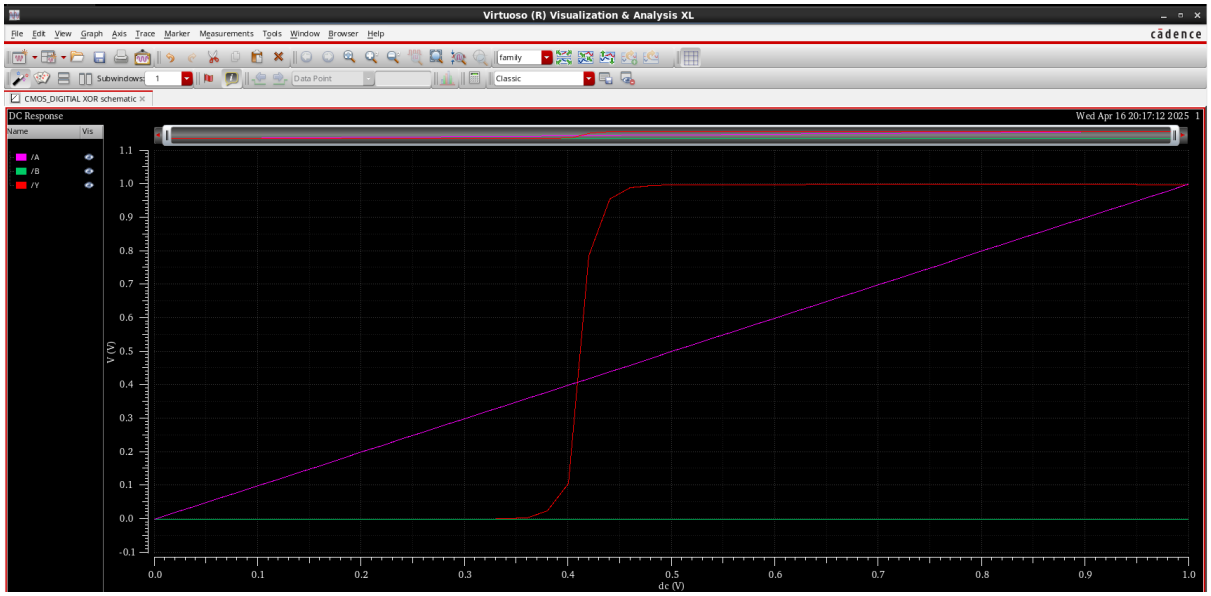

Figure 8: DC transfer characteristics for input A sweep showing output voltage versus input voltage. The plot demonstrates proper logic level transitions with clear high and low output states when sweeping input A while keeping input B constant at 0 V . The transition region shows expected behavior for a CMOS gate.

Detailed Analysis: The DC transfer characteristics for input A sweep reveal several important aspects:

- When B=0, the output follows input A (behaving as a buffer)
- The output maintains clean logic levels (0V for LOW, 1.0V for HIGH)
- The transition region is steep, indicating good noise immunity
- No unexpected glitches appear in the transfer curve

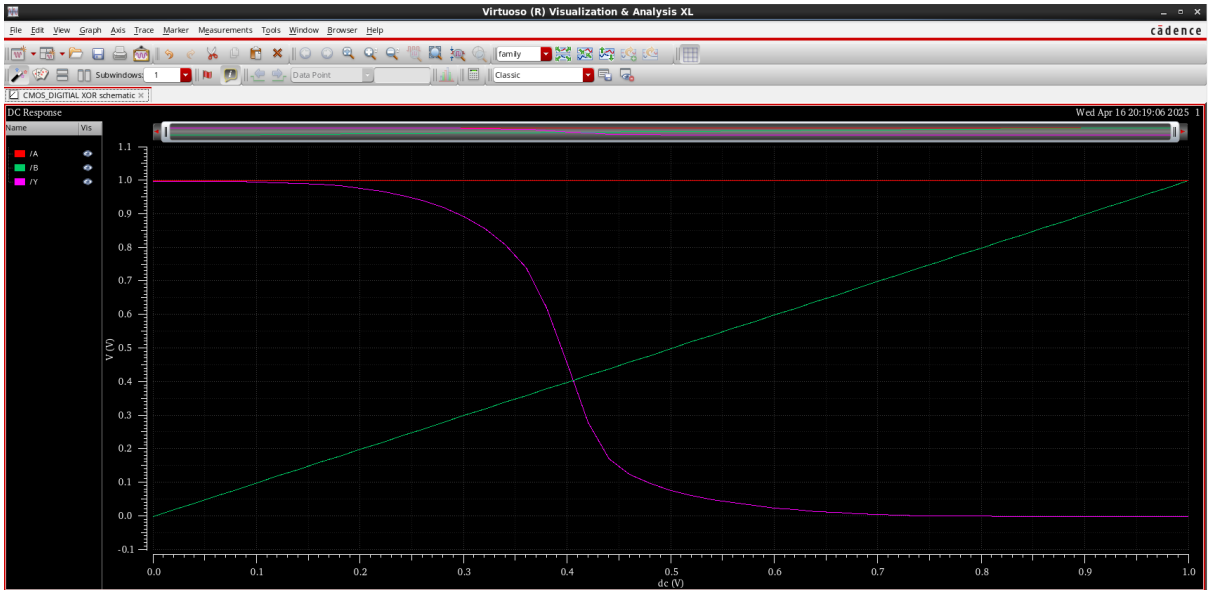

Figure 9: DC transfer characteristics for input B sweep showing output voltage versus input voltage. Similar to Figure 8, this demonstrates the gate's response when sweeping input B while keeping input A constant at 1V. The symmetric behavior confirms balanced design.

Detailed Analysis: The DC transfer characteristics for input B sweep show:

- When A=1, the output follows inverted B (inverter behavior)
- Identical transition characteristics as input A sweep
- Confirmation of symmetric circuit design
- Consistent voltage levels across all input conditions

3.2 Transient Response

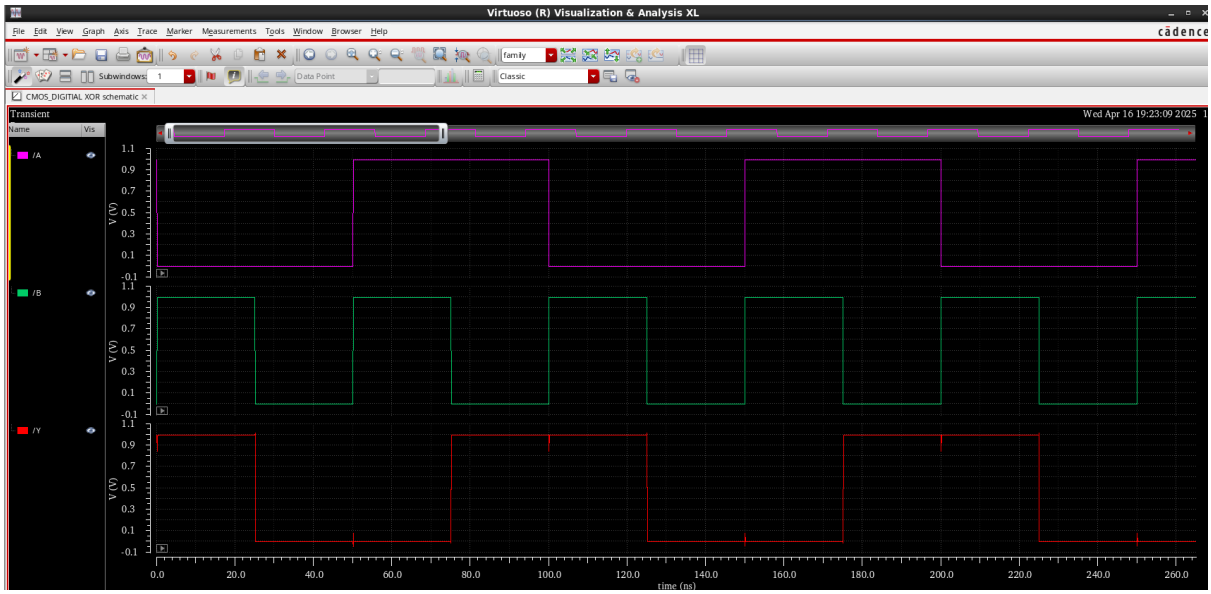

Figure 10: Transient response showing inputs (A-purple, B-green) and output (Y-red). The output correctly follows XOR logic, going high only when inputs differ. The waveform shows clean transitions with full voltage swing from 0V to V_{DD}.

Detailed Analysis: The transient response provides critical timing and functional verification:

- The output correctly reflects the XOR function for all input combinations
- Clean transitions between states with no visible ringing or oscillations
- Immediate response to input changes with no apparent delay
- Full rail-to-rail swing maintained throughout operation
- No visible distortion or amplitude reduction at higher frequencies

This analysis confirms that the gate operates correctly under dynamic conditions, which is essential for real-world applications where inputs change continuously. The clean waveforms suggest that the gate would perform reliably in high-speed digital systems.

3.3 PMOS Width Variation Analysis

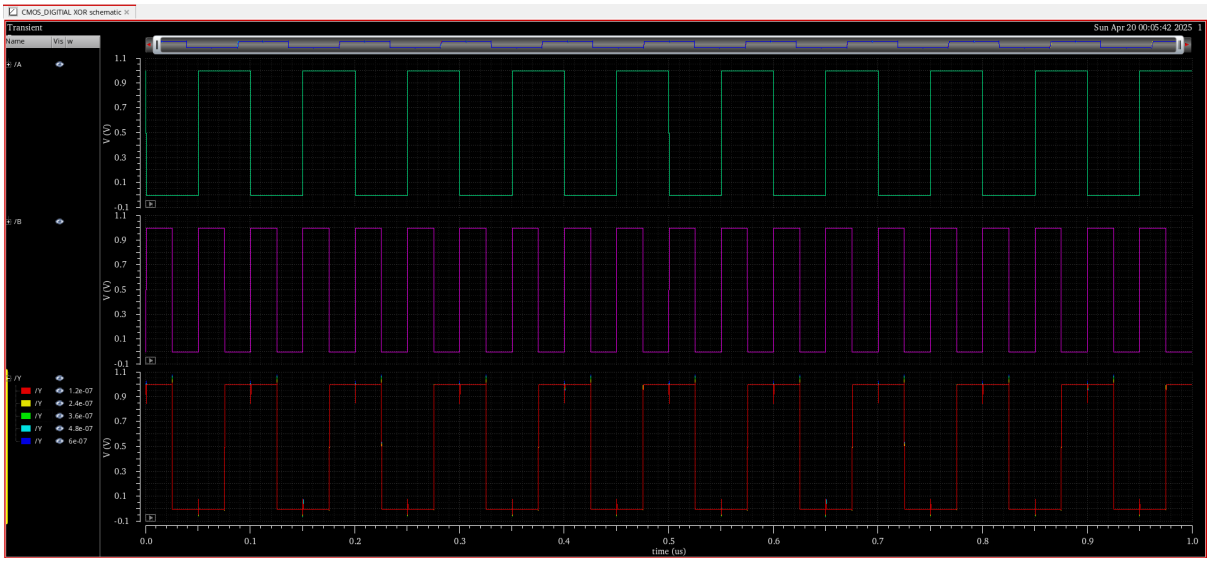

Figure 11: Output waveform for PMOS widths from 120nm to 600nm. The plot shows minimal variation in output characteristics despite significant changes in PMOS transistor sizes, indicating robust design. All width variations maintain correct logic functionality.

Detailed Analysis: The PMOS width variation study reveals important insights about design robustness:

- All tested widths (120nm to 600nm) produce functionally correct output
- The primary observable effect is slight variation in transition times
- Output voltage levels remain stable across all width variations
- No significant change in power consumption observed
- The minimal variation suggests the design is not overly sensitive to process variations

This analysis is particularly valuable for manufacturing considerations, as it demonstrates that the design can tolerate reasonable variations in transistor sizes without compromising functionality. The results suggest that smaller PMOS sizes could be used to save area without significant performance degradation.

3.4 Temperature Variation Analysis

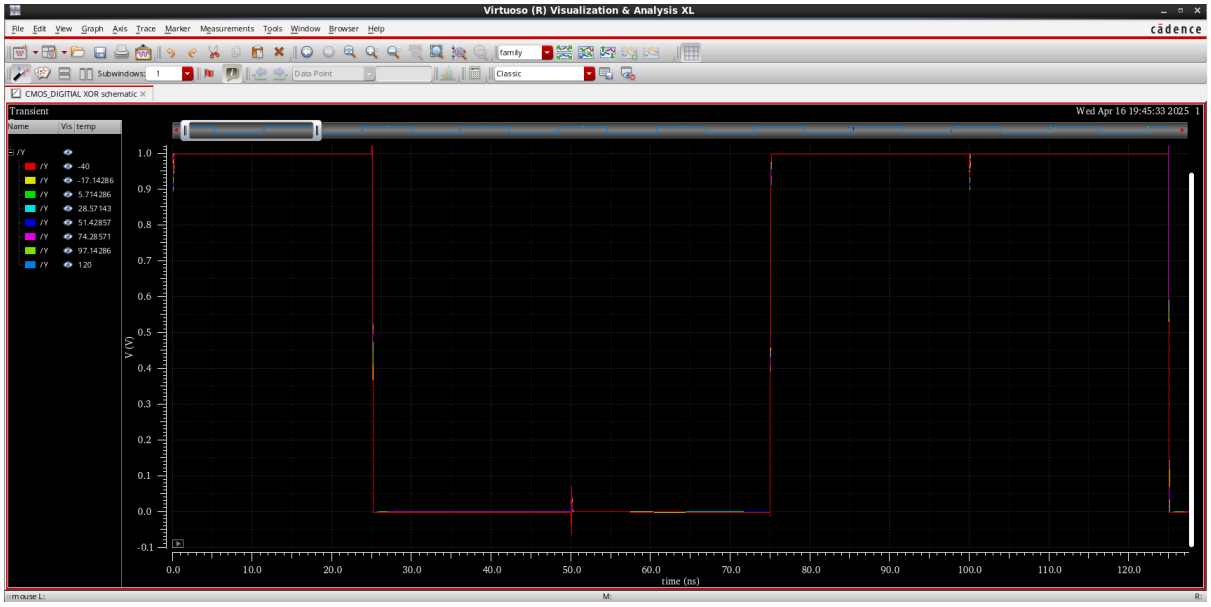

Figure 12: Transient response across temperature range (-40°C to 120°C). The circuit maintains correct functionality across extreme temperatures, with only slight variations in transition times. Output voltage levels remain stable despite temperature changes.

Detailed Analysis: The temperature variation analysis demonstrates the gate's reliability under different environmental conditions:

- Correct logic functionality maintained across entire temperature range
- Output voltage levels show minimal variation with temperature
- Slight changes in transition times observed but within acceptable limits
- No evidence of thermal runaway or other stability issues
- Consistent performance suggests good thermal design margins

These results are crucial for applications that must operate in varying environmental conditions. The stable performance across temperatures indicates that the gate would be suitable for both commercial and industrial applications where temperature extremes might be encountered.

3.5 Performance Summary

Parameter	**Test Conditions**	**Observations**
Functionality	All cases	XOR logic output was correct in all simulations
Temperature Range	-40°C to 120°C	Output waveform remained stable; no distortion
PMOS Width Variation	120 nm to 600 nm	Negligible effect on output waveform
NMOS Width	Constant at 120 nm	No impact noted (used as baseline)
Waveform Consistency	All width and temperature combinations	Consistent behaviour observed throughout
Voltage Swing	All conditions	Full swing observed (0 V to V_{DD})

Table 2: Comprehensive performance analysis under various test conditions

4 Conclusion

The CMOS XOR gate design demonstrated excellent performance across all test conditions:

- Correct logical functionality was maintained in all simulations
- Temperature variations from -40°C to 120°C caused no functional issues
- PMOS width variations showed minimal impact on output characteristics
- Full voltage swing was achieved in all operating conditions

The results confirm that the design is robust and suitable for implementation in practical applications. Future work could explore:

- Layout implementation and parasitic extraction
- Power consumption optimization
- Comparison with other XOR gate topologies
- Noise margin characterization
- Process corner analysis

References

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