Pratyay Rudravaram

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Education

University Of Illinois Urbana Champaign GPA: 3.66/4.00

Bachelor of Science in Computer Engineering, Minor in Mathematics - James Scholar Honors *December 2026*

- **Relevant Coursework** : Computer Organization and Design, FPGA, Operating Systems, Digital Design, Logic Synthesis, Parallel Programming, Data Structures, Electronics, Analog Signal Processing

Experience

RTL Verification Intern, Deepgrid Semi June 2025 – July 2025

- Developed a testing strategy to verify 5 modules of an open-source hardware accelerator using executed SystemVerilog UVM-esqe testbenches while ensuring 100% functional correctness and simulation coverage.
- Collaborated on the testing of a RISC-V based image detection system targeting the Arty A7 FPGA platform.

PCB Design Intern, Apollo Computing Laboratories June 2024 – Aug 2024

- Developed a 2-layer 8-channel power delivery board to enable high availability data-center applications.
- Designed and implemented hardware to control power supply to a server, ensuring precise control.

Electronics Intern, Thermo Fisher Scientific May 2022 – July 2022

- Coded a Raspberry pi test-bench to calibrate a thermocouple for blood bank temperature regulation using python.
- Simulator was deployed to 10+ locations across India and was used to calibrate blood bank coolers for a lower cost

Extracurriculars

Undergraduate Teaching Assistant, ECE385(Digital Systems and FPGA) Jan 2025 – Present

- Hosted office hours for course's FPGA projects including VGA text controller and RISC processor.
- Moderated the 1000+ members class discord server and clarified student questions on SV and FPGA testing.
- Conducted demos, reviewed SystemVerilog testbenches, and facilitated hardware debugging and verification.

Officer, ACM SIGARCH@UIUC Aug 2024 – Present

- Officer and Workshop Lead for UIUC's premier computer architecture student organization.
- Designing workshops to introduce students to RTL design and simulation, computer architecture and ISAs.
- Organized meetings to discuss papers on topics like transactional memory, branch prediction, and cache coherence.

Projects

Superscalar Out-of-Order RISC-V CPU | *SystemVerilog, Verdi, VCS*

- Created a speculative out-of-order RISC-V CPU with an ERR architecture, implementing the RV32IM spec.
- Supports upto 2 instruction commits per cycle, multiple integer execution units, parametric multiplier/div, etc.
- Synthesized dual-issue/commit core with L0+L1 cache on FreePDK's 45nm process node at 525MHz

FPGA-Based Video Game – Spartan-7 Board | `pratyaygopal.github.io/docs/fnaf.pdf`

- Developed a modified port of Five Nights at Freddy's on a Spartan-7 FPGA, achieving real-time gameplay.
- Implemented and integrated an SPI-based keyboard interface supporting up to six simultaneous key presses.
- Designed game logic, randomized seed selection and optimized scalable graphics within a 270 KB RAM constraint.
- Recognized as one of the top 10 projects in ECE 385 and showcased for its technical complexity.

Breadboard Synth | *Falstad, Arduino, Oscilloscopes*

- Designed and Implemented 4 modules for a fully modular music synthesizer for the ECE198 Honors lab.
- Used Falstad for design and worked with electrical workbench tools for testing.

Temperature Regulation Calibrator | `github.com/pratyaygopal/Thermocouple-Simulator`

- Built a proof of concept of an affordable, temperature calibrator using thermocouples and Raspberry Pi.
- Ran 100+ simulations of the ADC/DAC and recorded data to ensure minimal variance in the output voltage.

Technical Skills

Languages: SystemVerilog, Verilog, Bash, C, C++, VHDL, Python, Java

Tools: Git, KICAD, ORCAD, PADS, Intel Quartus, Xilinx Vivado, VS Code, Verdi, VCS, Verilator

Protocols: AXI-4, AXI Stream, SPI, TCP, UDP, UART, I2C