Pratyay Rudravaram

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Education

University Of Illinois Urbana Champaign GPA: 3.7

Bachelor of Sciences in Computer Engineering - James Scholar Honors *December 2026*

- **Relevant Coursework** : Computer Architecture, FPGA, Digital Design, Logic Synthesis, Parallel Programming, Data Structures, Electronics, Analog Signal Processing

Experience

Digital Systems and FPGA Course Assistant Jan 2025 – Present

- Hosted office hours for course's FPGA projects including VGA text controller and RISC processor.
- Moderated the 1000+ members class discord server and clarified student questions on SV and FPGA testing.
- Conducted demos, reviewed SystemVerilog code, testbenches, and facilitated hardware debugging and verification.

FPGA and PCB Design Intern, Apollo Computing Laboratories June 2024 – Aug 2024

- Designed and implemented FPGA-based hardware for mission-critical infrastructure, improving system efficiency.
- Developed a power delivery board from concept to completion for high availability data-center applications.

Intro to Digital Logic Grader Jan 2024 – Present

- Assessed student assignments weekly and provided constructive feedback and handled regrade requests.
- Created rubrics for Digital Logic Design Homework problems that did not have streamlined solutions.

Electronics Intern, Thermo Fisher Scientific May 2022 – June 2022

- Coded a Raspberry pi test-bench to calibrate a thermocouple for blood bank temperature regulation using python.
- Simulator was deployed to 10+ locations across India and was used to calibrate blood bank coolers for a lower cost
- Maintained and updated a spreadsheet of testing data for 100+ trials gathered from SPICE simulation.

Projects

RISCV Five Stage Pipelined Processor | *System Verilog, Verdi, VCS*

- Achieved an instruction throughput of 0.5–1 issues per cycle with optimized forwarding and hazard detection.
- Implemented global stalling and data hazard resolution, including forwarding and pipeline flushing for hazards.
- Simulated and debugged using coremark, ensuring design compliance with the RISCV 32I ISA.

FPGA Video Game | *Vivado, FPGA, SPI, HDMI*

- Ported a modified version of "Five Nights At Freddys" on a Spartan-7 based Urbana Board FPGA.
- Designed the game logic and scalable graphics running at 55 Hz through HDMI and utilizes 270kB of RAM.
- One of the top 10 projects in the class and demoed at the ECE 385 showcase due to the complexity of the project.

16-bit Multi-Cycle RISC Processor on FPGA | *System Verilog, Vivado, FPGA*

- Designed a control unit, a complex datapath, and established seamless interfacing between hardware and RAM.
- Implemented a 16-bit RISC processor with multiple execution phases and memory-mapped I/O on FPGA.

Breadboard Synth | *Falstad, Arduino, Oscilloscopes*

- Designed and Implemented 4 modules for a fully modular music synthesizer for the ECE198 Honors lab.
- Used Falstad for design and worked with electrical workbench tools for testing.

Temperature Regulation Calibrator | *Raspberry Pi, Python, ADC/DAC*

- Built a proof of concept of an affordable, temperature calibrator using thermocouples and Raspberry Pi.
- Ran 100+ simulations of the ADC/DAC and recorded data to ensure minimal variance in the output voltage.
- Github repo: https://github.com/pratyaygopal/Thermocouple-Simulator

Technical Skills

Languages: SystemVerilog, Verilog, Bash, C, C++, VHDL, Python, Java

Tools: Git, KICAD, ORCAD, PADS, Altera Quartus, Xilinx Vivado, VS Code, Verdi, VCS

Certifications: VMware Certified Professional (VCP-DCV), AWS Solutions Architect – Associate, ISC2 CC