Pratyay Rudravaram

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Education

University Of Illinois Urbana Champaign GPA: 3.7/4.0

Bachelor of Science in Computer Engineering, Minor in Mathematics *December 2026*

Relevant Coursework: Computer Organization and Design, FPGA, Operating Systems, Digital Design, Logic Synthesis, Parallel Programming, Data Structures, Electronics, Analog Signal Processing

Experience

RTL Verification Intern, Deepgrid Semi June 2025 - July 2025

- Developed a testing strategy to verify 5 modules of an open-source hardware accelerator using executed SystemVerilog UVM-esqe testbenches while ensuring 100% functional correctness and simulation coverage
- Implemented 4 self-checking testbenches with scoreboard mechanisms and functional coverage models.
- Integrated Vivado-based synthesis and implementation flow to validate FPGA compliance and performance.

PCB Design Intern, Apollo Computing Laboratories June 2024 - Aug 2024

- Developed a 2-layer 8-channel power delivery board to enable high availability data-center applications.
- Designed and implemented hardware to control power supply to a server, ensuring precise control.
- Documented design process, BOMs, and test procedures for future manufacturing and certification.

Computer Architecture [ECE411] Course Assistant Aug 2025 – Present

- Hosted office hours for class projects like the pipelined processor and multicycle set associative cache.
- Clarified doubts during office hours, conducted exam review sessions and proctored exams for 150+ students.

Digital Systems FPGA [ECE385] Course Assistant Jan 2025 – Present

- Hosted office hours for course's FPGA projects including VGA text controller and RISC processor.
- Moderated the 1000+ members class discord server and clarified student questions on SV and FPGA testing.
- Conducted demos, reviewed SystemVerilog testbenches, and facilitated hardware debugging and verification.

President, ACM SIGARCH@UIUC Aug 2024 - Present

- Officer and Workshop Lead for UIUC's premier computer architecture student organization. (sigarch.net)
- Designing workshops to introduce students to RTL design and simulation, computer architecture and ISAs.

Projects

WRAITH: A Resource-Efficient Dataflow Accelerator |

- Working on the RTL, Verification and Layout of the CGRA mesh and preiperal in order pipeline processors.
- Targeting tapeout of a preliminary architecture on TSMC's 65nm process node in Fall 2025.

Superscalar Out-of-Order RISC-V CPU | *pratyay.org/docs/ooo.pdf*

- Created a speculative out-of-order RISC-V CPU with an ERR architecture, implementing the RV32IM spec.
- Supports upto 2 instruction commits per cycle, multiple integer execution units, parametric multiplier/div, etc.
- Synthesized dual-issue/commit core with L0+L1 cache on FreePDK's 45nm process node at 525MHz

FPGA-Based Video Game – Spartan-7 Board | *pratyay.org/docs/fnaf.pdf*

- Developed a modified port of Five Nights at Freddy's on a Spartan-7 FPGA, achieving real-time gameplay.
- Implemented and integrated an SPI-based keyboard interface supporting up to six simultaneous key presses.
- Designed game logic, randomized seed selection and optimized scalable graphics within 270 KiloBytes of RAM.

External Electrical Neuron (N.E.R.V.E) | *pratyay.org/docs/nerve.pdf*

- Developed a system that uses an STM32 microcontroller to send electrical signals to muscles via a TENS unit.
- Programmed a muscular contraction in a user by spiking brain wave intensity using a portable EEG.

Technical Skills

Languages: SystemVerilog, Verilog, Bash, Assembly, C, C++, VHDL, TCL, CUDA, Python, Java

Tools: Git, Intel Quartus, Xilinx Vivado, VS Code, Verdi, VCS, Verilator, Linux

Protocols: AXI-4, AXI Stream, SPI, TCP, UDP, UART, I2C

Lab Tools: Falstad, Arduino, Oscilloscopes, Raspberry Pi, KICAD, ORCAD, PADS, GPUS