Microprocessors, Microcontrollers &
Embedded systems

8051 architecture

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- Microcontrollers
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References

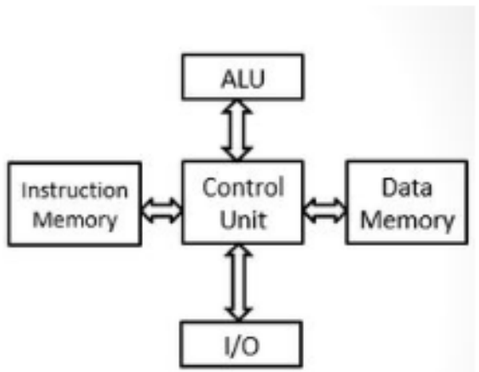
- 8051
  - The 8051 Microcontroller – Architecture, Programming & Applications, Kenneth J. Ayala
  - Atmel 8051 Hardware manual: http://ww1.microchip.com/downloads/en/DeviceDoc/doc4316.pdf

8051 specific features

- 8-bit CPU
- 16-bit PC & DPTR
- 8-bit Program Status word (PSW)
- 8-bit SP
- Internal ROM or EPROM (4K)
- Internal RAM 128 bytes
- 32 I/O pins (4 ports: P0:P3)
- Two 16-bit Timer/Counters: T0 & T1
- Full duplex serial data Tx/Rx
- Control registers: TCON, TMOD, SCON, PCON, IP & IE
- Two external & three internal interrupts
- Oscillator &Clock circuit

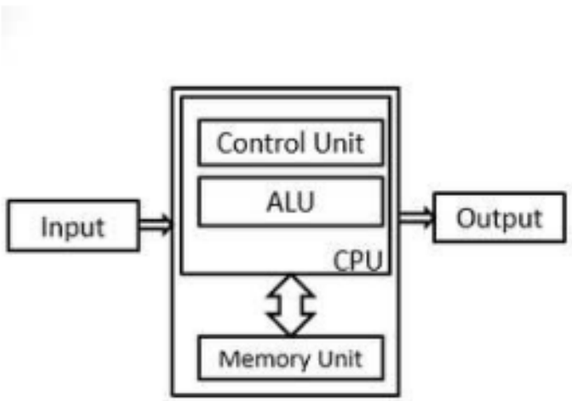
Microcontroller architecture

Harvard architecture – diagram



Harvard Model

Von Neumann architecture – diagram



Von Neumann Model

Harvard	Von Neumann
It requires two memories for their instruction and data.	It requires only one memory for their instruction and data.
Design of Harvard architecture is complicated.	Design of the von Neumann architecture is simple.
Harvard architecture requires separate bus for instruction and data.	Von Neumann architecture requires only one bus for instruction and data.
Processor can complete an instruction in one cycle	Processor needs two or more clock cycles to complete an instruction.
Easier to pipeline, so high performance can be achieve.	Low performance as compared to Harvard architecture.
Comparatively high cost.	It is cheaper.

Modified Harvard architecture: allows the contents of the instruction memory to be accessed as data

Instruction set architecture: RISC vs CISC

- **RISC**
  - Reduced Instructions implies simplified instructions that require single clock cycle for execution
  - Memory-to-register load/store are separate instructions
  - More working memory (RAM) is necessary to store instructions
  - Compiler must perform more work to convert high-level program into assembly instructions
  - Simple processor hardware to decode instructions
  - Instructions can be easily pipelined
  - Small number of single-cycle instructions
  - Limited addressing modes
  - Processors: MIPS, PowerPC, Atmel's AVR, PIC, Arm processors, RISC-V
- **CISC**
  - Complex instructions which require multiple clock cycles for execution. Emphasizes efficiency in #instructions per program
  - Memory-memory: Load/Store incorporated in instruction
  - With single cycle instructions, less RAM is necessary to store assembly instructions
  - Compiler has to work less to convert high-level into assembly instructions
  - Complex processor hardware to decode instructions
  - Pipelining is complex
  - Large number of instructions
  - Compound addressing modes
  - Processors: Intel x86, Motorola 68K, PDP-11

Example: https://cs.stanford.edu/people/eroberts/courses/soco/projects/risc/risccisc/

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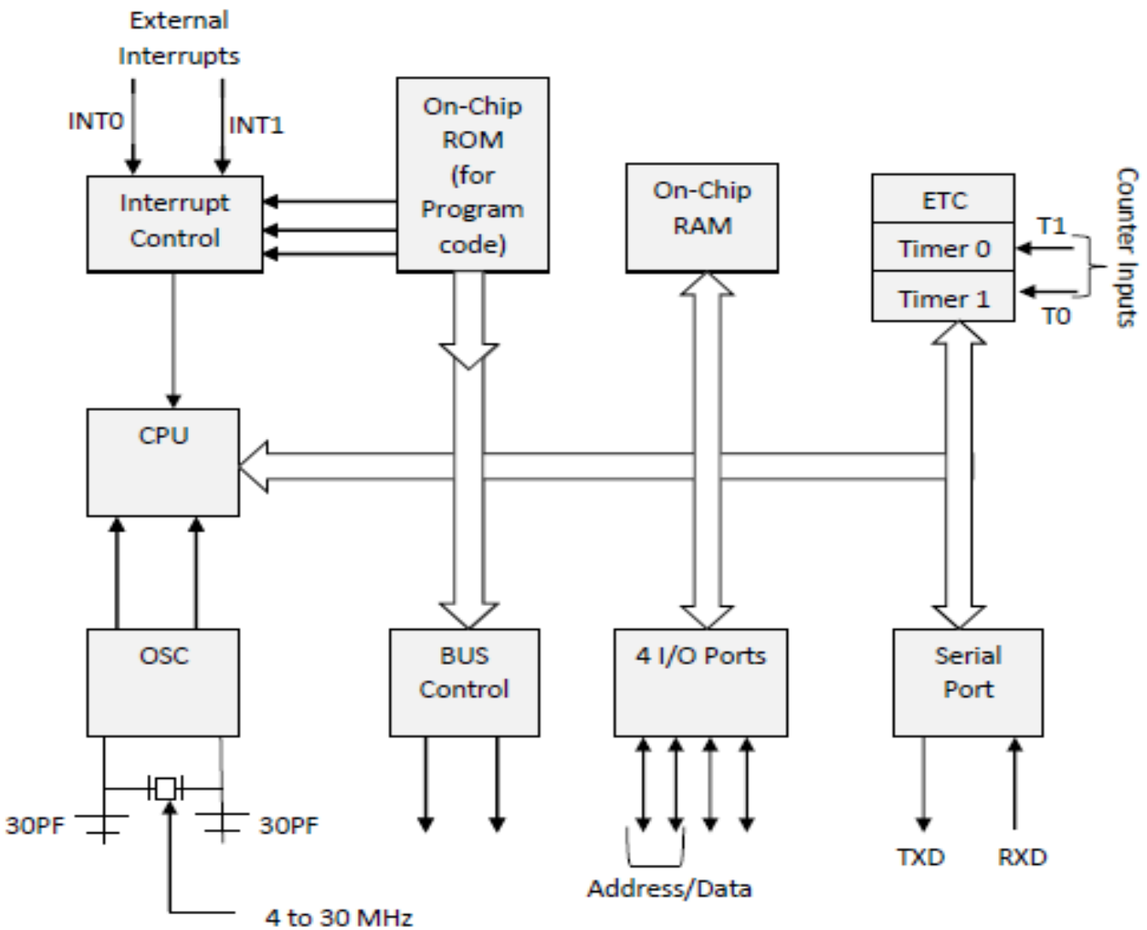

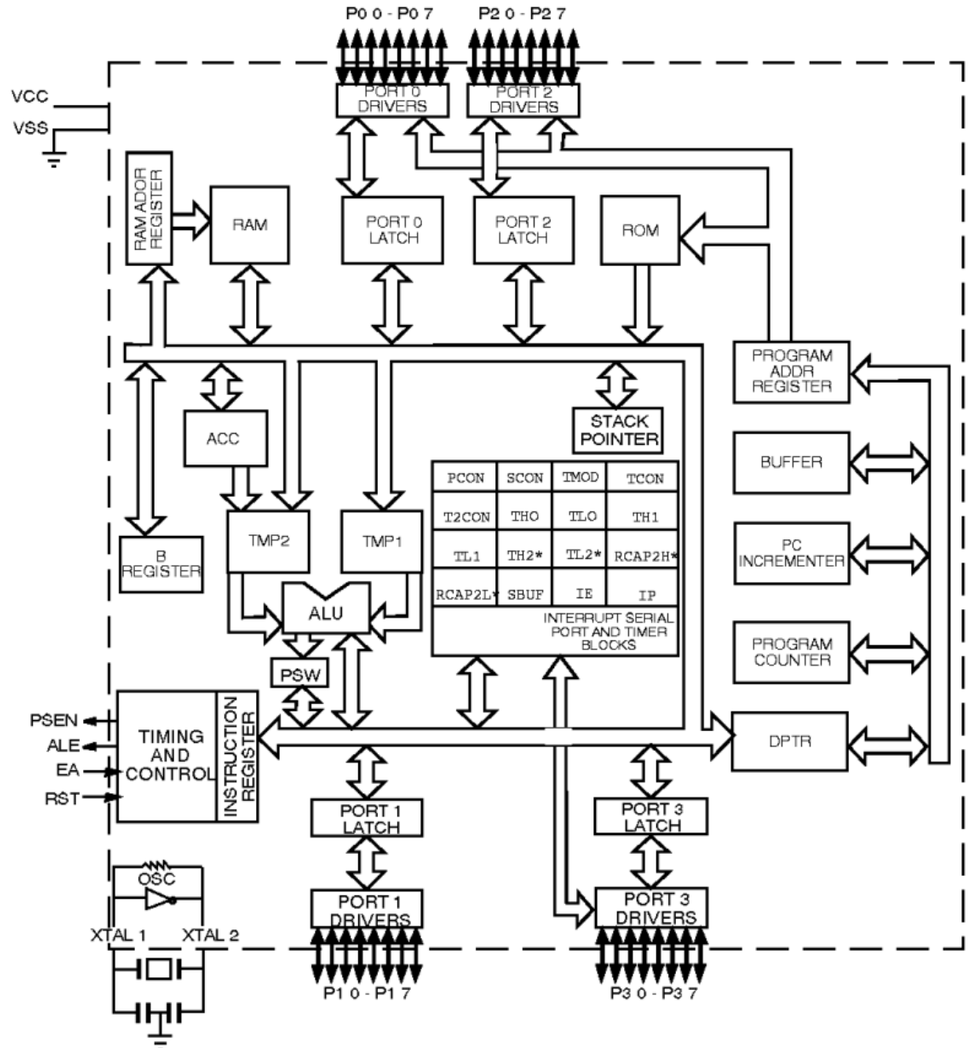

Watch this video: https://www.youtube.com/watch?v=jFDMZpkUWCw

http://ww1.microchip.com/downloads/en/DeviceDoc/doc4316.pdf

Thanks