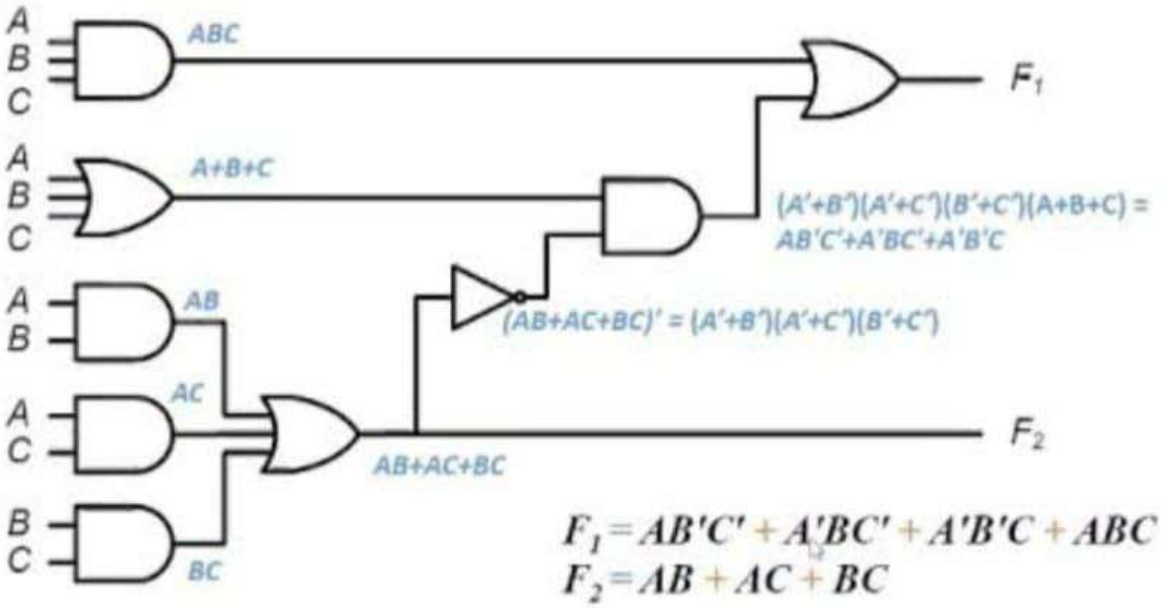


$$F_1 = AB'C' + A'BC' + A'B'C + ABC$$
$$F_2 = AB + AC + BC$$

tion - Route Design - impl_1 | Timing Summary - Route Design - impl_1 | **Path 1 - dataflow_circuit_timing_summary_routed**

Summary

Name	Path 1
Slack	∞ns
Source	A (input port)
Destination	F1 (output port)
Path Group	(none)
Path Type	Max at Slow Process Corner
Requirement	∞ns
Data P...Delay	8.200ns (logic 5.287ns (64.482%) route 2.912ns (35.518%))
Logic Levels	3 (IBUF=1 LUT3=1 OBUF=1)

Data Path

Delay Type	Incr (ns)	Path ...	Location	Cell ...	Cell	Netlist Resources
	(r) 0.000	0.000	Site: U14	A		A
net (fo=0)	0.000	0.000				A
IBUF (Prop_ibuf_I_O)	(r) 1.435	1.435	Site: U14	O	A_IBUF_inst (IBUF)	A_IBUF_inst/O
net (fo=2, routed)	1.212	2.648				A_IBUF
LUT3 (Pro...t3_I2_O)	(r) 0.150	2.798	Site: ...E_X0Y2	O	F1_OBUF_inst_i_1 (LUT3)	F1_OBUF_inst_i_1/O
net (fo=1, routed)	1.700	4.498				F1_OBUF
OBUF (Pr...buf_I_O)	(r) 3.702	8.200	Site: W14	O	F1_OBUF_inst (OBUF)	F1_OBUF_inst/O
net (fo=0)	0.000	8.200				F1
			Site: W14	F1		F1

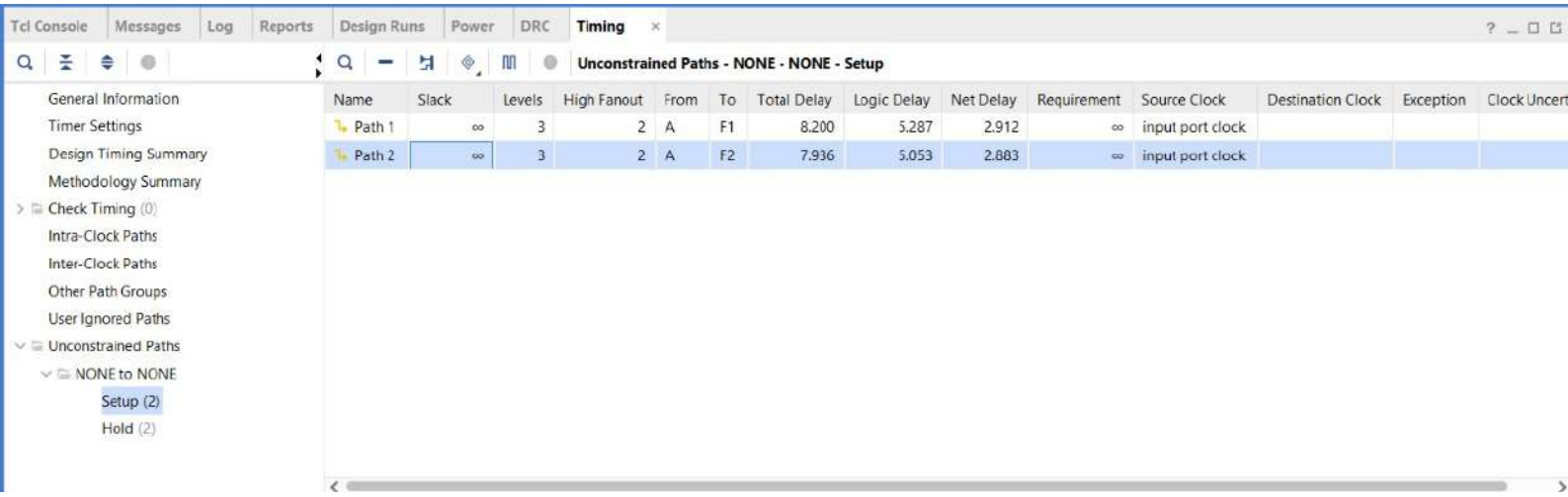
Route Design - impl_1 | Path 1 - dataflow_circuit_timing_summary_routed | **Path 2 - dataflow_circuit_timing_summary_routed**

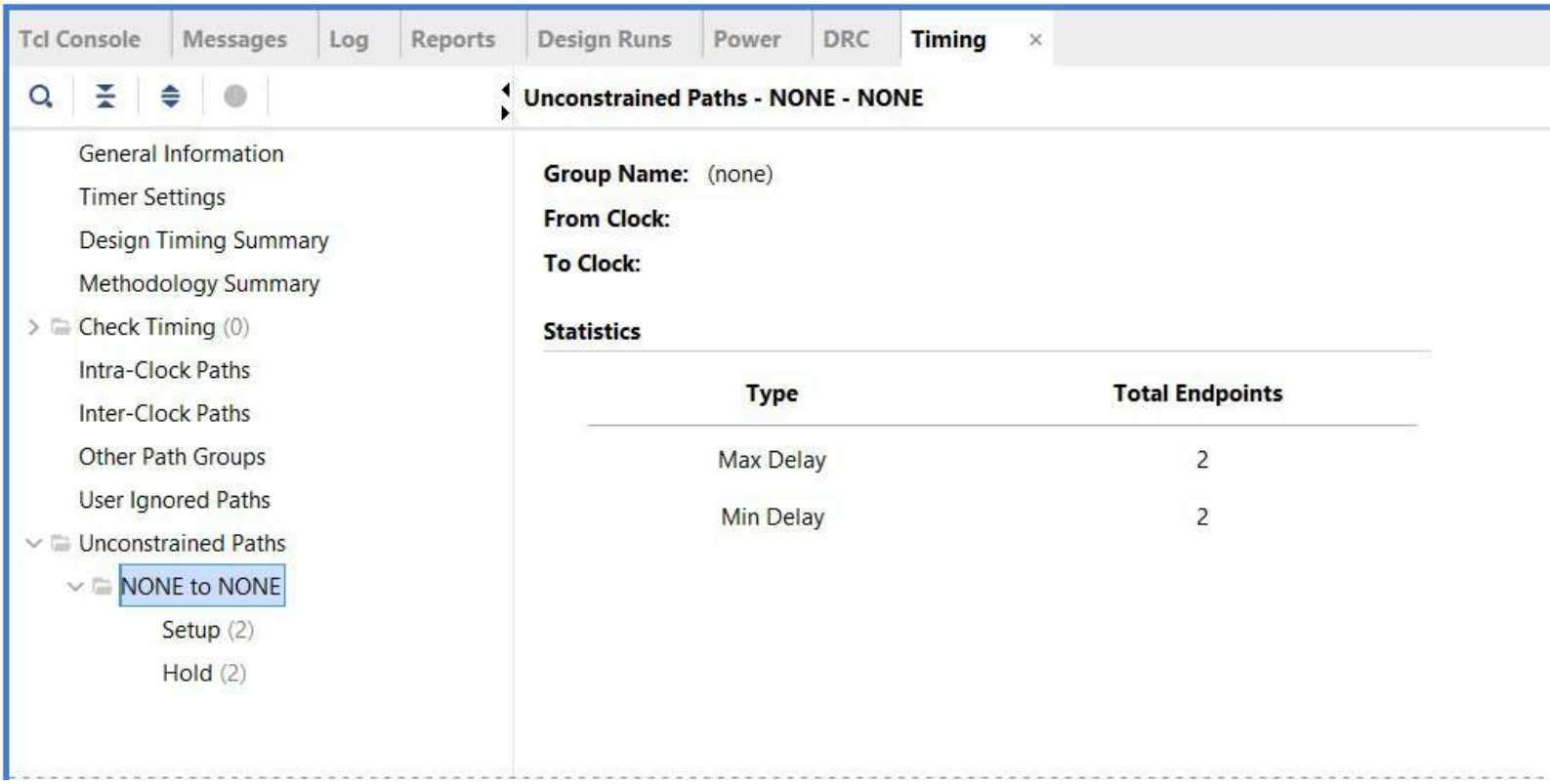
Summary

Name	Path 2
Slack	∞ns
Source	A (input port)
Destination	F2 (output port)
Path Group	(none)
Path Type	Max at Slow Process Corner
Requirement	∞ns
Data P...Delay	7.936ns (logic 5.053ns (63.666%) route 2.883ns (36.334%))
Logic Levels	3 (IBUF=1 LUT3=1 OBUF=1)

Data Path

Delay Type	Incr (ns)	Path (ns)	Location	Cell Pin	Cell	Netlist Resources
	(r) 0.000	0.000	Site: U14	A		A
net (fo=0)	0.000	0.000				A
IBUF (Prop_ibuf_I_O)	(r) 1.435	1.435	Site: U14	O	A_IBUF_inst (IBUF)	A_IBUF_inst/O
net (fo=2, routed)	1.212	2.648				A_IBUF
LUT3 (Pro...t3_I0_O)	(r) 0.124	2.772	Site: ...E_X0Y2	O	F2_OBUF_inst_i_1 (LUT3)	F2_OBUF_inst_i_1/O
net (fo=1, routed)	1.671	4.443				F2_OBUF
OBUF (Pr...buf_I_O)	(r) 3.493	7.936	Site: V14	O	F2_OBUF_inst (OBUF)	F2_OBUF_inst/O
net (fo=0)	0.000	7.936				F2
			Site: V14	F2		F2


Tcl Console
Messages
Log
Reports
Design Runs
Power
DRC
Timing
Unconstrained Paths - NONE - NONE - Setup
General Information
Timer Settings
Design Timing Summary
Methodology Summary
Check Timing (0)
Intra-Clock Paths
Inter-Clock Paths
Other Path Groups
User Ignored Paths
Unconstrained Paths
NONE to NONE
Setup (2)
Hold (2)
Name Slack Levels High Fanout From To Total Delay Logic Delay Net Delay Requirement Source Clock Destination Clock Exception Clock Uncert
Path 1 ∞ 3 2 A F1 8.200 5.287 2.912 ∞ input port clock
Path 2 ∞ 3 2 A F2 7.936 5.053 2.883 ∞ input port clock


Tcl Console
Messages
Log
Reports
Design Runs
Power
DRC
Timing
Unconstrained Paths - NONE - NONE
General Information
Timer Settings
Design Timing Summary
Methodology Summary
Check Timing (0)
Intra-Clock Paths
Inter-Clock Paths
Other Path Groups
User Ignored Paths
Unconstrained Paths
NONE to NONE
Setup (2)
Hold (2)
Group Name: (none)
From Clock:
To Clock:
Statistics
Type
Total Endpoints
Max Delay
2
Min Delay
2