Chiranjeevi Praveen

Bachelor of Technology
Electronics and Communication
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Education

Degree	Institute/Board	CGPA/Percentage	Year
B.Tech, ECE	Indian Institute of Information Technology Nagpur	8.03	[2022 - 2026]
Secondary	Sri Shirdi Sai Junior College	92%	[2020 - 2022]

Skills

- **Languages**: Verilog, SystemVerilog, Python, C/C++
- **Tools**: GIT, Proteus 8 Professional ,Xilinx Vivado,Xilinx Vitis, MATLAB, ANSYS
- **Platforms**: Linux, Windows, Arduino, Raspberry, AutoCAD, LTSpice

Experience

- **National Remote Sensing Centre (NRSC), ISRO** *May 2025 – Present*
  Project Intern
  - Engineered a real-time QPSK receiver system on the Xilinx Zynq-7000 FPGA platform using Verilog, integrating Automatic Gain Control (AGC), Symbol Synchronizer (ZCTED-based), and Phase Ambiguity Resolver (UW and Differential Encoding/Decoding) to ensure robust signal acquisition and reliable communication in noisy environments.
  - Optimized system performance by reducing AGC convergence time by 20%, correcting $\pm 90°/180°$ phase errors under high BER conditions, and enhancing timing accuracy for optimal symbol sampling.
  - Implemented ADC and DAC loopback on the Zynq UltraScale+ ZCU208 board, leveraging TICS Pro for clock setup, Vivado for bitstream generation, and Vitis IDE for application deployment.
  - Set up the ADRV9361-Z7035 SDR board using GitHub reference designs by integrating IP blocks in Vivado and successfully generating bitstreams through provided examples, without external guidance.
  - Currently developing Viterbi and Reed–Solomon decoders for Forward Error Correction (FEC) to reduce Bit Error Rate (BER) by 15% to 20%, enhancing data reliability in digital communication systems.

Projects

- **RF Energy Harvesting and LoRaWAN Communication for Smart Agriculture** *Dec 2024 – Ongoing*
  Tools: Antenna, Rectifiers, Arduino, Sensors, LoRaWAN
  - Designed an RF energy harvesting system that delivered up to 3V using ambient RF signals through rectification, voltage boosting, and supercapacitor-based storage to power embedded sensors and microcontrollers.
  - Integrated a LoRaWAN communication module achieving 10+ km transmission range for real-time environmental data transfer with low power consumption.
  - Created an advanced low-energy visual interface using an E-Ink display which allowed continuous monitoring of four key agricultural metrics, leading to farming practices based on collected observations.
- **Sensor-Based Assistive Control System for Quadriplegic Patients Using Verilog** *Sept 2024-Nov 2024*
  Tools: Verilog, Xilinx-Vivado, Sensors, BASYS3 board
  - Developed a Verilog-based signal processing algorithm to enhance the performance of an FPGA system interfaced with the ADS 2110 ADC.
  - Implemented I2C communication on the Basys 3 FPGA, enabling seamless and efficient ADC integration for real-time signal processing.
  - Led the development of noise reduction and debouncing logic on the FPGA board, incorporating advanced filtering techniques to minimize sensor output interference by 30%.

Achievements

- Qualified for the final round (Top 20%) of the Fetching Fortunes Competition, organized by IIT Hyderabad's E-Cell, after clearing multiple evaluation stages.

Courses

- Digital Signal Processing, Digital & Analog Communications, Wave Guides & Antennas, Embedded Systems, Control Systems, Digital Circuits, CMOS, and Digital Image Processing at IIIT Nagpur.
- Completed Remote Sensing and GPS Technology Implementation from the Indian Institute of Remote Sensing, focusing on applications in geo-spatial analysis.