Design of Area Efficient, Low Power, High Speed and Full Swing Hybrid Multipliers

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***Abstract*—The multiplier is the most basic unit of an arithmetic circuit which is predominantly used in digital processing units and several integrated circuits. The efficiency of a processing unit is measured by its speed and power consumption. The multiplier circuit involves an extensive use of adders that generally add to its hardware complexity and thus is a major bottleneck to fast processing and also consumes high power. Thus it becomes critical to improve speed and reduce power consumption in the multiplier module. The conventional multipliers implemented using the CMOS and GDI technologies and their combination versions, albeit showing improved speed and low power consumption, still suffer from high hardware complexity. This paper proposes the design of an 8-bit hybrid Wallace tree multiplier. The key idea here is to use the power efficient GDI technology based 1-bit hybrid full adder within the popularly used array and Wallace tree multipliers to obtain a new multiplier design with fewer transistors and full output voltage swing. The proposed designs are implemented using Tanner EDA with 250nm technology and simulation results show substantial improvement when compared with the state-of-the-art.**

Keywords—GDI technology; Low power high speed multiplier; Hybrid adder; Wallace tree multiplier; Array multiplier.

I. INTRODUCTION

Multipliers are predominantly used in microprocessors and digital signal processors and are used extensively for performing arithmetic operations [1]. The modus operandi for multiplication in digital systems is repeated additions of partial products and the conventional multipliers require a large number of adders for partial product addition for higher order multiplication. The most basic multiplier is the array multiplier. Several multiplier circuits have been designed over the years to reduce the number of partial products and also to improve speed, namely the Booth [2], the Wallace tree (WT) [3], the Baugh-Wooley [4] multipliers, etc. These multipliers have been implemented in the conventional complementary metal oxide semiconductor (CMOS). Conventional logic designs like the static CMOS and the pass transistor logic (PTL) are vital in designing full adders in multipliers. The PTL offers advantage in terms of the number of transistors used within the adders. The recently proposed gate diffusion input (GDI) technology brought about a novel structural modification to the CMOS implementation and facilitated reduction in the number of transistors used in the circuitry. This consequently reduced the area and the power dissipation and thereby increased the speed of the processor. Over the years research into developing GDI based multiplier circuits to improve speed and reduce power dissipation is gaining popularity [5, 6].

In addition to some of the conventional multipliers mentioned above, the Vedic multiplier and its variants have gained prominence over the years owing to its speed of computation [7]. Among other developments is the design of one bit adder using GDI technology as proposed in [8]. Here the designed adder was used within a multiplier to obtain full swing at the output voltage. However the adder consists of 21 transistors and hence is expensive both in terms of speed and power consumption. Other attempts to develop fast multipliers included hybrid versions of multipliers. [9] proposed the 16 bit Booth-Wallace multiplier but this design does not achieve full swing at the output. More recently attempts at combining both CMOS and GDI technologies have gained popularity because this hybrid combinational design results in fewer transistors with achieving possibly full voltage swing at the output. The authors in [10] developed a 16 bit Wallace tree multiplier using full adder modules by combining CMOS and GDI technologies. Although this approach has proved to be fast, it does not achieve full output voltage swing. To achieve full swing in the output voltage, [11] and [12] proposed GDI technology based 4 bit multiplier circuits using a hybrid combination of conventional multipliers. However their designs used over 18 transistors to implement the full adder and hence do not compare well in terms of power and speed. The recently proposed [13] 1 bit adder using both CMOS and GDI technologies has shown promise by involving only 14 transistors in its adder circuitry. A review on state-of-the-art multipliers used in modern VLSI design can be found in [14]. It is imperative that it is critical to design a multiplier that consists of fewer transistors and also obtains a full swing in the output voltage and this paper focuses in that direction.

This paper employs a GDI based 1-bit hybrid full adder consisting of just 14 transistors within the conventional array and WT multipliers, while the conventional adders proposed in recent literature use 24, 21 and 18. This paper proposed to employ the hybrid adder within the array and/or WT multipliers, hence the name hybrid array (H-A) and hybrid Wallace tree (H-WT). The key idea here is to reduce the partial products involved in the multiplication process by reducing the number of bits in each stage via the column compression method using a combination of adder circuits. This proposal, moreover, achieves full swing at the output voltage by virtue of using GDI and swing restoration schemes (i.e., pass transistor logic) together within the developed adder circuit. The merits of this idea are reduced power and area

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consumption by virtue of substantially reducing the number of transistors and full swing at the output voltage thus making the design robust to voltage errors.

The rest of the paper is organised as follows. Section 2 briefly describes the conventional multipliers and the 1-bit GDI based hybrid full adder. Section 3 presents the proposed H-A and H-WT multipliers. In section 4, we present the simulation and comparative results and conclude in section 5.

II. Multipliers And Their Digital Implementations

The concept of digital logic design provides a basic understanding on how digital circuits operate. The digital circuits are generally constructed by using logic gates which are the representations of a Boolean logical function. In order to realise the Boolean logic several digital design technologies including the CMOS, the PTL and the GDI technologies have been introduced. The multiplier circuits are been implemented using these technologies.

A multiplier generally consists of two operands, the multiplicand and the multiplier to generate a product result. The two operands are multiplied bit-by-bit in parallel to generate a partial product (PP) matrix. The PP terms are added to obtain the product. That is to say, the multipliers are an interconnection of complex adders. The PP matrix determines the overall performance of the multiplier in terms of speed, area and power consumption so the organisation and implementation of adders within the multiplication circuitry become critical for high speed low power applications. A *N*-bit array multiplier operation using an n-bit multiplicand *A* and an m-bit multiplier *B* is described as

$$A = \sum_{i=0}^{n-1} a_i 2^i, i = 0, \dots, n-1$$

$$B = \sum_{j=0}^{m-1} b_j 2^j, j = 0, \dots, m-1$$

$$P = AB = \sum_{i=0}^{n-1} \sum_{j=0}^{m-1} a_i b_j 2^i 2^j$$

This operation results in N^2 partial product terms which can be added using N (N-1) full adders and AND gates. The array multiplier [1] is the most widely used multiplier circuit that employs the above logic. An 8-bit array multiplier logic implementation is shown in Figure 1. Here the PPs are generated using AND gates and are then shifted as per their bit positions and added. It is apparent that the 8-bit array multiplier employs 56 full adders and 64 AND gates. The Wallace tree multiplier (WT) [3] proposed to compress the PP columns and achieve faster multiplication in logarithm time of the word length of the multiplier operand. The Figure. 2 shows the 8-bit Wallace tree multiplier. An 8-bit WT multiplier employs 64 AND gates and 46 full adders thus substantially improving the speed of the multiplication process. This paper proposes to achieve further improvement in terms of speed, area and power consumption by using the GDI based hybrid adders within the Wallace tree multiplier. The hybrid adder is now described in brief.

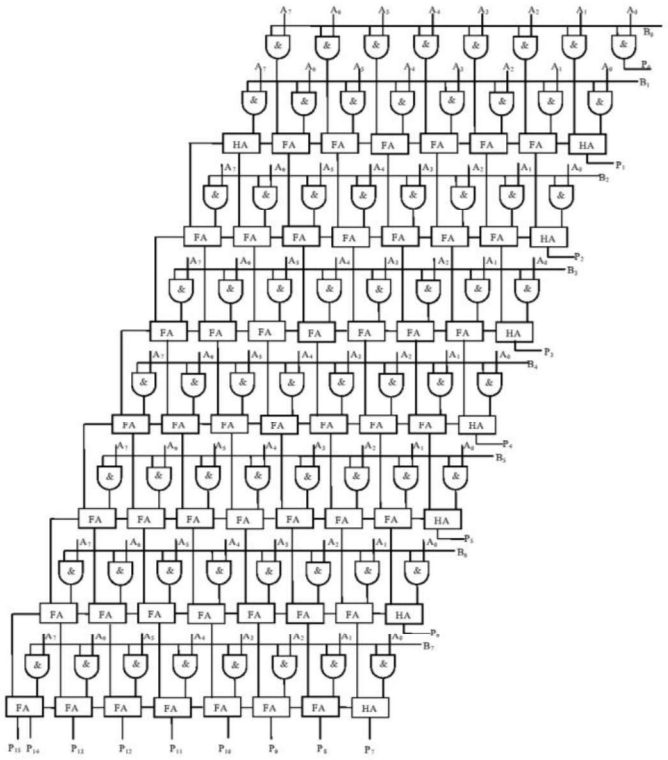

Fig. 1. 8-Bit Array Multiplier

A. The GDI based 1-bit hybrid full adder

The 1-bit hybrid full adder [13] proposed recently employed multiple logic styles and reported favourable results in terms of low power consumption. The schematic diagram of hybrid 14T full swing GDI full adder is shown in Figure 3. The adder employs two GDI MUX blocks, one GDI XNOR cell, swing restored transmission gate (SRTG) block and swing restored pass transistor (SRPT) block. The key idea here is that the MUX-1 is used to generate Sum from the outputs of XOR and XNOR cells with control input Cin. The MUX-2 multiplexes the inputs B and the output of XNOR cell with control element Cin in generating Cout. For full swing restoration at the output Sum and Carry Cout are achieved by using SRTG and SRPT cells respectively.

The functions that realise the 1-bit hybrid full adder is as below,

$$\text{Sum} = \overline{\text{C}_{\text{in}}}(\text{A} \oplus \text{B}) + \text{C}_{\text{in}}(\text{A} \odot \text{B})$$

$$\text{C}_{\text{out}} = \overline{(\text{A} \odot \text{B})}\text{C}_{\text{in}} + (\text{A} \odot \text{B})\text{B}$$

The merit of the proposed GDI based hybrid full adder over the conventional full adder is that the transistor count is halved and consequently we gain tremendously in terms of area and power dissipation.

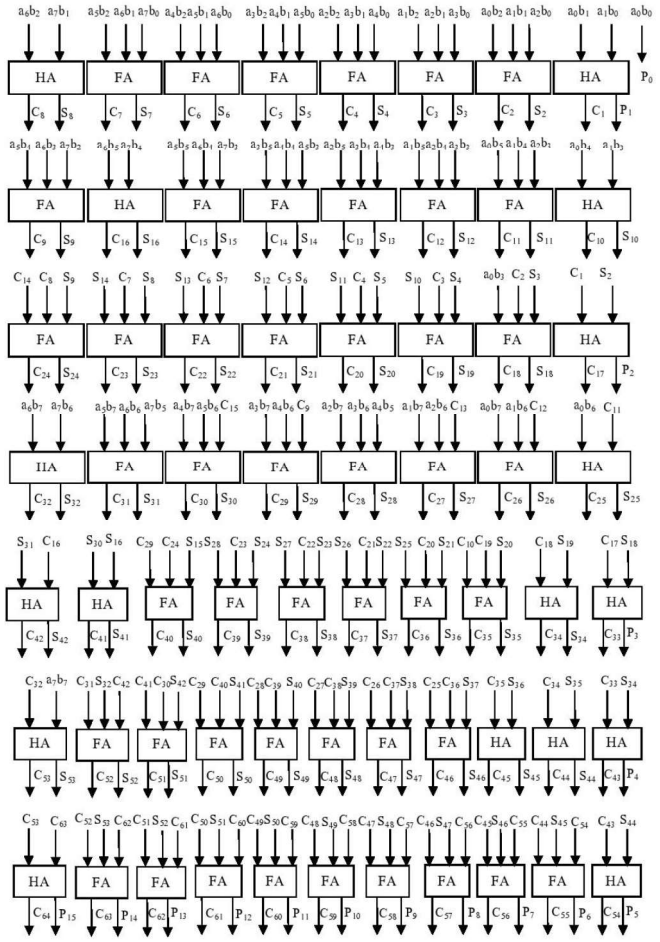

Fig. 2. 8-Bit Wallace Tree Multiplier

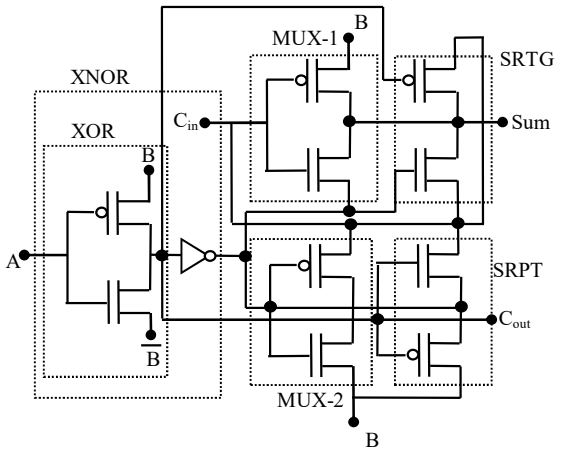

Fig. 3. GDI based 1-bit hybrid full adder

III. Proposed H-A And H-WT Multipliers

In this paper we propose to use the GDI 1-bit hybrid adder within the array and Wallace tree multiplier circuits, hence the name, H-A and H-WT multipliers. The array multiplier is the most popularly used one, and the WT multiplier is considered the fastest multiplier by virtue of adding the PPs in parallel using a tree of carry save adders (CSA). However the WT multiplier requires excess wiring due to its irregular structure thereby increasing the power consumption and dissipation. This problem is overcome by using the GDI technology that reduces the area requirement. However GDI structures do not achieve full swing in the output voltage. We propose to solve this problem by using the hybrid 1-bit full adder in [13] within the WT multiplier. The schematic diagram for the proposed H-WT multiplier is the same as shown in Figures 1 and 2 with the exception that the adders are now replaced with 1-bit hybrid full adders. The dot representation of the proposed 8-bit H-WT is shown in Figure 4. Here the multiplier and multiplicand operands are multiplied together to form N=8 row PP matrix. These PPs are generated in parallel using AND gates. The underlying principle is to reduce the number of PPs by reducing the number of bits in each stage using full and half adders.

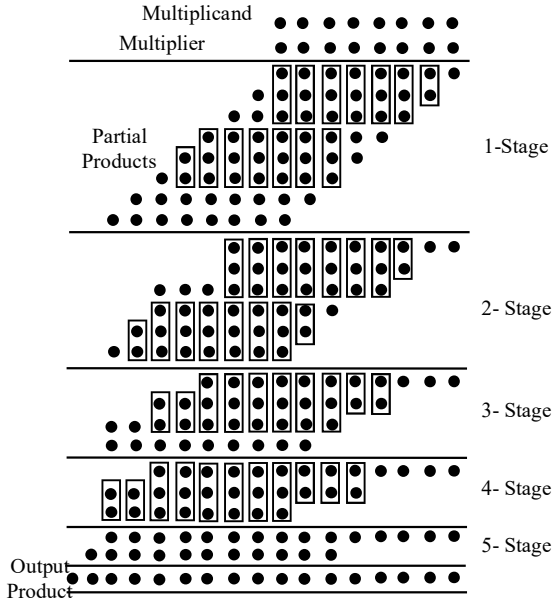

Fig. 4. Dot representation of the proposed 8-bit H-WT

As can be seen in the figure, let R_i be the total number of rows in a PP matrix. The number of rows in the remaining groups is calculated by

$$R_r = \frac{2R_i - 1}{3} + R_{i-1} \bmod 3, i = 1, \ldots, N$$

and the number of rows in the last group is given by $R_l = R_i \bmod 3$. In the first stage of a partial product matrix the full adder adds 3 bits from a single column and produces a 2 bit output - one in the same column and the other in the successive column. Similarly the half adder adds 2 bits from a single column and produces a 2 bit output - one in the same column and the other in the successive column. The multiplier consists of the number of such column compressions stages until a two row matrix is generated. In the final stage the two operands are compressed by using fast carry propagate adder to obtain the final product result. Therefore the total number of

adders the last stage are $FA_l = (2N-1) - S$ where S is the number of stages in a H-WT multiplier.

The key merits of this implementation for the H-WT case is that we now require only 64 AND gates, 46 adders and only half the number of transistors, 14 against 28 in the conventional case. Moreover the critical benefit is that we obtain full swing in the output voltage by virtue of using the hybrid 1-bit full adder.

IV. Simulation Study

The proposed H-A and H-WT multipliers are implemented on Tanner tools EDA with 250nm technology. We test the performance of our multipliers in terms of delay, energy, area and normalised efficiency. We first show the implementation of the proposed H-WT multiplier (we limit the demonstration to the H-WT case). The schematic of the GDI based 1-bit full adder and our H-WT multiplier using former are shown in Figures 5 and 6 respectively. For the multiplier implementation, the output waveforms are shown in Figure 7. In this figure, we show the waveforms in four subfigures for convenience sake. It can be seen that the 8-bit multiplicand A = {a0, a1, …, a7} = {1,0,1,0,1,0,1,0} = 170 and the 8-bit multiplier B = {b0, b1,..., b7} = {1,1,0,0,1,1,0,0} = 207 results in the product P = {p0, p1,…, p15} = {1,0,0,0,0,1,1,1,0,1,1,1,1,0,0,0} = 34680 and carry bit of C = {0}. The results in these figures validate the proposed method and that we indeed obtain legal results for all binary combinations.

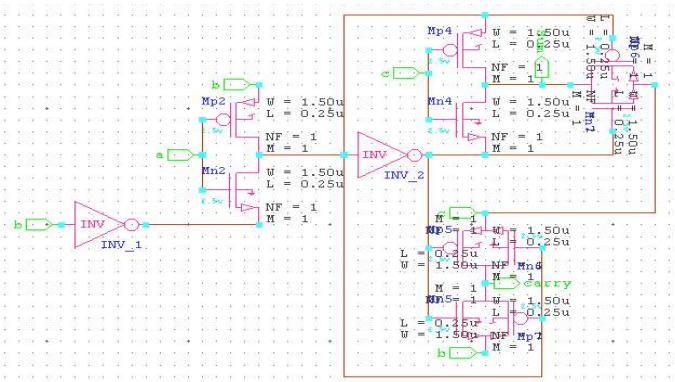

Fig. 5. Schematic diagram of the GDI based 1-bit hybrid full adder.

We now present how well the proposed H-A and H-WT multipliers perform against the conventional multipliers in Table I. Apart from detailing the transistor count, we use three performance characteristics. First, the power consumption of a circuit, defined as

$$P = \propto C_L V_{DD}^2 f$$

where P is the power consumption $\propto$ is the switching activity, C_L is the load capacitance, V_{DD} is the supply voltage, f is the switching frequency. Second, the time delay of a circuit, defined as

$$t_d = \frac{C_L V_{DD}}{(V_{DD} - V_T)^{\propto}}$$

where define each term td is the time delay and VT is the threshold voltage.

Fig. 6. Schematic diagram of the proposed GDI based H-WT multiplier. Each block in the figure is either a AND gate, conventional half adder or a 1-bit hybrid full adder shown in Figure 5.

It can be observed from the table that our proposed H-A multiplier requires only 848 transistors against the 2440 in the most popularly used array multiplier and the proposed H-WT multiplier requires only 886 against 2547 in the conventional CMOS WT multiplier. This means that there is nearly four times reduction in the transistor count and this substantially reduces the area requirement of our multiplier circuit. With respect to power consumption, it can be observed that the proposed H-A and H-WT multipliers consume nearly 40% less power than the conventional array and WT multipliers. This is due to the fact that the number of transistors in the full adders is halved which consequently reduces the amount of current drawn by the circuit during operation. The big advantage of the proposed H-A and H-WT multipliers can be seen in terms of its delay characteristic. It can be observed that our proposed methods achieve nearly 100 times improvement in speed against the conventional array and WT multipliers owing to twice the reduction in the amount of wiring in the circuitry as a consequence of halving the number of required transistors. Moreover the proposed methods are 10 times faster than [10] although they are 10 times power inefficient; a possible reason for this can be attributed to the full swing at the output obtained in the proposed methods.

Finally, we discuss the full output swing. The Figure 7 shows the two inputs to the multiplier, the multiplicand and the multiplier. Considering the first test case in the plots; the first 8 plots represent the 8-bit multiplicand A = {a0, a1, …, a7} = {1,0,1,0,1,0,1,0} = 170 and the second 8 plots represent the 8-bit multiplier B= {b0, b1,..., b7} = {1,1,0,0,1,1,0,0} = 207. For this input Figure 8 shows the output of the proposed H-WT multiplier obtaining full swing at the output P = {p0, p1,..., p15} = {1,0,0,0,0,1,1,1,0,1,1,1,1,0,0,0} = 34680. The carry bit C = {0} is not shown in the figure. The Figure 9

shows the product for the GDI based multiplier method proposed by Ravi Korra et al., in [10]. It can be observed that [10] does not achieve full output swing, albeit showing superiority in power reduction as shown in Table 1, while our methods achieve full swing due to the use of hybrid adders thus making it robust to signal fluctuations.

TABLE I. EXPERIMENTAL COMPARATIVE RESULTS.

Design	Transistor Count	Power (W)	Delay (ns)
Proposed H-A multiplier	848	5.83E-04	1.2549
Proposed H-WT multiplier	886	6.93E-04	2.6734
Array multiplier	2440	8.10E-04	99.1246
WT multiplier	2547	9.71E-04	188.5159
Vedic multiplier	2862	6.71E-03	100.0600
Shoba Mohan et al., 2015	1647	1.17E-03	11.6243
Ravi Korra, 2017	604	8.94E-05	10.5230

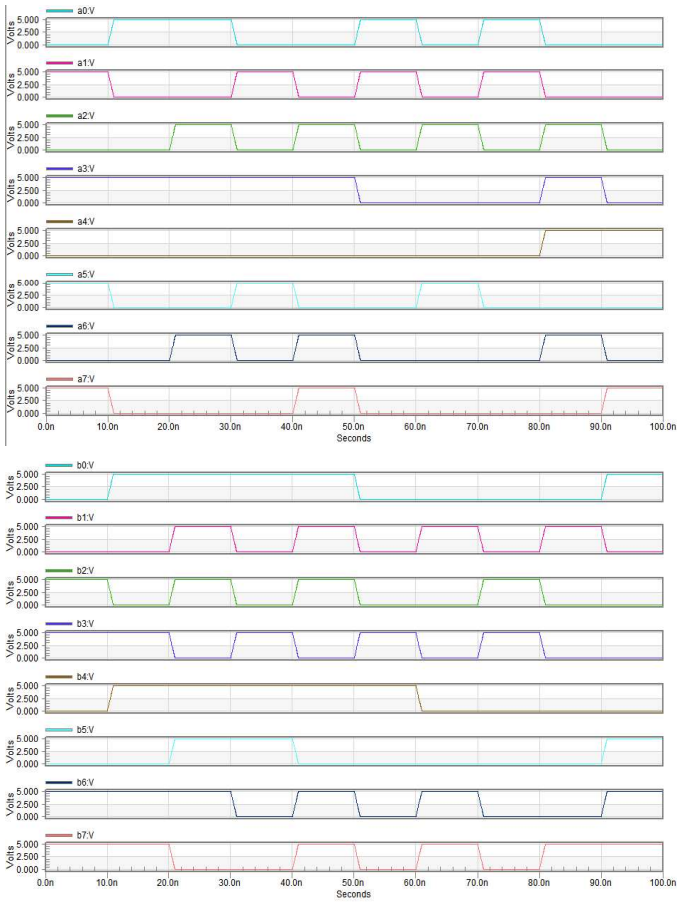

Fig. 7. The first 8 plots represent the multiplier bits and the second 8 the multiplicand bits. The first test case corresponds to A = {1,0,1,0,1,0,1,0} = 170 and the second to B = {1,1,0,0,1,1,0,0} = 207.

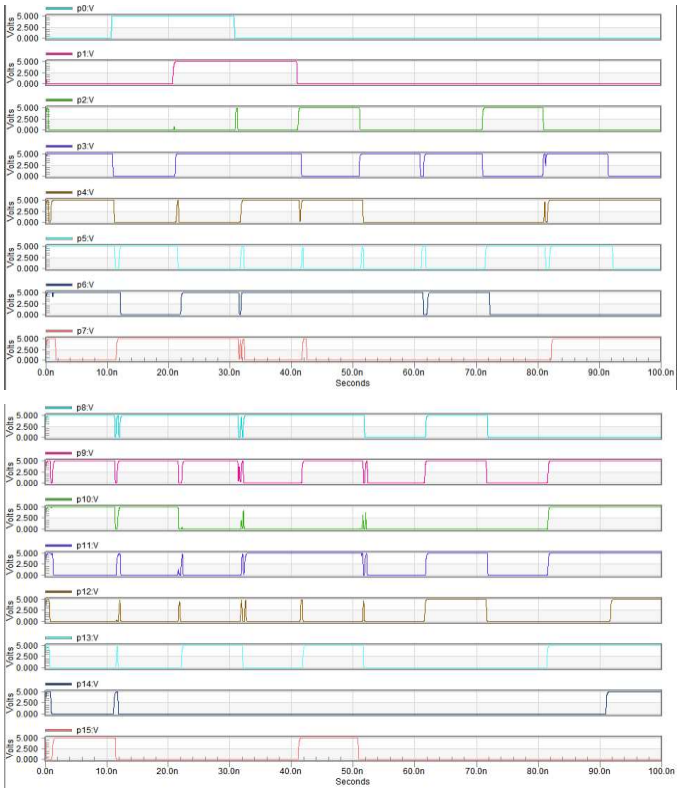

Fig. 8. Output waveforms of the proposed GDI based H-WT multiplier output. The first test case represent the product result P = {p0, p1,..., p15} = 34680.

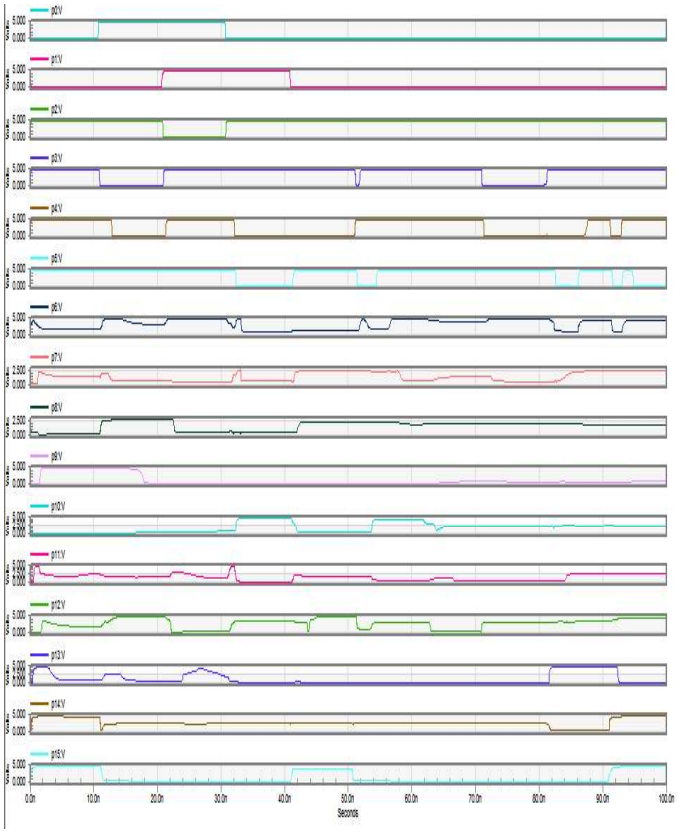

Fig. 9. Output waveforms of the GDI based multiplier in [10].

V. CONCLUSION

This paper proposed a novel idea of using the GDI based 1 bit hybrid full adder within the array and WT multiplier structures. This idea exploits the possibility of achieving full output voltage swing using the hybrid adder whilst achieving lower power consumption and faster operation by virtue of reducing the circuitry involved for the multiplication process. Using simulative comparisons, it has been shown that the proposed H-A and H-WT multipliers are superior to the conventional ones in terms of power, delay and area consumption.

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