SN54LS189A, SN54LS219A, SN54LS289A, SN54LS319A
SN74LS189A, SN74LS219A, SN74LS289A, SN74LS319A

64-Bit Random-Access Memories

These monolithic TTL memories feature Schottky clamping for high performance and a fast chip-select access time to enhance decoding at the system level. A three-state output version and an open-collector-output version are offered for both of the logic choices. A three-state output offers the convenience of an open-collector output with the speed of a totem-pole output; it can be bus-connected to other similar outputs, yet it retains the fast rise time characteristic of the TTL totem-pole output. An open-collector output offers the capability of direct interface with a data line having a passive pull-up.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

• ISO-9001
• AS9120 certification
• Qualified Manufacturers List (QML) MIL-PRF-38535
  • Class Q Military
  • Class V Space Level
• Qualified Suppliers List of Distributors (QSLD)
  • Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

- **Organized as 16 Words of Four Bits Each**

- **Choice of Buffered 3-State or Open-Collector outputs**

- **Choice of Noninverted or Inverted Outputs**

- **Typical Access Time . . . 50 ns**

SN54LS189A, SN54LS289A . . . J PACKAGE
SN74LS189A, SN74LS289A . . . J OR N PACKAGE
(TOP VIEW)

```
        A0 [ 1    U  16 ] VCC
        S̄ [ 2       15 ] A1
       R/W̄[ 3       14 ] A2
        D1 [ 4       13 ] A3
        Q̄1 [ 5       12 ] D4
        D2 [ 6       11 ] Q̄4
        Q̄2 [ 7       10 ] D3
       GND [ 8        9 ] Q̄3
```

SN54LS219A, SN54LS319A . . . J PACKAGE
SN74LS219A, SN74LS319A . . . J OR N PACKAGE
(TOP VIEW)

```
        A0 [ 1    U  16 ] VCC
        S̄ [ 2       15 ] A1
       R/W̄[ 3       14 ] A2
        D1 [ 4       13 ] A3
        Q1 [ 5       12 ] D4
        D2 [ 6       11 ] Q4
        Q2 [ 7       10 ] D3
       GND [ 8        9 ] Q3
```

description

These monolithic TTL memories feature Schottky clamping for high performance and a fast chip-select access time to enhance decoding at the system level. A three-state output version and an open-collector-output version are offered for both of the logic choices. A three-state output offers the convenience of an open-collector output with the speed of a totem-pole output; it can be bus-connected to other similar outputs, yet it retains the fast rise time characteristic of the TTL totem-pole output. An open-collector output offers the capability of direct interface with a data line having a passive pull-up.
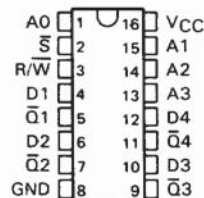
write cycle

Information to be stored in the memory is written into the selected address location when the chip-select ($\overline{S}$) and the write-enable ($R/\overline{W}$) inputs are low. While the write-enable input is low, the memory outputs are off (three-state = Hi-Z, open-collector = high). When a number of outputs are bus-connected, this off state neither loads nor drives the data bus; however, it permits the bus line to be driven by other active outputs or a passive pull-up.

read cycle

Information stored in the memory (see function table for input/output phase relationship) is available at the outputs when the write-enable input is high and the chip-select input is low. When the chip-select input is high, the outputs will be off.
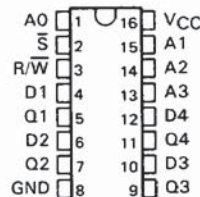
FUNCTION TABLE

FUNCTION	INPUTS		OUTPUTS			
	CHIP SELECT	WRITE ENABLE	'LS189A	'LS289A	'LS219A	'LS319A
Write	L	L	Z	Off	Z	Off
Read	L	H	Complement of Data Entered	Complement of Data Entered	Data Entered	Data Entered
Inhibit	H	X	Z	Off	Z	Off

H = high level, L = low level, X = irrelevant, Z = high impedance

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SN54LS189A, SN54LS219A, SN54LS289A, SN54LS319A
SN74LS189A, SN74LS219A, SN74LS289A, SN74LS319A
64-BIT RANDOM-ACCESS MEMORIES

logic symbols

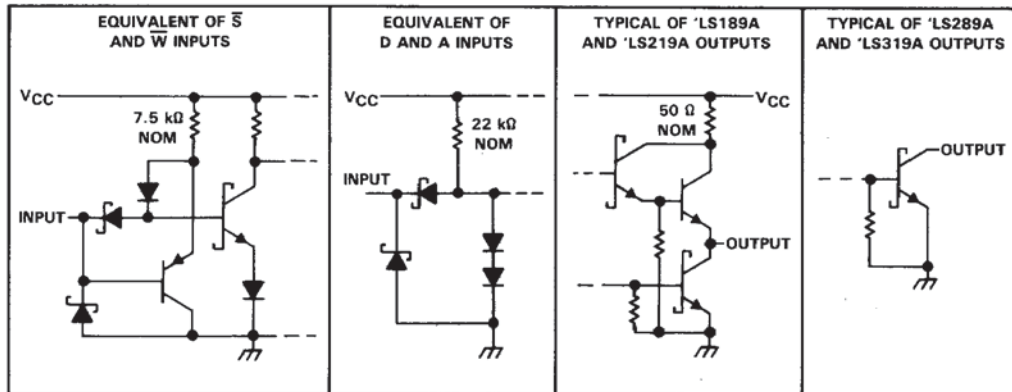
'LS189A
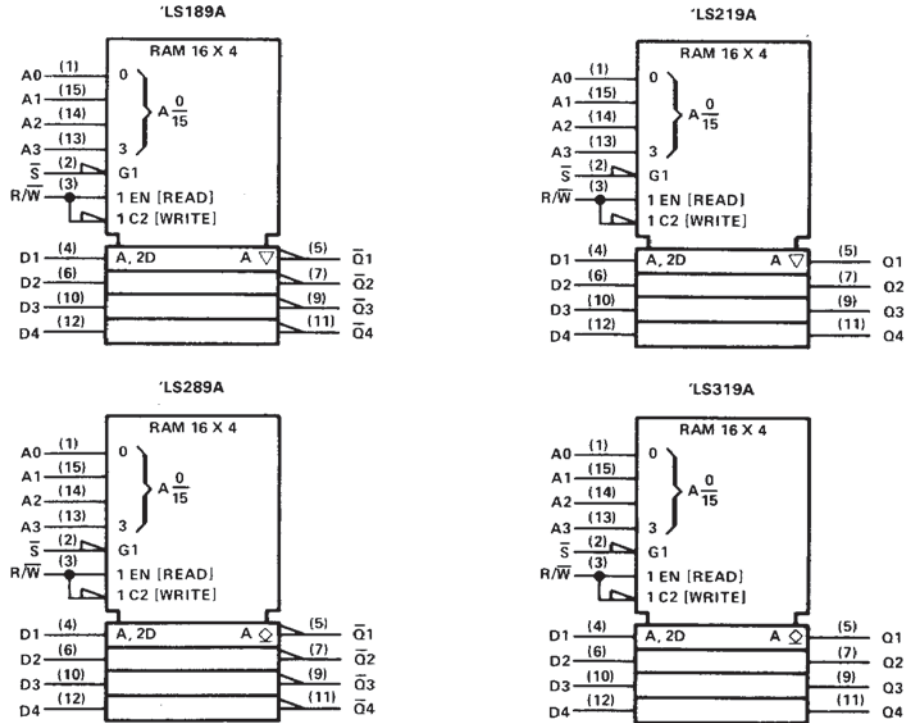
'LS219A

'LS289A

'LS319A

schematics of inputs and outputs

| EQUIVALENT OF $\overline{S}$ AND $\overline{W}$ INPUTS | EQUIVALENT OF D AND A INPUTS | TYPICAL OF 'LS189A AND 'LS219A OUTPUTS | TYPICAL OF 'LS289A AND 'LS319A OUTPUTS |

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) .... 7 V
Input voltage .... 7 V
Off-state output voltage: 'LS189A, 'LS219A .... 5.5 V
         'LS289A, 'LS319A .... 7 V
Operating free-air temperature range: SN54LS' Circuits .... −55°C to 125°C
            SN74LS' Circuits....................... 0°C to 70°C
Storage temperature range .... −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS189A, SN54LS219A			SN74LS189A, SN74LS219A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−1			−2.6	mA
Low-level output current, I_{OL}				12			24	mA
Width of write pulse (write enable low), $t_{w(wr)}$		100			70			ns
Setup time	Address before write pulse, $t_{su(ad)}$	0↓			0↓			ns
	Data before end of write pulse, $t_{su(da)}$	100↑			60↑			
	Chip-select before end of write pulse, $t_{su(S)}$	100↑			60↑			
Hold time	Address after write pulse, $t_{h(ad)}$	0↑			0↑			ns
	Data after write pulse, $t_{h(da)}$	0↑			0↑			
	Chip-select after write pulse, $t_{h(S)}$	0↑			0↑			
Operating free-air temperature, T_A		−55		125	0		70	°C

↑↓The arrow indicates the transition of the write-enable input used for reference: ↑ for the low-to-high transition, ↓ for the high-to-low transition.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[†]		SN54LS189A SN54LS219A			SN74LS189A SN74LS219A			UNIT
				MIN	TYP[‡]	MAX	MIN	TYP[‡]	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max, I_{OH} = MAX		2.4	3.1		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL}max, V_O = 2.7 V				20			20	µA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL}max, V_O = 0.4 V				−20			−20	µA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				100			100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current[§]	V_{CC} = MAX		−30		−130	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			35	60		35	60	mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
[‡]All typical values are at V_{CC} = 5 V, T_A = 25°C.
[§]Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
NOTE 2: I_{CC} is measured with the write-enable and chip-select inputs grounded, all other inputs at 4.5 V, and all outputs open.

switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LS189A SN54LS219A			SN74LS189A SN74LS219A			UNIT
				MIN	TYP[‡]	MAX	MIN	TYP[‡]	MAX	
$t_{a(ad)}$	Access time from address	C_L = 45 pF, See Note 3			50	90		50	80	ns
$t_{a(S)}$	Access time from chip select (enable time)				35	70		35	60	ns
t_{SR}	Sense recovery time				55	100		55	90	ns
t_{PXZ}	Disable time from high or low level	from $\overline{S}$	C_L = 5 pF, See Note 3		30	60		30	50	ns
		from R/$\overline{W}$			40	70		40	60	

[‡]All typical values are at V_{CC} = 5 V, T_A = 25°.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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recommended operating conditions

		SN54LS289A, SN54LS319A			SN74LS289A, SN74LS319A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
Low-level output current, I_{OL}				12			24	mA
Width of write pulse (write enable low), $t_{w(wr)}$		100			70			
Setup time	Address before write pulse, $t_{su(ad)}$	0‖			0‖			ns
	Data before end of write pulse, $t_{su(da)}$	100‖			60‖			
	Chip-select before end of write pulse, $t_{su(S)}$	100‖			60‖			
Hold time	Address after write pulse, $t_{h(ad)}$	0‖			0‖			ns
	Data after write pulse, $t_{h(da)}$	0‖			0‖			
	Chip-select after write pulse, $t_{h(S)}$	0‖			0‖			
Operating free-air temperature, T_A		-55		125	0		70	°C

‖The arrow indicates the transition of the write-enable input used for reference: ↑ for the low-to-high transition, ↓ for the high-to-low transition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[†]		SN54LS289A SN54LS319A			SN74LS289A SN74LS319A			UNIT
				MIN	TYP[‡]	MAX	MIN	TYP[‡]	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = -18 mA			-1.5			-1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V,	V_O = 2.4 V			20			20	μA
		V_{IL} = V_{IL}max,	V_O = 5.5 V			100			100	
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{IL} = V_{IL}max	I_{OL} = 24 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				100			100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				-0.4			-0.4	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			35	60		35	60	mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
[‡]All typical values are at V_{CC} = 5 V, T_A = 25°C.
[§]Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
NOTE 2: I_{CC} is measured with the write-enable and chip-select inputs grounded, all other inputs at 4.5 V, and all outputs open.

switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54LS289A SN54LS319A			SN74LS289A SN74LS319A			UNIT
			MIN	TYP[‡]	MAX	MIN	TYP[‡]	MAX	
$t_{a(ad)}$	Access time from address			50	90		50	80	ns
$t_{a(S)}$	Access time from chip select (enable time)	C_L = 45 pF, R_L = 667Ω, See Note 3		35	70		35	60	ns
t_{SR}	Sense recovery time			55	100		55	90	ns
t_{PLH}	Propagation delay time, low-to-high-level output (disable time)	from $\overline{S}$		30	60		30	50	ns
		from R/$\overline{W}$		40	70		40	60	

[‡]All typical values are at V_{CC} = 5 V, T_A = 25°.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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