A Course End Project Report on

SISO Shift Register Using D Filp Flop

A8431 - CMOS VLSI Design Laboratory

Submitted by

Batch No. 22CVDC08

B. Praveen Kumar Roll No - 22881A04D4

Course Facilitator

Dr.B.Srikanth
Assistant Professor

Department of Electronics and Communication Engineering Vardhaman College of Engineering, Hyderabad

April 2025

Contents

Abstract

In digital systems and communication, efficient data storage and transfer are crucial for per- formance optimization. One widely used building block in sequential logic circuits is the **SISO (Serial-In Serial-Out) Shift Register**, which allows for the storage and shifting of data in a sequential manner. This project focuses on the design and implementation of a **SISO Shift Register using D Flip-Flops**, developed and verified in the Cadence Virtuoso environment for CMOS VLSI design.

The SISO shift register employs D flip-flops to store the input data bit by bit, shifting the data serially on each clock cycle. The design is optimized using CMOS logic principles to achieve high-speed operation and low power consumption, ensuring it is suitable for integration into applications such as data buffers, serial communication, and digital signal processing.

This project demonstrates the implementation of a fundamental digital circuit within the Cadence Virtuoso toolset, focusing on both its functional correctness and its performance char- acteristics. The results highlight the impact of CMOS VLSI design on achieving low-power, high-speed performance in digital circuits. Furthermore, the project lays the groundwork for future developments, such as incorporating this design into FPGA-based systems or exploring further optimizations for advanced applications in communications and signal processing.

Keywords: SISO shift register, D flip-flop, CMOS VLSI, Cadence Virtuoso, sequential logic, low-power design, digital circuit design.

1 Introduction

The **SISO (Serial-In Serial-Out) Shift Register** is an essential building block in digital systems for serial data storage and shifting. This shift register is crucial in applications that require sequential data processing, such as data buffers, serial communication, and digital signal processing. A significant advantage of the SISO shift register is its ability to shift data one bit at a time, ensuring efficient data transfer and storage with minimal hardware complexity.

The primary objective of this project is to design and implement a 4-bit **SISO Shift Reg- ister using D Flip-Flops** in CMOS technology. The design leverages D flip-flops to store the input data and shift it sequentially with each clock cycle. This project focuses on optimiz- ing the shift register for high-speed operation and low power consumption, making it ideal for integration into modern digital systems.

The design and functionality of the SISO shift register are simulated and verified using Cadence Virtuoso, employing transient analysis to ensure correct operation and performance. This implementation serves as a foundational element in VLSI design and can be further adapted for use in advanced systems such as FPGA-based designs and applications requiring high-speed, low-power circuits.

2 Literature Review

Several approaches have been proposed for the design of **SISO (Serial-In Serial-Out) Shift Registers**, ranging from simple implementations using D flip-flops to more complex designs using advanced multiplexing techniques. D flip-flops are widely regarded as the most efficient and reliable choice for shift register implementations due to their ability to store and trans- fer data with precise timing control. These registers are essential for applications in digital communication, data buffering, and sequential data processing.

CMOS-based design offers advantages such as low power consumption, high-speed opera- tion, and noise immunity, which makes it particularly suitable for portable, embedded systems, and high-performance applications. Moreover, the use of Cadence Virtuoso for simulation and verification allows for accurate modeling and performance analysis of the shift register under real-world conditions, ensuring functional correctness and optimized design.

3 Objectives

- To design a 4-bit **SISO Shift Register using D Flip-Flops**.
- To implement the design using CMOS logic gates in a digital simulation environment (Cadence Virtuoso).
- To validate the design by observing transient waveform responses.
- To analyze timing behavior and ensure correct data shifting without glitches.
- To explore low-power, high-speed, and area-efficient implementation strategies suitable for VLSI systems.

4 Methodology

4.1 Block Diagram

The system for implementing the **SISO Shift Register** consists of the following blocks:

- **Serial Data Input (D)**: The serial data input is fed bit by bit into the shift register.

- **D Flip-Flops**: The core storage element for the shift register, responsible for holding and shifting the input data sequentially with each clock pulse.
- **Clock (CLK)**: The clock signal that controls the timing of data shifting in the register.
- **Serial Data Output (Q)**: The output that provides the shifted data one bit at a time.

4.2 Circuit Diagram and Components

4.2.1 Components Used

- Transmission Gate(TG)(CMOS Based)
- Voltage sources (for logic HIGH input)
- Ground terminals (for logic LOW)
- Inverter (CMOS Based)
- Simulation software (e.g., Cadence Virtuoso / LTspice)

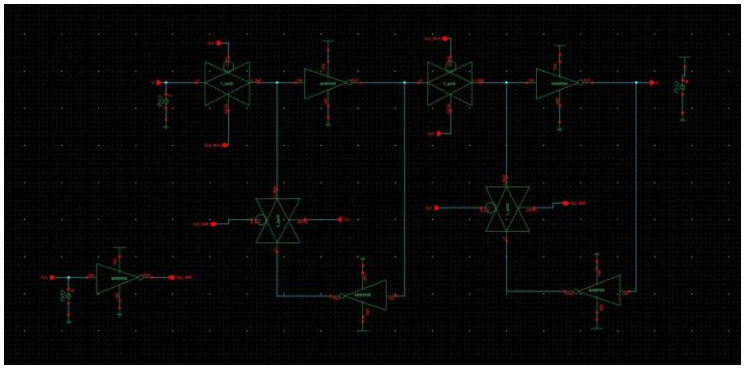

Figure 1: Circuit diagram of D Filp Flop Using TG

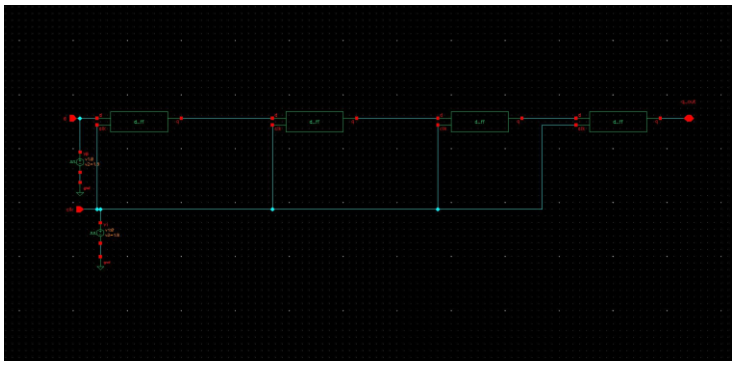

Figure 2: Circuit diagram of 4 bit SISO shift register

Figure 3 illustrates the logic circuit designed for SISO shift register using TG based D filp flop.

4.3 Working Principle

1. Four bits of serial data (D3, D2, D1, D0) are provided as input to the SISO shift register.
2. The D flip-flops store the input data sequentially on each clock cycle.

3. Each D flip-flop shifts the input data one bit at a time with each clock pulse, ensuring that the data is transferred from one flip-flop to the next.
4. The output (Q3, Q2, Q1, Q0) represents the serial data shifted through the register.

4.4 Software Tools Used

- **Cadence Virtuoso**: Used for schematic capture, layout design, and simulation of the CMOS SISO shift register, including transient analysis to verify correct functionality.
- **Digital Timing Analyzer**: Used to inspect the timing behavior, ensure glitch-free data transitions, and verify signal integrity during the shifting process.

4.5 Simulation and Verification

The circuit was simulated using a digital logic simulator to observe the timing behavior and correctness of the output.

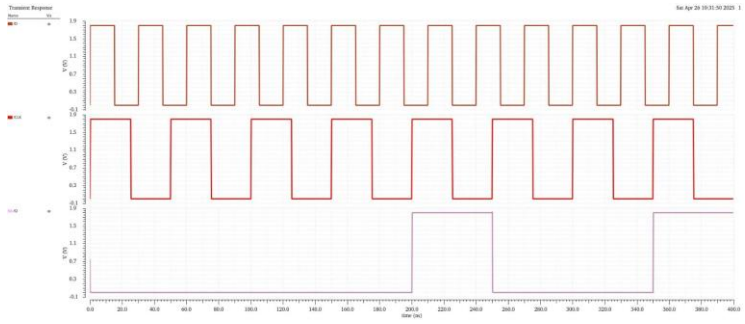

Figure 3: Transient waveform of 4bit SISO shift register using d filp flop

Figure 3 shows the transient response of the circuit.The Serial Input(SI) is given to the First d filp flop the ouput is connected to the two D filp flop so on the four D filp flop.In this date(D) is Shifted into the output(Q) on each falling clock edge(clk).Output upates only after a full clock cycle delay.

5 Results and Discussion

A SISO shift register was successfully implemented using a series of D flip-flops connected in cascade. The experimental setup included:

Input: A single serial data input.

Clock: A common clock signal fed to all flip-flops to synchronize data movement.

Output: The serial output taken from the last flip-flop. When the clock pulse was applied: The input data bit entered the first D flip-flop.

At each subsequent clock pulse, the bit moved (or ”shifted”) to the next flip-flop.

After ’n’ clock cycles (where ’n’ is the number of flip-flops), the first input bit appeared at the output.

The behavior was verified for a 4-bit SISO shift register by feeding the bit sequence 1 0 1 1. Observations were as follows:

The SISO shift register using D flip-flops demonstrated the expected behavior:

Data Movement: Each clock pulse successfully shifted the data from one flip-flop to the next, maintaining synchronization.

Clock Pulse	D-Input	Q1 (FF1)	Q2 (FF2)	Q3 (FF3)	Q4 (FF4)
1	1	1	0	0	0
2	0	0	1	0	0
3	1	1	0	1	0
4	1	1	1	0	1

Table 1: Truth table for 4-bit SISO shift register using D Flip-Flops

Data Integrity: No bit was lost or corrupted during shifting; the original input sequence was preserved at the output after the required number of clock cycles.

Timing: The shift register operation was strictly dependent on the rising (or falling) edge of the clock, as determined by the D flip-flop triggering method.

Applications: This basic SISO structure can be used for data serialization, delay generation, or simple memory storage in digital systems.

6 Mapping of Program Outcomes (POs) and Sustainable De- velopment Goals (SDGs)

6.1 Program Outcomes (POs) Mapping

The project work on SISO Shift Register contributes to several Program Outcomes as outlined below:

Table 2: Mapping of Program Outcomes (POs) to Project Relevance

PO No.	Program Outcome	Relevance to the Project
PO1	Engineering Knowledge	Applied CMOS VLSI concepts and digital logic theory in designing the shift register.
PO2	Problem Analysis	Identified the need for an efficient SISO shift register in digital systems for serial data storage and transfer.
PO3	Design/Development of Solutions	Developed the SISO shift register circuit using D flip- flops and verified the design through simulation.
PO5	Modern Tool Usage	Employed Cadence Virtuoso for schematic capture, simulation, and transient analysis of the SISO shift register.
PO6	Engineer and Society	Contributed to efficient data processing in digital systems with minimal power consumption and high-speed performance.

6.2 Sustainable Development Goals (SDGs) Mapping

This project also aligns with global development priorities as stated in the United Nations Sustainable Development Goals:

Table 3: Mapping of Sustainable Development Goals (SDGs) to Project Relevance

SDG No.	Goal	Relevance to the Project
SDG 9	Industry, Innovation, and Infrastructure	Supports reliable data processing and automation in digital systems through efficient logic design.
SDG 4	Quality Education	Encourages learning and innovation in VLSI design through practical application of theoretical knowledge.
SDG 12	Responsible Consumption and Production	Promotes efficient logic usage in hardware design, minimizing unnecessary complexity and resource usage.

Bibliography

[1] S. Brown and Z. Vranesic, *Fundamentals of Digital Logic with Verilog Design*, McGraw-Hill Education, 3rd ed., 2018.

[2] M. Morris Mano and Michael D. Ciletti, *Digital Design: With an Introduction to the Verilog HDL*, Pearson, 5th ed., 2017.

[3] P. Saxena and V. Rao, ”Application of Shift Registers in Digital Systems and Communi- cation,” *International Journal of Engineering and Technology*, vol. 11, no. 2, pp. 112–117, 2021.

[4] Cadence Design Systems, ”Cadence Virtuoso,”

[5] K. Ramesh and A. Venkat, ”Implementation of Shift Register Using CMOS Logic for Low- Power Applications,” *International Journal of VLSI Design & Communication Systems*, vol. 14, no. 1, pp. 10–15, 2021.