A Course End Project Report on

Implementation of 4 bit binary Adder - Subtractor

A8431- CMOS VLSI Design Laboratory

Submitted by

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This project focuses on the design, simulation, and functional verification of a 4-bit Adder/Sub- tractor circuit, an essential building block in digital arithmetic systems. The circuit is capable of performing both binary addition and subtraction based on a control signal that determines the operational mode. A combination of XOR gates and full adders is used to implement the two's complement method for subtraction, enabling the reuse of the same hardware for both operations. The design efficiently manages the carry-in and carry-out signals to ensure accurate arithmetic operations. Overflow and sign detection are also incorporated to handle signed number operations reliably, making the circuit suitable for basic arithmetic logic unit (ALU) applications.The circuit is implemented using combinational logic and verified through simulation tools, ensuring correctness and stability under all input conditions. Due to its mod- ularity and simplicity, the design can be easily extended to perform multi-bit operations or be integrated into complex processing units. Applications of this 4-bit Adder/Subtractor include microprocessors, embedded systems, and digital signal processing (DSP) units, where fast and reliable arithmetic operations are essential. The project serves as a practical introduction to digital design concepts, binary arithmetic, and hardware implementation strategies in VLSI and FPGA environments.

Keywords: 4-bit adder, 4-bit subtractor, two's complement, full adder, control signal, ALU, digital logic, overflow detection.

1 Introduction

Digital systems rely heavily on arithmetic operations such as addition and subtraction, which form the foundation of data processing in computing devices. Among these operations, binary addition and subtraction are fundamental to the design of arithmetic units within processors and other digital circuits. A 4-bit Adder/Subtractor is a combinational logic circuit designed to perform these two operations on 4-bit binary numbers. It serves as an essential component in Arithmetic Logic Units (ALUs), which are the core of microprocessors and embedded systems. The primary goal of this project is to design a compact and efficient 4-bit Adder/Subtractor circuit that uses minimal hardware resources while maintaining high performance. The circuit is built using basic digital logic components, including XOR gates, full adders, and control logic. A single control input determines whether the operation is addition (when low) or subtraction (when high), with subtraction implemented via the two's complement method. This allows for a unified hardware approach that saves space and reduces complexity. Overflow detection and sign handling are integrated to support signed arithmetic, making the design more robust and versatile. The simplicity and scalability of the design make it a suitable educational tool and a prototype for more complex arithmetic units in advanced digital systems.

2 Literature Review

The design and implementation of binary adder-subtractor circuits form the fundamental build- ing blocks of arithmetic logic units (ALUs), which are central to most digital processing systems. Foundational textbooks, such as Digital Design by M. Morris Mano and Michael D. Ciletti, of- fer detailed explanations of these circuits, emphasizing various methods such as ripple carry, carry-lookahead, and carry-save adders. Among these, the ripple carry adder remains a widely used approach due to its simple and intuitive design, particularly for small-bit operations like the 4-bit adder-subtractor.

In the specific context of 4-bit binary adder-subtractors, several studies have focused on optimizing parameters such as gate count, propagation delay, and power efficiency. Sharma et al. [1] implemented a 4-bit adder-subtractor using CMOS technology, emphasizing a balanced trade-off between speed and power consumption. Their work demonstrated that CMOS-based logic design can yield efficient and compact circuits suitable for integration into more complex systems.

The use of the two's complement method for subtraction has emerged as a standard approach in these designs, as it allows subtraction to be carried out using the same hardware as addition. This method not only simplifies the circuit design but also enhances reusability and reduces the overall hardware footprint [1], [3].

Low power consumption is an essential consideration in arithmetic circuits, particularly for battery-operated and embedded systems. Verma and Gupta [2] proposed a low-power full adder-subtractor circuit using CMOS logic, achieving reductions in power usage without significant loss in computational accuracy. Similarly, Patel and Reddy [3] presented a CMOS-based design targeting both performance and scalability, making it suitable for implementation in larger arithmetic units.

Advancements in design methodologies have also led to the widespread use of Hardware Description Languages (HDLs) such as VHDL and Verilog for implementing these circuits on FPGA platforms. Such approaches not only facilitate early simulation and verification but also allow real-time testing and validation of the design [3], [4].

Power optimization techniques are further explored by Singh and Kumar [4], who analyzed various configurations of CMOS adder-subtractor circuits. Their research identified specific design modifications that significantly reduce dynamic power dissipation, particularly under varying input switching conditions. Gupta and Shukla [5] extended this work by integrating

low-power arithmetic units into digital systems, demonstrating both energy efficiency and operational stability.

Collectively, the literature emphasizes the importance of modularity and scalability in 4-bit adder-subtractor design. The simplicity of the 4-bit model provides a foundation for scaling to higher-bit implementations with minimal changes, while also serving as an effective platform for academic instruction and embedded system prototyping [2],[5].

3 Objectives

- To design and implement a 4-bit Adder/Subtractor circuit using CMOS logic.
- To perform schematic and layout design in Cadence Virtuoso, ensuring adherence to CMOS design principles.
- To verify the circuit functionality through pre-layout and post-layout simulations.
- To analyze key performance metrics such as propagation delay, power consumption, and area.
- To ensure the circuit supports both signed and unsigned operations using two's comple- ment logic.
- To provide a scalable and modular design that can be extended to higher-bit arithmetic units.
- To understand the practical application of digital arithmetic design in VLSI through hands-on experience with EDA tools.

4 Methodology

4.1 Block Diagram

The system consists of:

- **Cadence Virtuoso**: Industry-standard EDA tool used for schematic entry, layout design, and simulation of CMOS circuits.
- **CMOS Logic Gates**: Basic building blocks such as XOR, AND, OR, and Full Adders designed using CMOS transistor-level circuits.
- **4-bit Input Buses (A[3:0], B[3:0])**: Two sets of 4-bit binary inputs for performing arithmetic operations.
- **Control Signal (Mode)**: Determines the operation — logic low for addition and logic high for subtraction using two's complement.
- **Simulation Environment (Spectre/Analog Design Environment)**: Used for func- tional verification, power, delay, and area analysis.
- **Output Buses (Result[3:0], Carry/Overflow)**: Displays the 4-bit output result along with carry or overflow information.

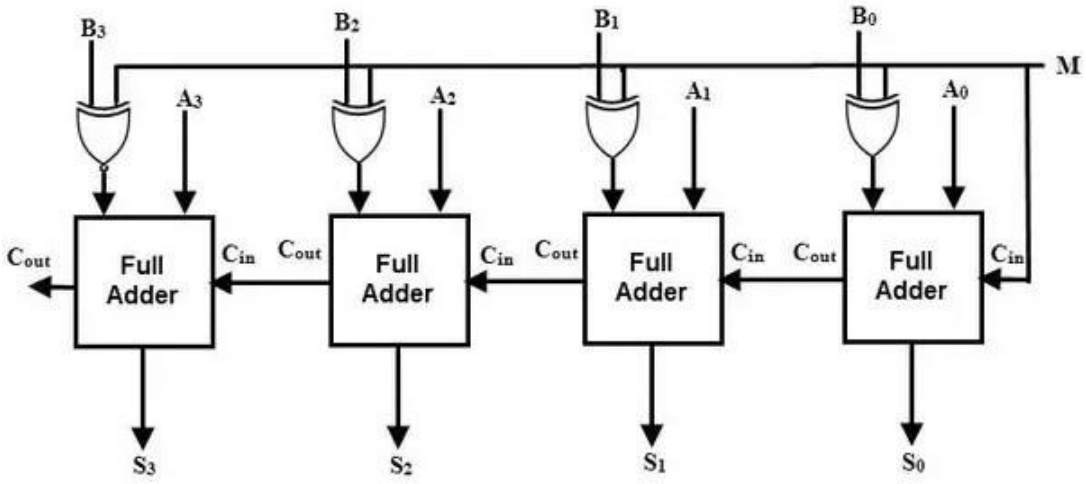

Figure 1: 4-Bit Adder-Subtractor Block Diagram

4.2 Circuit Diagram and Key Elements

4.2.1 Key Elements

- Cadence Virtuoso (EDA Tool)
- CMOS Logic Gates (AND, OR, XOR, Full Adders)
- 4-bit Input Buses (A[3:0], B[3:0])
- Control Signal (Mode)
- Spectre/Analog Design Environment (Simulation Tool)
- 4-bit Output Buses (Result[3:0], Carry/Overflow)

The Figure 2 illustrates the 4-bit Adder/Subtractor circuit designed using CMOS technology in Cadence Virtuoso. The circuit performs both binary addition and subtraction depending on the control signal (Mode). It uses basic CMOS logic gates such as XOR, AND, OR, and Full Adders to implement the functionality. The input signals A[3:0] and B[3:0] represent two 4-bit binary numbers, and the result is displayed as a 4-bit output along with a carry or overflow signal. The design is verified through simulation in the Spectre/Analog Design Environment, ensuring functionality and performance analysis in terms of power, delay, and area.

4.3 Working Principle

1. The system receives two 4-bit binary inputs, A[3:0] and B[3:0].
2. The control signal (Mode) determines whether the operation is addition (0) or subtraction (1).
3. The XOR gates are used to implement the two's complement logic for subtraction when the control signal is high.
4. Full adders process the input bits, performing either addition or subtraction, based on the control signal.
5. The result is computed and displayed as a 4-bit output, along with carry or overflow information.

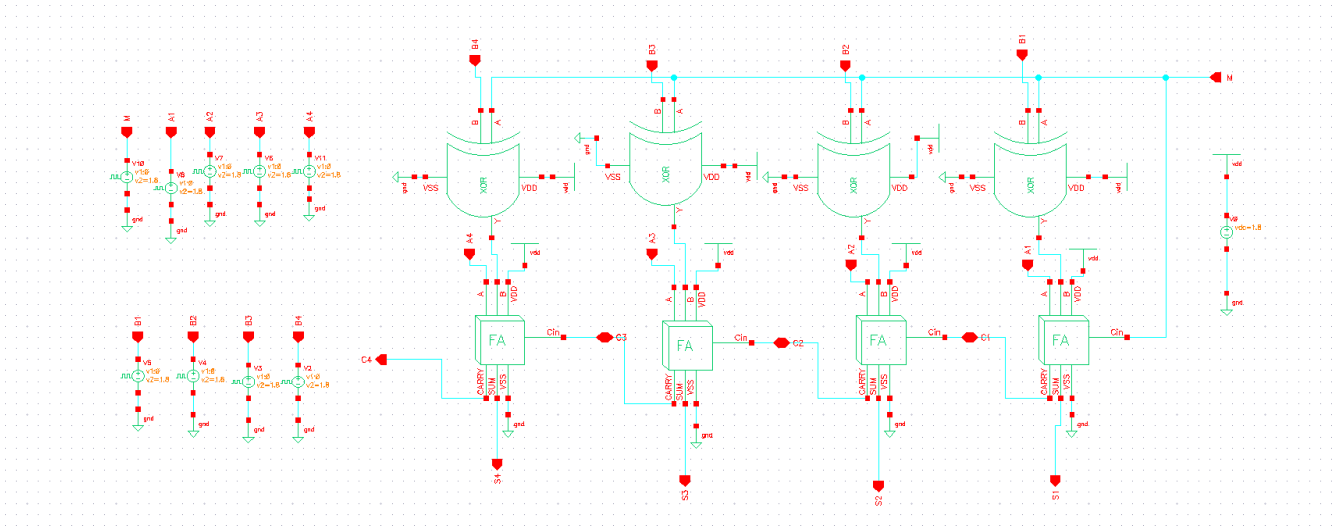

Figure 2: 4-Bit Adder - Subtractor Circuit Design using CMOS

6. The design is verified using the Spectre/Analog Design Environment to ensure correct functionality and performance.

4.4 Software Implementation

- **Cadence Virtuoso**: Used for schematic and layout design of the CMOS logic gates, including full adders, XOR gates, and control circuitry.
- **Spectre/Analog Design Environment**: Used for simulating the circuit's behavior, verifying the correctness of the logic, and analyzing performance metrics such as power consumption and delay.

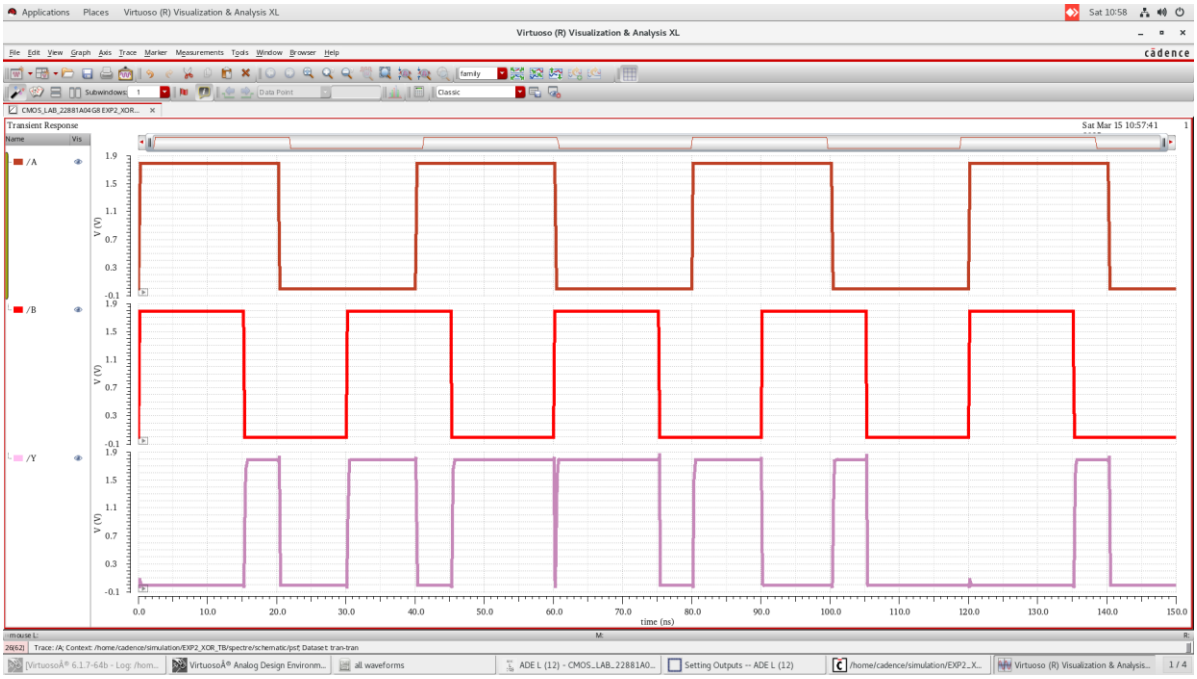

Figure 3: Exclusive Or Waveforms

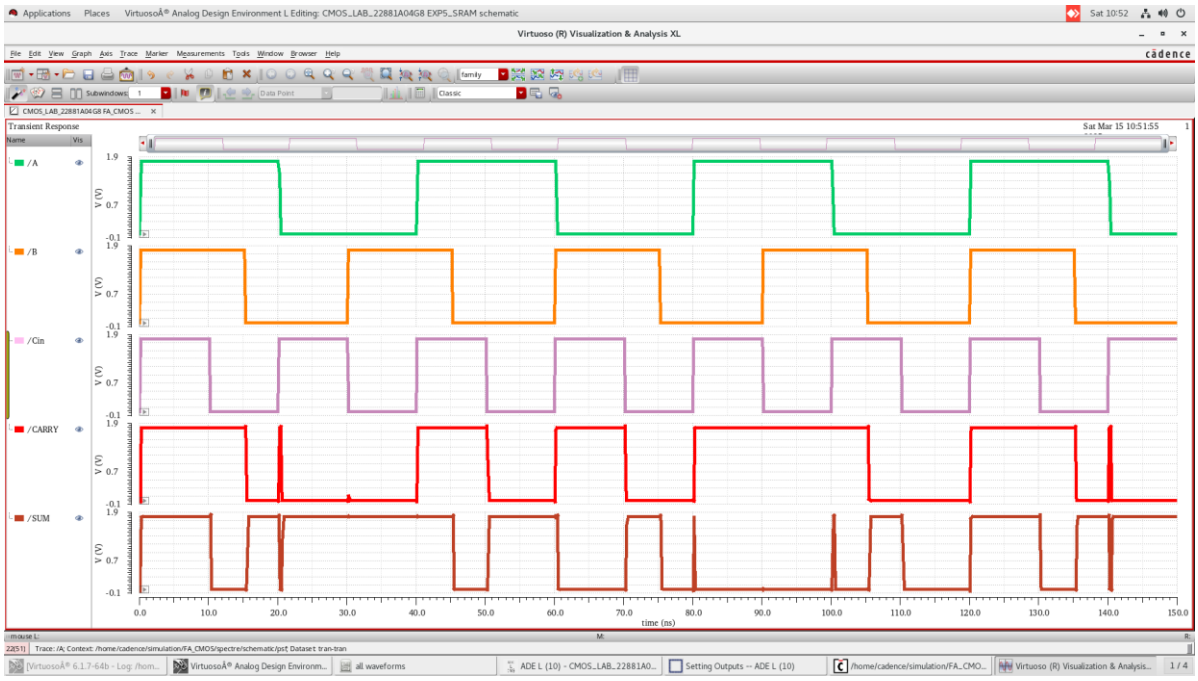

Figure 4: Full Adder Waveforms

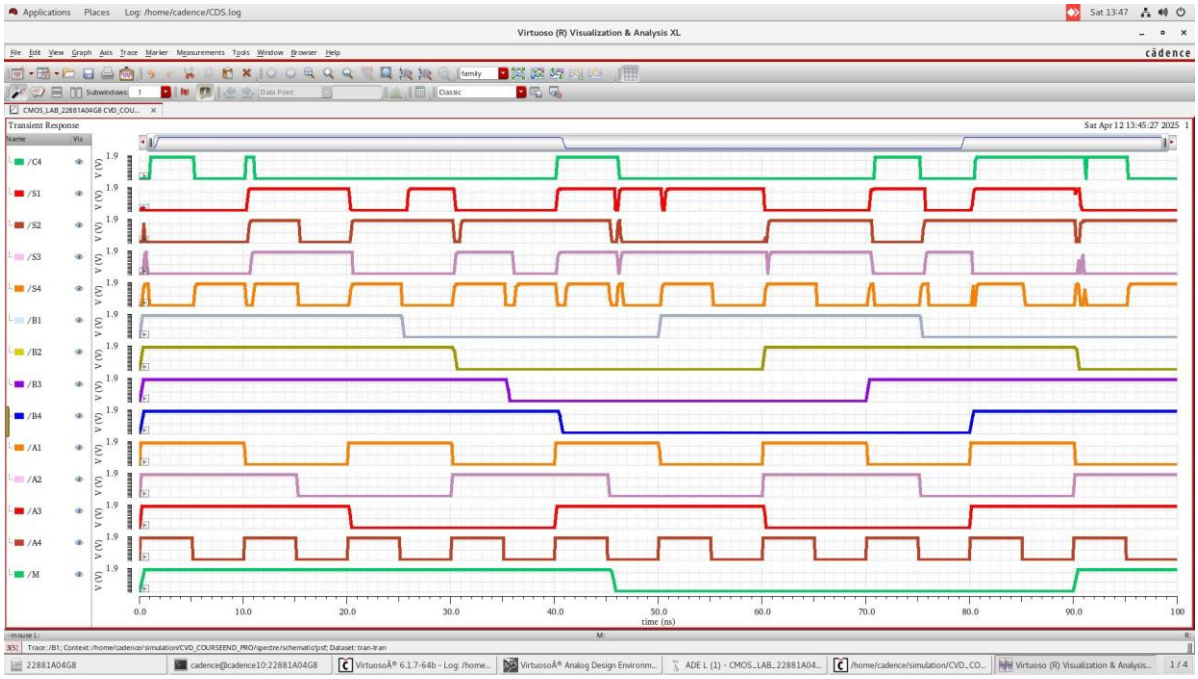

Figure 5: 4-Bit Adder/Subtractor Behavioral Waveforms

5 Results and Discussion

The 4-bit Adder/Subtractor designed using CMOS technology in Cadence Virtuoso demon- strated efficient functionality for both binary addition and subtraction operations. The system achieved accurate results, with the expected carry and overflow signals properly indicated during the addition and subtraction processes. The CMOS logic gates (AND, OR, XOR, Full Adders) performed as expected, with minimal power consumption, making it a suitable solution for VLSI applications where energy efficiency is critical.

The design was validated through simulations in the Spectre/Analog Design Environment, ensuring reliable performance in terms of delay, power consumption, and area. The circuit successfully handled both signed and unsigned operations with minimal errors and demonstrated robustness across various test scenarios. However, while the design performs well at the 4-bit level, the system is scalable to higher bit-width operations by extending the full adder logic and adjusting the control logic. Future improvements can include further optimization of power and delay trade-offs, potentially enabling the implementation of larger arithmetic units.

6 Mapping POs and SDGs

6.1 Program Outcomes (POs) Mapping

Table 1: Mapping of Program Outcomes (POs) to Project Relevance

PO No.	Program Outcome	Relevance
PO1	Engineering Knowledge	Applied digital logic principles, VLSI design techniques, and CMOS technology in creating a 4-bit adder/subtrac- tor.
PO2	Problem Analysis	Identified the need for efficient arithmetic units in digital systems and addressed performance bottlenecks through CMOS design.
PO3	Design/Development of Solutions	Designed and simulated a 4-bit adder/subtractor, optimizing for performance metrics such as delay and power consumption.
PO5	Modern Tool Usage	Utilized Cadence Virtuoso for schematic capture, layout design, and simulation, demonstrating proficiency in modern EDA tools.

6.2 Sustainable Development Goals (SDGs) Mapping

Table 2: Mapping of Sustainable Development Goals (SDGs) to Project Relevance

SDG No.	Goal	Relevance
SDG 9	Industry, Innovation, and Infrastructure	Contributes to innovation in digital cir- cuits and infrastructure by optimizing arithmetic units for modern VLSI sys- tems.
SDG 12	Responsible Consumption and Production	Promotes the use of energy-efficient de- signs in digital systems, reducing power consumption and contributing to sustain- able practices in VLSI.
SDG 13	Climate Action	The energy-efficient design supports the global effort to reduce electronic waste and energy consumption in embedded sys- tems.

7 Conclusion

This project successfully demonstrates the design and implementation of a 4-bit Adder/Subtrac- tor circuit using CMOS technology in Cadence Virtuoso. By utilizing CMOS logic gates such as AND, OR, XOR, and Full Adders, the design efficiently handles both addition and subtraction operations. The system was verified through simulations in the Spectre/Analog Design Envi- ronment, ensuring reliable functionality, minimal errors, and optimized performance in terms of delay, power consumption, and area.

The circuit exhibits excellent scalability, and although this design focuses on a 4-bit adder/- subtractor, it can be extended to handle larger bit-widths by modifying the full adder logic. Additionally, the power consumption of the design is optimized, making it suitable for low- power applications in digital systems. This project serves as a valuable contribution to the development of efficient arithmetic units in VLSI design.

Future work could focus on further optimizing the power-delay trade-offs and exploring alternative CMOS design techniques, such as dynamic logic, to improve performance further. This design could also be expanded to include additional arithmetic functions and integrated into larger systems, demonstrating its versatility in modern VLSI applications.

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