A Course End Project Report on

Design and Implementation of a Binary to Gray Code and Gray to Binary Code Converter

A8431 - CMOS VLSI Design Laboratory

Submitted by

B. Praveen Kumar Roll No - 22881A04D4

Course Facilitator

Dr. B. Srikanth
Assistant Professor

Department of Electronics and Communication Engineering
Vardhaman College of Engineering, Hyderabad

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Abstract

In digital systems, efficient data encoding techniques are crucial for error reduction and optimized performance. The Gray code is one such encoding method, where only one bit changes between consecutive values, minimizing errors and improving reliability in digital circuits. This project focuses on the design and implementation of both a **Binary to Gray Code Converter** and a **Gray to Binary Code Converter** using CMOS technology.

The Binary to Gray Code Converter takes binary input and generates the corresponding Gray code output, while the Gray to Binary Code Converter performs the inverse operation. Both converters are designed using optimized digital logic principles to achieve low power consumption and high-speed performance, making them suitable for applications in memory addressing, rotary encoders, and error detection and correction systems.

The project emphasizes the practical application of these converters in VLSI design, with simulations and validation performed to verify the functionality and performance of the circuits. The results showcase the efficiency of CMOS logic in implementing these converters. Additionally, this work lays the groundwork for future improvements, such as integration into FPGA platforms or exploration of power-efficient reversible logic techniques.

Keywords: Binary to Gray code converter, Gray to Binary code converter, CMOS VLSI, digital logic design, low-power circuits, encoder, reversible logic.

1 Introduction

Binary to Gray code and Gray to Binary code conversions are fundamental operations in digital systems, especially in communication and error correction applications. Gray code is valued for its unique property, where only one bit changes between consecutive values, minimizing errors during data transmission and synchronization. This project focuses on the design and implementation of both a 4-bit **Binary to Gray Code Converter** and a **Gray to Binary Code Converter** using CMOS XOR logic gates. The design is simulated and tested for correct functionality using transient analysis. These converters are essential in applications such as rotary encoders, memory addressing, and error detection circuits, where minimizing bit transitions is critical.

2 Literature Review

Various methods for Binary to Gray code and Gray to Binary code conversion have been explored, with solutions ranging from software algorithms to hardware-based designs using multiplexers and combinational logic. XOR-based logic implementations are popular due to their simplicity, reliability, and hardware efficiency. For Gray to Binary conversion, the reverse operation of the Binary to Gray converter can also be efficiently implemented using XOR gates. Gray code is particularly useful in systems where bit changes during transitions can lead to errors, such as in digital communication and synchronization applications.

CMOS-based circuit design is preferred due to its low power consumption and better noise immunity, making it ideal for modern portable and embedded systems. Furthermore, CMOS logic circuits are scalable, providing an advantage for high-performance applications in VLSI designs. The combination of CMOS technology with these encoding methods ensures efficient power usage, making these converters suitable for integration into real-world systems like memory devices, sensors, and signal processing units.

3 Objectives

- To design a 4-bit **Binary to Gray Code Converter** and a 4-bit **Gray to Binary Code Converter** using XOR logic.
- To implement the design using CMOS logic gates in a digital simulation environment.
- To validate both converters by observing transient waveform responses.
- To analyze timing behavior and ensure glitch-free output transitions for both converters.
- To explore low-power and area-efficient implementation strategies suitable for VLSI systems.

4 Methodology

4.1 Block Diagram

The system for converting Binary code to Gray code and Gray code to Binary code consists of the following blocks:

- **Binary Inputs (B0-B3)**: 4-bit binary input values for the Binary to Gray code conversion.

- **XOR Logic Units**: XOR gates used to generate the Gray code outputs from binary inputs in the Binary to Gray code converter, and vice versa in the Gray to Binary code converter.
- **Gray Code Outputs (G0-G3)**: The converted 4-bit Gray code output from the Binary to Gray code converter.
- **Binary Code Outputs (B0-B3)**: The converted 4-bit binary output from the Gray to Binary code converter.

4.2 Circuit Diagram and Components

4.2.1 Components Used

- XOR logic gates (CMOS based)
- Voltage sources (for logic HIGH input)
- Ground terminals (for logic LOW)
- Simulation software (e.g., Cadence Virtuoso / LTspice)

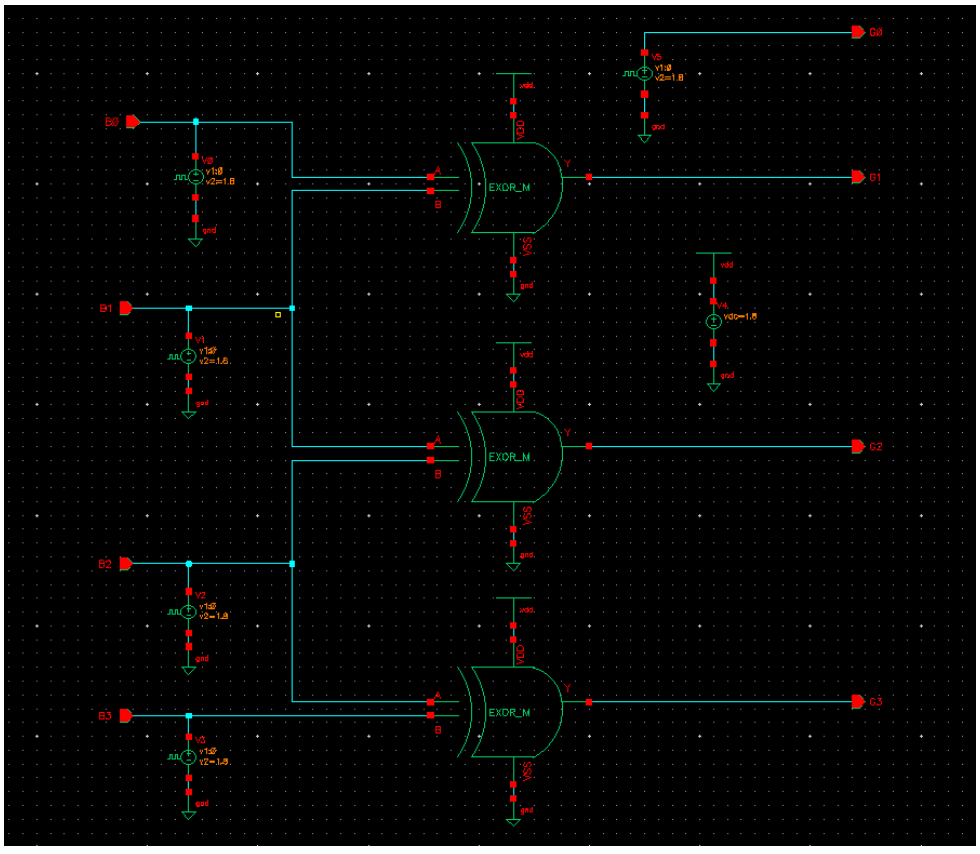

Figure 1: Circuit diagram of 4-bit Binary to Gray code converter

Figure 1 illustrates the logic circuit designed for converting a 4-bit binary input to its corresponding Gray code using XOR gates. This configuration is part of the dual-purpose system aimed at enabling bidirectional conversion between Binary and Gray codes. The logic used for Binary to Gray conversion adheres to the standard transformation rules:

$$Gray_3 = Binary_3 Gray_2 = Binary_3 \oplus Binary_2 Gray_1 = Binary_2 \oplus Binary_1 Gray_0 = Binary_1 \oplus Binary_0 \quad (1)$$

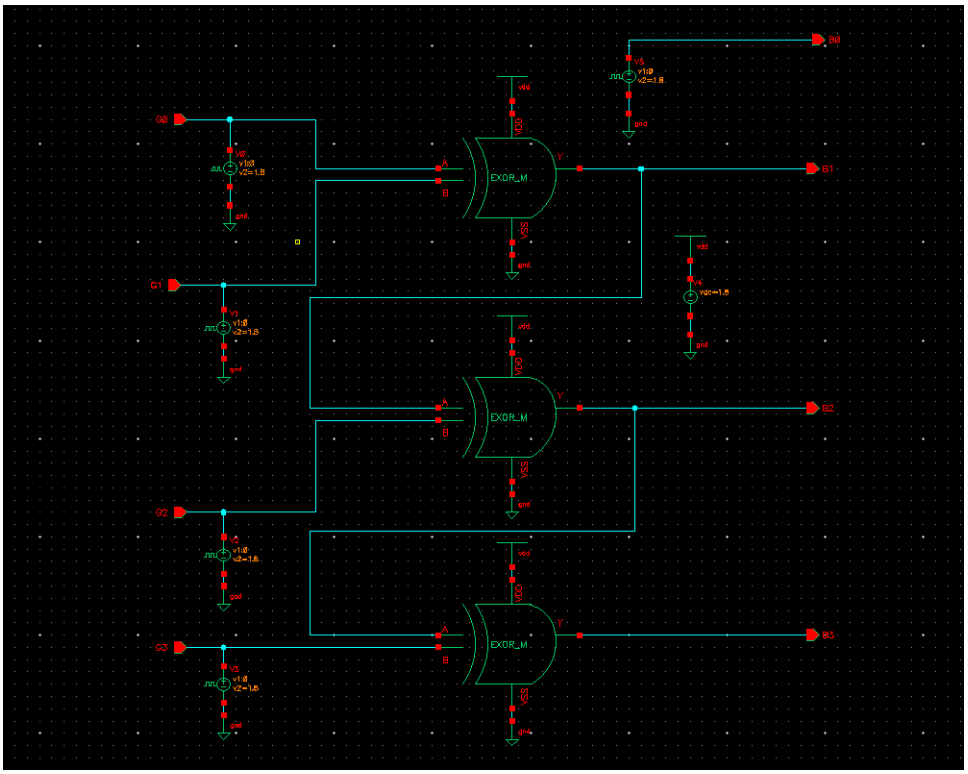

Figure 2: Circuit diagram of 4-bit Gray to Binary code converter

4.3 Working Principle

1. A 4-bit binary input (B3, B2, B1, B0) is provided to the circuit.
2. The most significant bit (MSB) of the Gray code output is directly taken from the MSB of the binary input.
3. Each of the remaining Gray bits is generated by XOR-ing the current binary bit with the bit immediately preceding it.
4. The resulting output (G3, G2, G1, G0) forms the 4-bit Gray code equivalent of the given binary input.

4.4 Software Tools Used

- **Cadence Virtuoso / LTspice**: Employed for schematic design, circuit simulation, and transient response analysis of the XOR-based converter.
- **Digital Timing Analyzer**: Utilized to verify signal integrity, monitor timing behavior, and ensure glitch-free transitions.

4.5 Simulation and Verification

The Binary to Gray code converter was simulated using a digital logic simulation environment. The timing behavior, transition delays, and output correctness were observed under various input conditions to ensure accurate Gray code generation. The simulation results confirmed the correct functionality of the designed circuit across all 4-bit binary inputs.

5 Results and Discussion

The designed Binary to Gray code converter was successfully implemented using XOR logic gates, and its functionality was verified through simulation. The circuit effectively converts a 4-bit binary input into the corresponding Gray code output.

Figure 3 presents the transient response of the system. It can be observed that the Gray code output changes in accordance with the XOR logic applied to the binary inputs:

- $G_3 = B_3$
- $G_2 = B_3 \oplus B_2$
- $G_1 = B_2 \oplus B_1$
- $G_0 = B_1 \oplus B_0$

The waveform clearly demonstrates that for every valid 4-bit binary input, the corresponding Gray code output transitions correctly, with only one bit changing between successive values—this confirms adherence to the fundamental property of Gray coding.

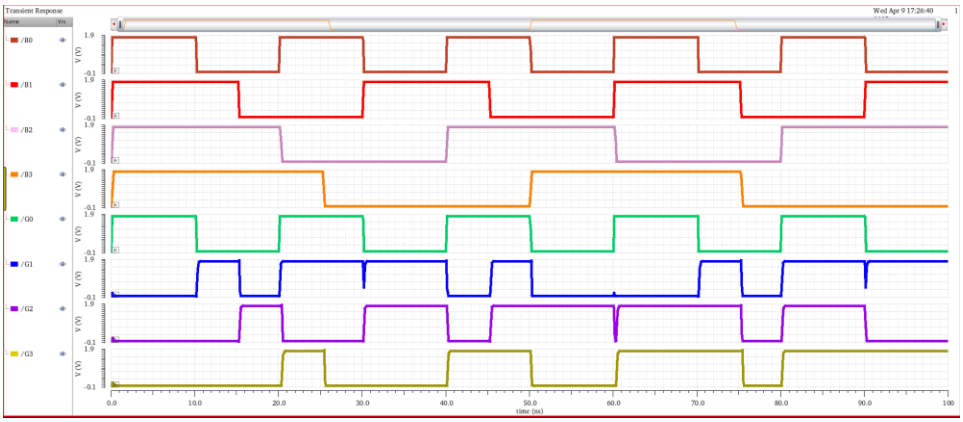

Figure 3: Transient waveform of 4-bit Binary to Gray code converter

Figure 4 shows the transient response of the Binary to Gray code converter circuit. As observed from the simulation, for each transition in the binary input, only a single bit changes in the Gray code output. This behavior validates the fundamental property of Gray codes and confirms the correct functional implementation of the converter.

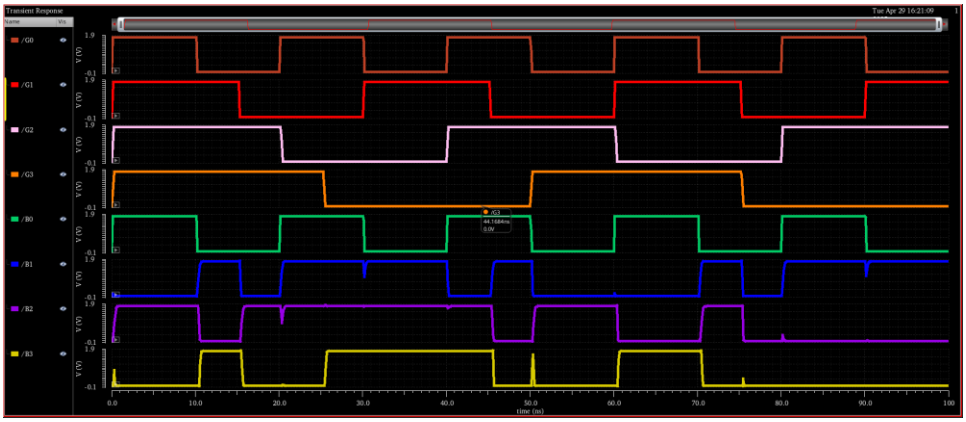

Figure 4: Transient waveform of 4-bit Gray to Binary code converter

6 Mapping of Program Outcomes (POs) and Sustainable Development Goals (SDGs)

6.1 Program Outcomes (POs) Mapping

Table 1: Mapping of Program Outcomes (POs) to Project Relevance

PO No.	Program Outcome	Relevance to the Project
PO1	Engineering Knowledge	Applied CMOS VLSI design concepts and digital logic fundamentals in the development of a real-world logic converter.
PO2	Problem Analysis	Identified the practical requirement for reliable Binary to Gray code conversion in digital communication and memory addressing.
PO3	Design/Development of Solutions	Designed and implemented a 4-bit logic converter circuit using XOR gates and validated through simulation.
PO5	Modern Tool Usage	Utilized LTspice/Cadence Virtuoso for schematic design, simulation, and timing verification.
PO6	Engineer and Society	Contributed to the advancement of secure and optimized digital systems through efficient code conversion methods.

6.2 Sustainable Development Goals (SDGs) Mapping

Table 2: Mapping of Sustainable Development Goals (SDGs) to Project Relevance

SDG No.	Goal	Relevance to the Project
SDG 9	Industry, Innovation, and Infrastructure	Enhances digital system reliability and efficiency through innovative logic design techniques.
SDG 4	Quality Education	Provides a practical learning platform for students to apply digital electronics and VLSI theory.
SDG 12	Responsible Consumption and Production	Encourages minimalistic and power-efficient logic circuit design, reducing unnecessary resource usage in hardware implementations.

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