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ME 4405 Section B

Lab Assignment Four

Serial Communication Using UART

Questions:

1. Suppose you use a baud rate of 38400. How far off can the clock rate of your 2 devices be before you start reading data incorrectly? Do not use the 5% approximation, but rather compute the answer exactly. How does it compare to the 5% approximation? (10 pts)

$$T = \frac{1}{Baud\ rate} = \frac{1}{38400\frac{bits}{second}} = 2.604 * 10^{-5}\frac{seconds}{bit}$$

$$Maximum\ timing\ error = 0.5 * T = 0.5 * 2.604 * 10^{-5}\frac{seconds}{bit} = 1.3021 * 10^{-5}\frac{seconds}{bit}$$

To ensure that the data is read correctly, the difference between the amount of time required to read a byte (9 bits specifically, since the transmission of the starting bit is assumed to be in sync) of data using the actual clock rate and that using the baud rate of 38400 must be a maximum of 0.5 times the reciprocal of the baud rate:

$$Delay = \frac{0.5 * T}{9} = 1.44676 * 10^{-6}\frac{seconds}{bit}$$

$$Lower\ limit\ of\ delayed\ baud\ rate = B_{lower} = (T + Delay)^{-1} = 36378.947$$
$$Upper\ limit\ of\ delayed\ baud\ rate = B_{upper} = (T - Delay)^{-1} = 40658.824$$

$$\%\ Error, 1 = \frac{\left|B_{upper} - 38400\right|}{38400} * 100\% = \mathbf{5.882}\%$$

$$\%\ Error, 2\ = \frac{|B_{lower} - 38400|}{38400} * 100\% = \mathbf{5.263}\%$$

$Since\ (\%\ Error, 2)\ is\ less\ than\ (\%\ Error, 1)$:

$$\%\ \boldsymbol{Error} = \mathbf{5.263}\%$$

For a baud rate of 38400, the clock rate of the two devices can be a maximum of **5.263%** off from each other before the data is started to be read incorrectly. Although this value is slightly more than the 5% approximation, the 5% approximation remains to be a recommended rule to follow to ensure that the data is read correctly.

2. Suppose your clock signals differ by more than the amount in Question 1. What error flag would you expect to see, in what register? Why would this error flag get triggered in this situation? (5 pts)
   If the clock signals differ by more than the amount in Question 1, a **framing error flag** would occur in the **TXIFG register**. Because the significant difference in the clock signals would cause the entire byte in the TXBUF register to not be set in the TXIFG register properly (because the stop bit would be incorrect), the TXBUF register would never be cleared which would prevent the TXIFG register from being set.

3. How could you solve the above problem (i.e., by changing the baud rate)? What is the inherent performance penalty associated with this solution? (10 pts)
   You would solve the above problem by simply reducing the baud rate utilized for the program, thereby allowing a greater level of accuracy in exchanging data between the two devices. However, this would additionally cause data to transmit between the devices at a slower rate.