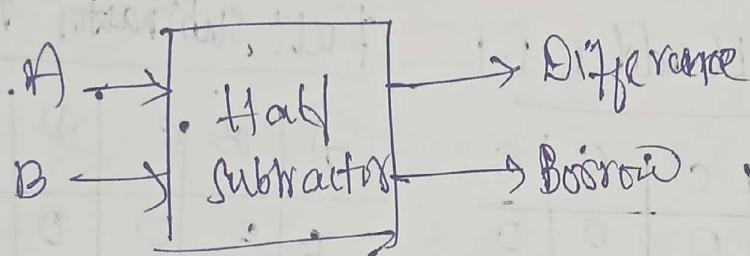


Answers to terminal QuestionsAdders & Subtractors

- 1). Draw the half subtractor principle with input, output and truth table.

Sol: Half subtractor

- Performs subtraction of 2 binary bits
- It has 2 inputs & 2 outputs

① Block Diagram② Truth table

A	B	D	B̄
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

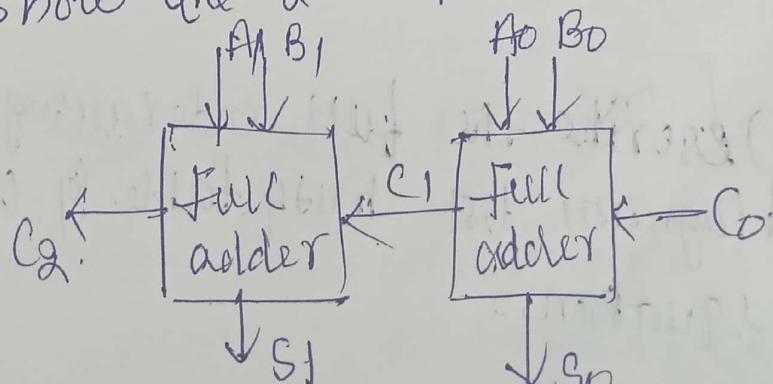
Op. Expressions

$$\text{Difference } (D) = \overline{A}B + A\overline{B} = A \oplus B$$

$$\text{Borrow } (B) = \overline{A}B$$

- 2) Show the 2-bit parallel adder circuit

Ans:



3) Show the half adder & half subtractor truth table.

Ans. Half adder T.T.      Half Subtractor T.T

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

A	B	D	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

4) Show the full adder & full subtractor truth table.

Ans. Full adder T.F

A	B	C	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Full subtractor T.F

A	B	C	D	B
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	0	1
1	0	1	0	0
1	1	0	1	0
1	1	1	1	1

L.A.G

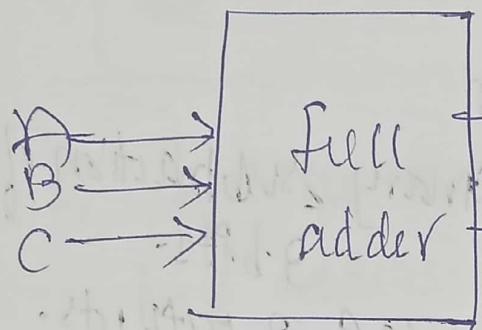
1) Describe the full adder using block diagram, list truth table & output equations.

Ans: Full adder

→ performs binary addition of 3 bits

→ It has 3 inputs & 2 outputs.

① Block Diagram



② Truth table

A	B	C	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

③ O/P Expressions

$$\text{Sum}(S) = \overline{ABC} + \overline{AB}\overline{C} + A\overline{BC} + ABC = \text{Eml}(1, 2, 4, 7)$$

$$= C(\overline{A}\overline{B} + AB) + \overline{C}(\overline{A}B + A\overline{B})$$

$$= C(A \oplus B) + \overline{C}(A \oplus B)$$

$$\text{Let } A \oplus B = X$$

$$\text{Sum} = C\overline{X} + \overline{C}X = C \oplus X$$

$$= C \oplus A \oplus B$$

Sum =  $A \oplus B \oplus C$

$$\text{Carry}(C) = \overline{ABC} + A\overline{B}\overline{C} + A\overline{BC} + \overline{AB}C = \text{Eml}(3, 5, 6, 7)$$

$$= C(\overline{A}B + A\overline{B}) + \overline{C}AB(C + \overline{C})$$

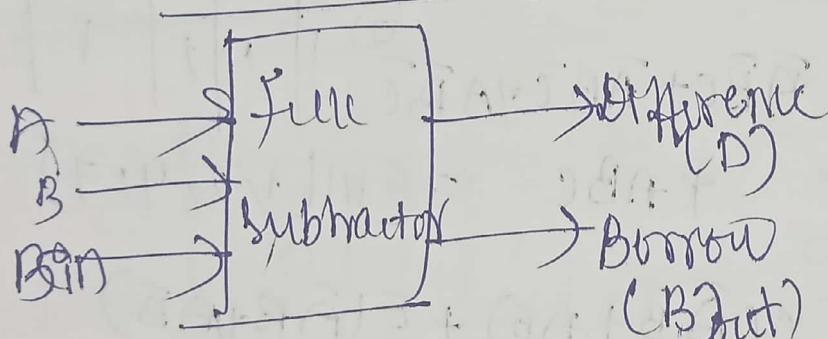
$$\text{Carry} = C(A \oplus B) + AB$$

- Q) Describe full subtractor using block diagram, list its truth table and output equations.

Ans: Full Subtractor

- It performs binary subtraction of 3 bits.
- It has 3 inputs & 2 outputs.

① Block Diagram



② Truth Table

A	B	B <sub>in</sub>	D	B <sub>out</sub>
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	1
1	1	1	1	1

③ O/P expressions

$$\text{Difference } (D) = \overline{A}\overline{B}B_{\text{in}} + \overline{A}B\overline{B}_{\text{in}}$$

$$+ A\overline{B}\overline{B}_{\text{in}} + A\overline{B}B_{\text{in}}$$

$$\therefore \text{Em}(6, 7, 14, 17)$$

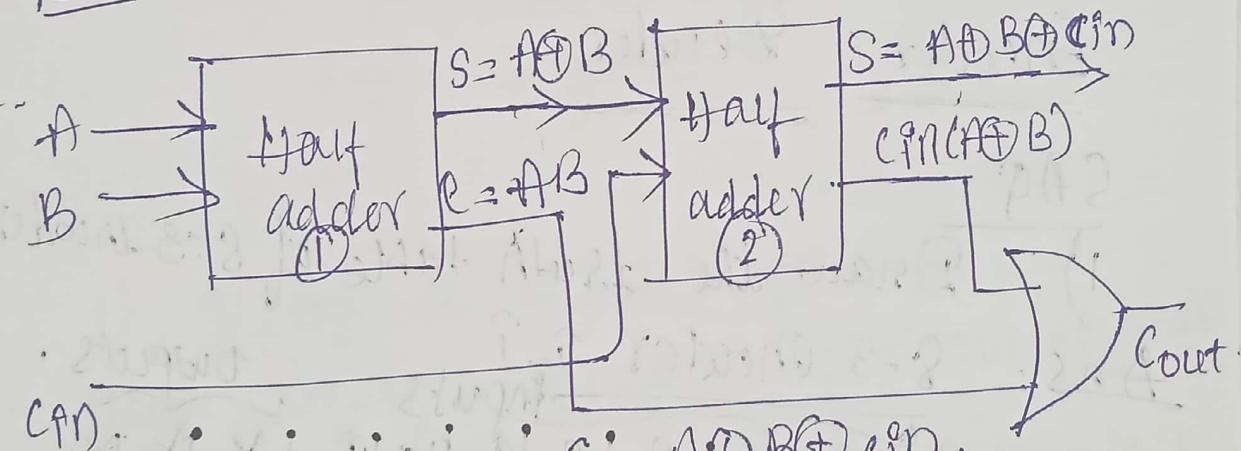
$$\therefore B_{\text{in}}(\overline{A}\overline{B} + AB) + \overline{B}_{\text{in}}(AB + A\overline{B})$$

$$\boxed{\text{Difference} = A \oplus B \oplus B_{\text{in}}}$$

$$\begin{aligned}
 B_{out} &= \bar{A}\bar{B} B_{in} + \bar{A}B \bar{B}_{in} + \bar{A}B B_{in} + \\
 &\quad A\bar{B} B_{in} \\
 &= B_{in}(\bar{A}\bar{B} + \bar{A}B) + \bar{A}B(B_{in} + \bar{B}_{in}) \\
 B_{out} &= \boxed{B_{in}(\bar{A} \oplus B) + \bar{A}B}
 \end{aligned}$$

3) Realize the full adder using two half adders.

Ans:



$$S = A \oplus B \oplus c_{in}$$

$$C_{out} = C_{in}(A \oplus B) + AB$$

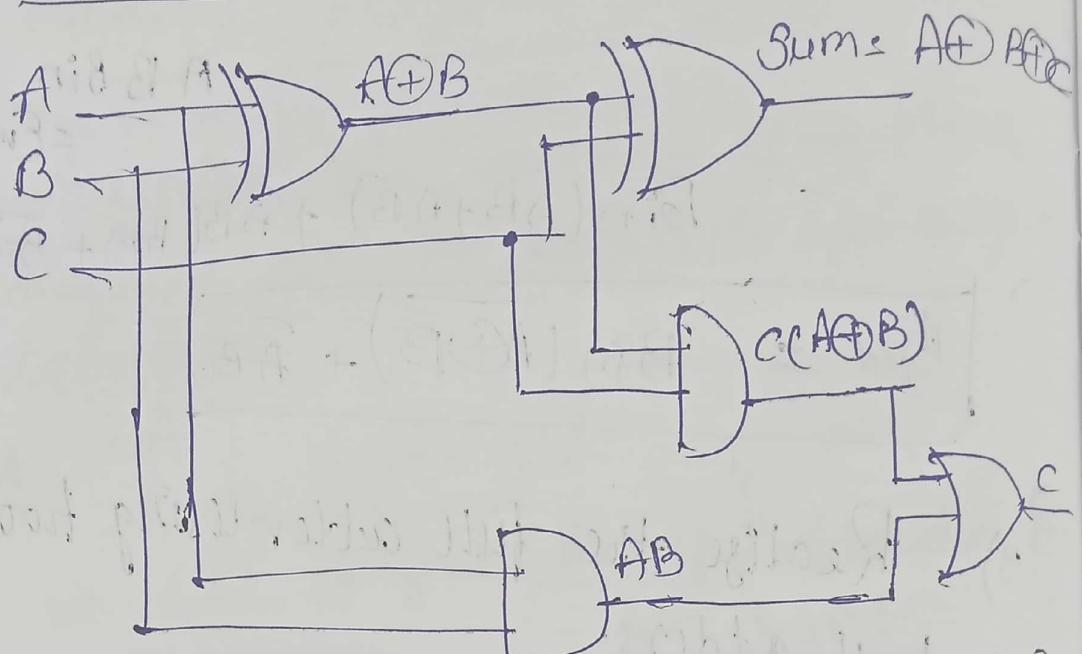
4) Realize the output functional equations of full adder using required logic gates.

Ans: For a full adder,

$$\text{Sum} = A \oplus B \oplus c$$

$$\text{Carry} = C(A \oplus B) + AB$$

## Logic circuit



$$\text{Carry} = C(A \oplus B) + AB$$

## Encoder & Decoder

### S&Q

1) Draw the truth table of 8:3 encoder.

Ans: 8-3 Encoder

		Inputs							Outputs			
$I_7$	$I_6$	$I_5$	$I_4$	$I_3$	$I_2$	$I_1$	$I_0$	$Y_2$	$Y_1$	$Y_0$		
0	0	0	0	0	0	0	0	1	0	0	0	
0	0	0	0	0	0	1	0	0	0	1		
0	0	0	0	0	0	0	0	0	0	1		
0	0	0	0	0	1	0	0	0	1	1		
0	0	0	0	1	0	0	0	0	1	0		
0	0	0	1	0	0	0	0	0	1	0		
0	0	1	0	0	0	0	0	0	0	1		
0	1	0	0	0	0	0	0	0	1	1		
1	0	0	0	0	0	0	0	0	1	1		

2) List the applications of decoder.

Ans Applications of decoder

1) Memory addressing

2) Address decoding

3) Error correction

3) List the applications of encoder.

Ans:- 1) used in printed circuit boards

AB : 2) used in calculators

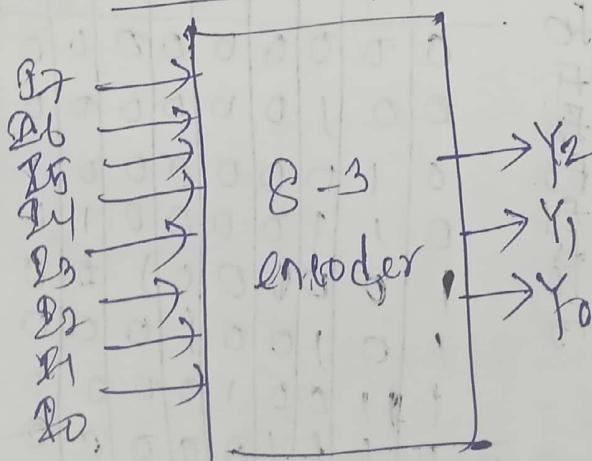
3) They can be used to generate digital signals.

LAQ

1) Design a circuit diagram for 8-to-3 line encoder, including input, output labels.

Ans:- 8-3 encoder It has 8 inputs & 3 outputs

(i) Block Diagram



(ii) Truth table

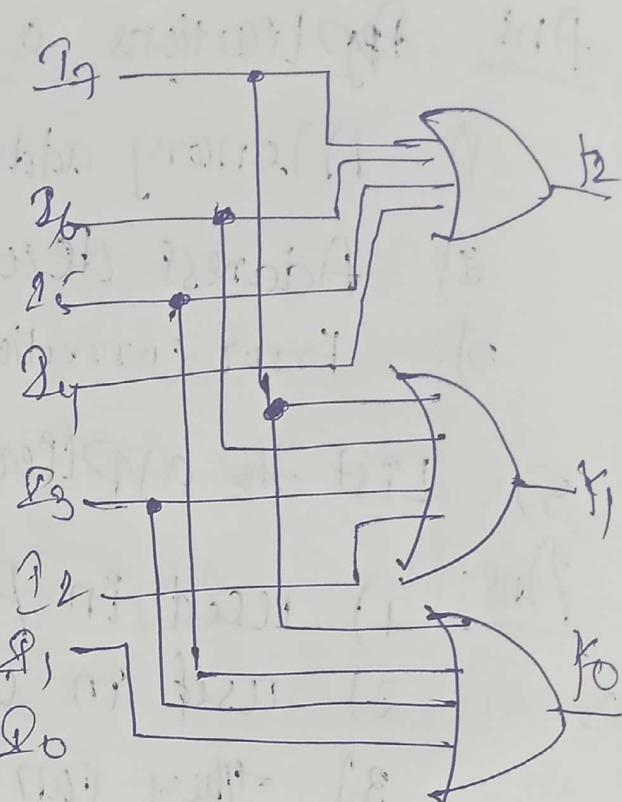
I <sub>7</sub>	I <sub>6</sub>	I <sub>5</sub>	I <sub>4</sub>	I <sub>3</sub>	I <sub>2</sub>	I <sub>1</sub>	I <sub>0</sub>	Y <sub>2</sub>	Y <sub>1</sub>	Y <sub>0</sub>
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	1	0	0
0	0	0	0	0	1	0	0	0	1	1
0	0	0	0	1	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	1	0
0	0	1	0	0	0	0	1	0	1	0
0	1	0	0	0	0	0	1	1	0	1
1	0	0	0	0	0	0	1	1	1	1

③ Output expressions      ④ Logic circuit

$$Y_2 = P_2 + P_6 + P_5 + P_4$$

$$Y_1 = P_2 + P_6 + P_3 + P_7$$

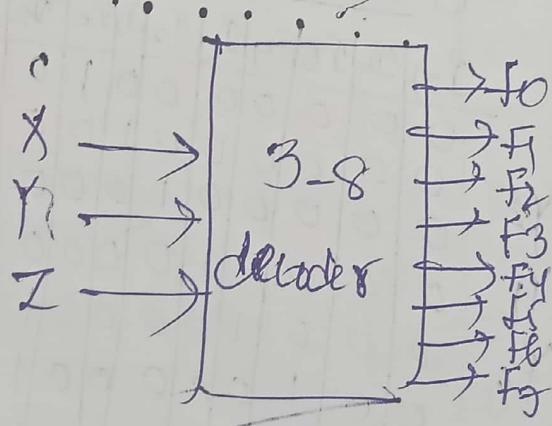
$$Y_0 = P_2 + P_5 + P_3 + P_1$$



2) Design a logic diagram for 3-to-8 DMD decoder, including input, output labels.

Ans: 3-8 decoder! It has 3 inputs & 8 outputs.

① Block Diagram



② Truth table

X	Y	Z	F <sub>7</sub>	F <sub>6</sub>	F <sub>5</sub>	F <sub>4</sub>	F <sub>3</sub>	F <sub>2</sub>	F <sub>1</sub>	F <sub>0</sub>
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	0	1	0
0	1	1	0	0	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

③ Output expressions

④ Logic circuit

$$f_0 = \bar{x}yz$$

$$f_1 = \bar{x}\bar{y}z$$

$$f_2 = \bar{x}y\bar{z}$$

$$f_3 = \bar{x}y\bar{z}$$

$$f_4 = x\bar{y}z$$

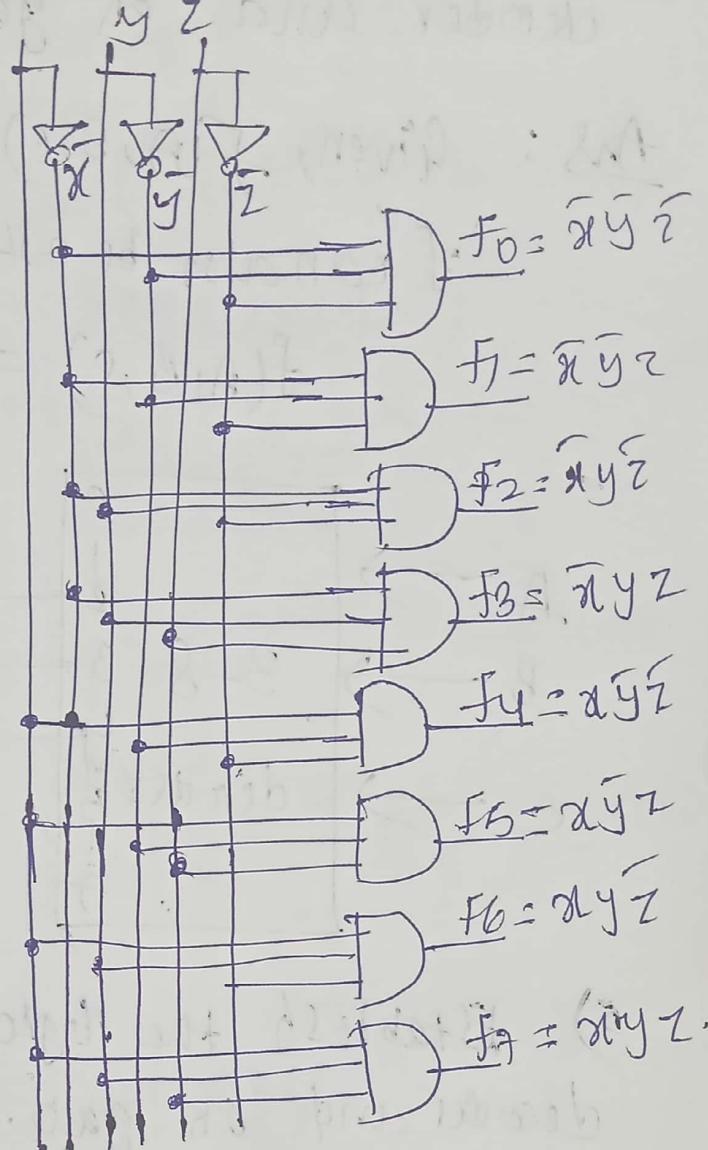
$$f_5 = x\bar{y}\bar{z}$$

$$f_6 = xy\bar{z}$$

$$f_7 = xy\bar{z}$$

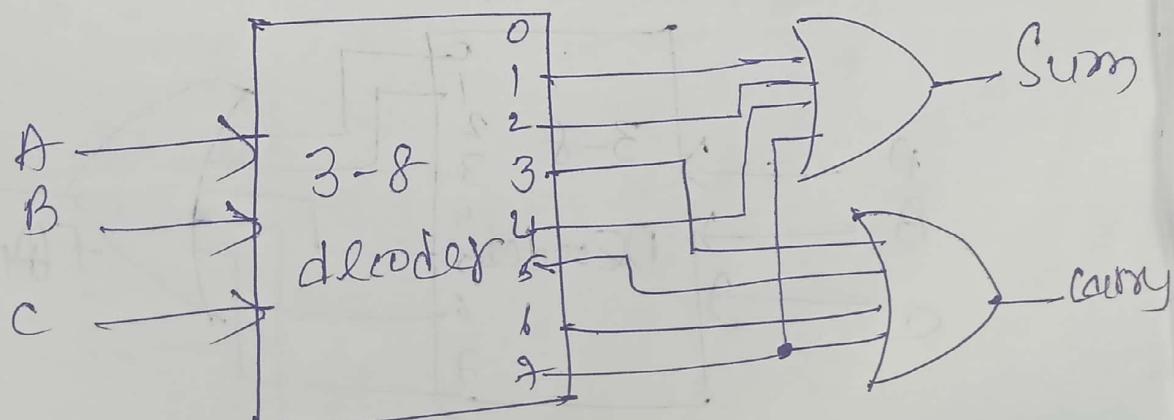
$$f_8 = xy\bar{z}$$

$$f_9 = xyz$$



3) Design a full adder using appropriate decoder & OR gate.

Ans: For a full adder, Sum =  $\sum m(1, 2, 4, 7)$   
Carry =  $\sum m(3, 5, 6, 7)$ .

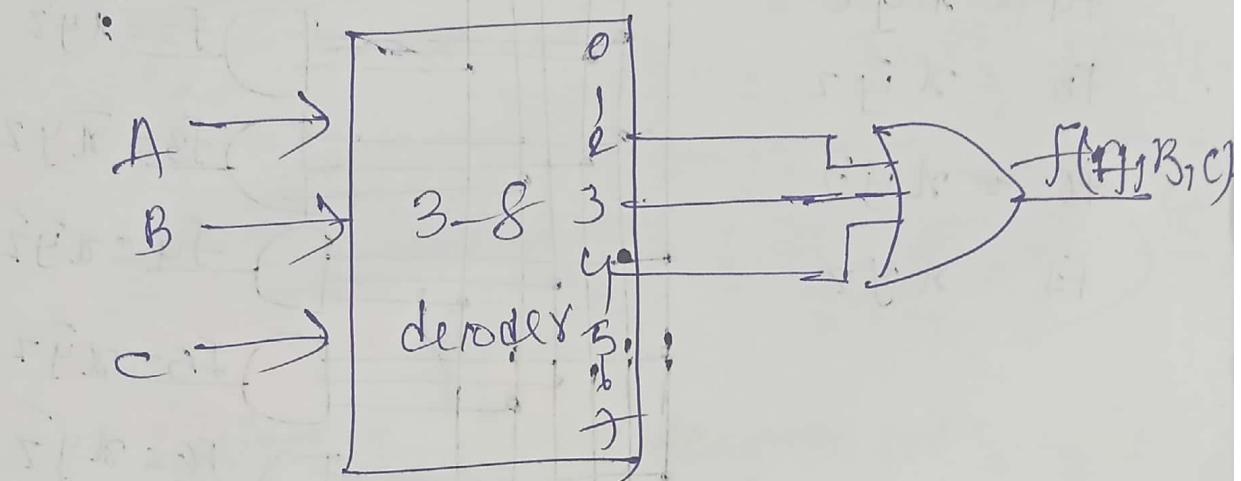


4) Establish the logic circuit using decoder and OR gate.  $f(A, B, C) = \overline{IM}(0, 1, 3, 7)$

Ans: Given,  $f(A, B, C) = \overline{IM}(0, 1, 3, 7)$

$f$  can also be written as,

$$f(A, B, C) = \overline{EM}(2, 3, 4)$$

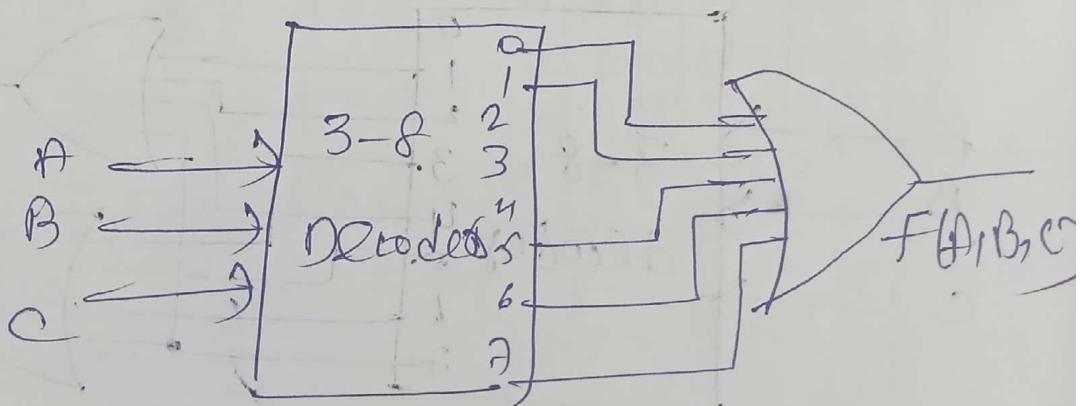


5) Establish the logic circuit using decoder and OR gate.  $f(A, B, C) = \overline{AB} \bar{C}$

$$\overline{AB} \bar{C} + \overline{A} \overline{B} \bar{C} + \overline{A} \overline{B} \bar{C} + A \overline{B} \bar{C} + A B \bar{C}$$

Ans: Given,  $f(A, B, C) = \overline{AB} \bar{C} + \overline{A} \overline{B} \bar{C} + \overline{A} \overline{B} \bar{C} + A \overline{B} \bar{C} + A B \bar{C}$

$$f(A, B, C) = \overline{EM}(0, 1, 5, 6, 7)$$

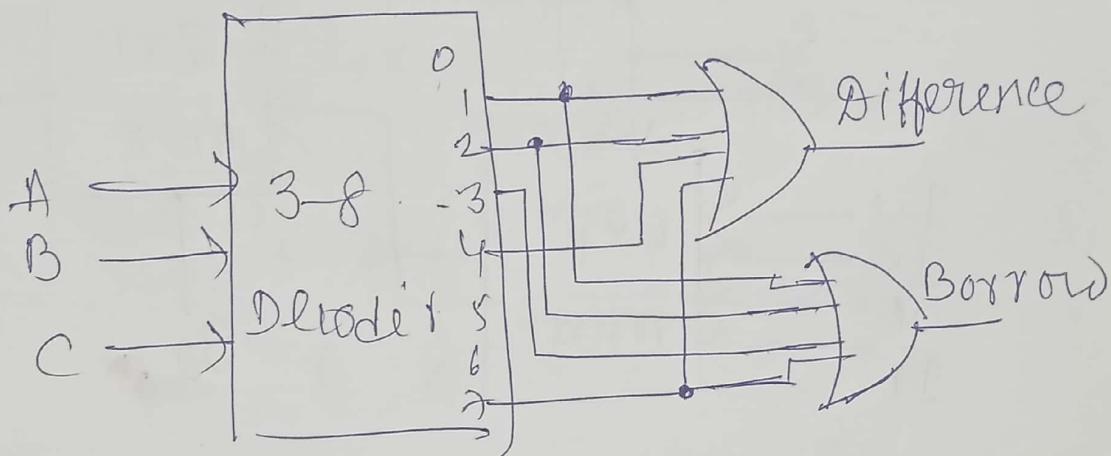


6) Establish full subtractor logic circuit using decoder & OR gates.

Ans: for a full subtractor,

$$\text{Difference} = \Sigma m(1, 2, 4, 7)$$

$$\text{Borrow} = \Sigma m(1, 2, 3, 7)$$



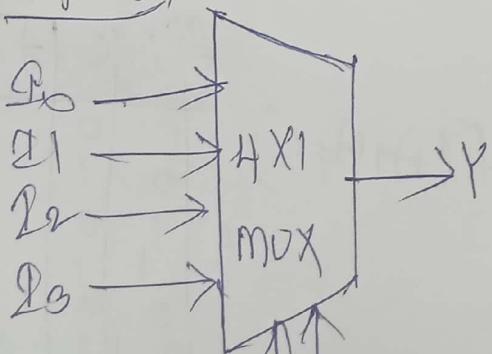
## Multiplexing & Demultiplexing

SAQ

1) Provide symbol and truth table for 4-to-1 multiplexer.

Ans: 4-to-1 multiplexers

Symbol

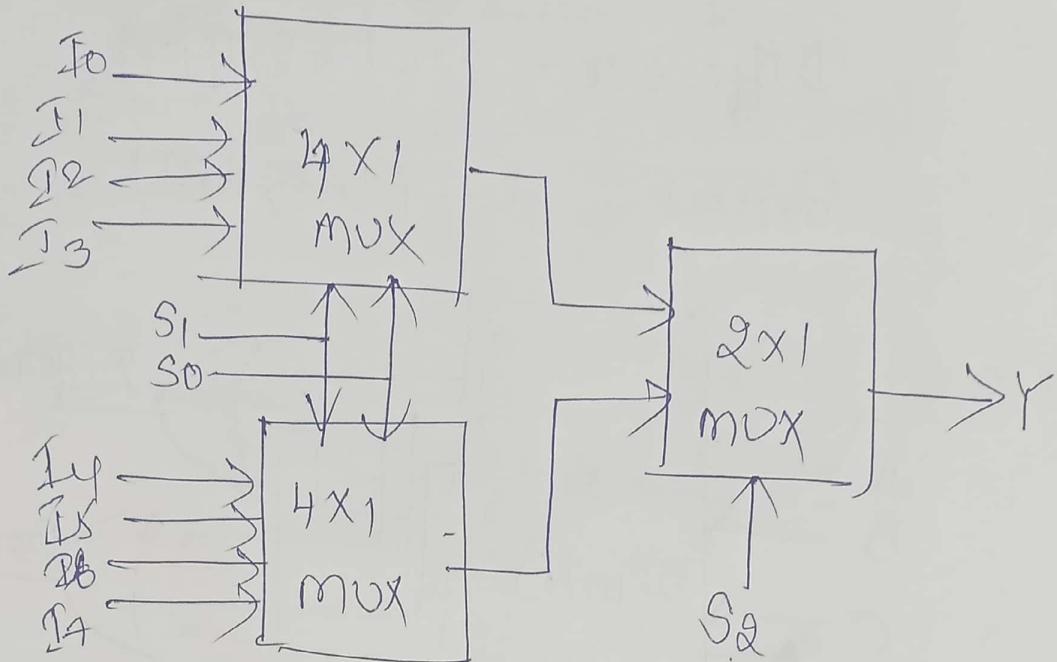


Truth-table

S <sub>1</sub>	S <sub>0</sub>	Y
0	0	D <sub>0</sub>
0	1	D <sub>1</sub>
1	0	D <sub>2</sub>
1	1	D <sub>3</sub>

2) Design 8:1 MUX using two 4:1 MUX  
and one 2:1 MUX.

Ans:



L&P

- 1) Produce the logic circuit using an appropriate multiplexer.  $f(A, B, C) = A'B'C + A'B'C' + ABC' + ABC$

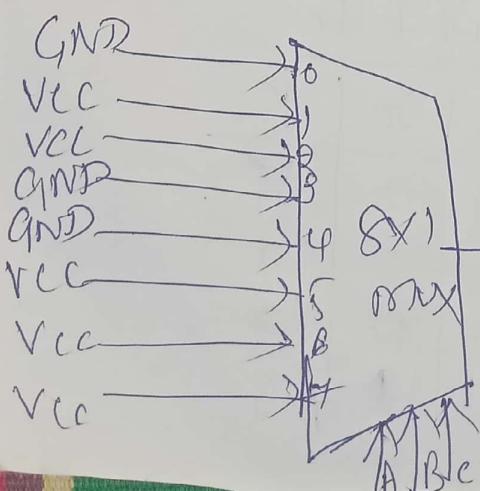
Ans:

$$+A'B'C' + A'B'C + ABC' + ABC$$

Given,  $f(A, B, C) = A'B'C + A'B'C' + ABC' + ABC$

001 010 101 110 111

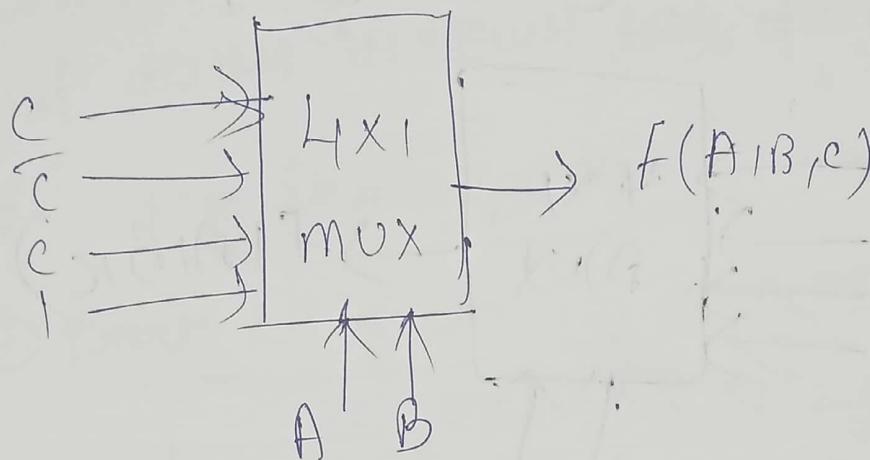
(1) (2) (5) (6) (7)



A	B	C	$f(A, B, C)$
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

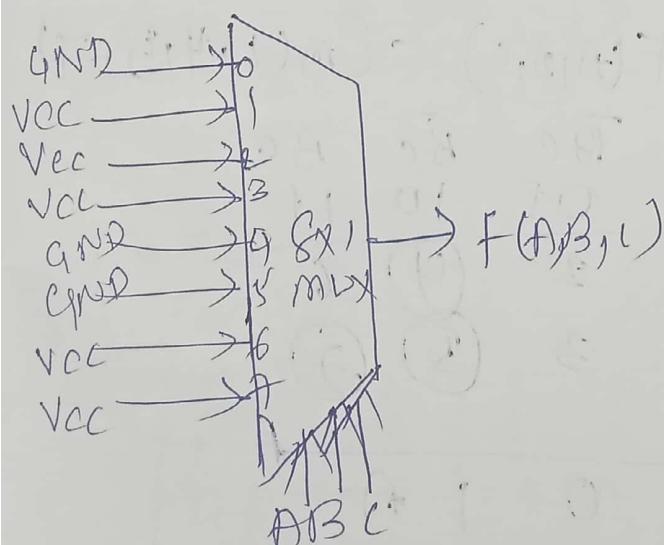
## Implementation Table

	$\bar{A}\bar{B}$	$\bar{A}B$	$A\bar{B}$	$AB$
	00	01	10	11
C = 0	0	2	4	6
C = 1	1	3	5	7
	C	$\bar{C}$	C	1



Q) Produce the logic circuit using appropriate  
multiplexer.  $f(A, B, C) = \sum m(1, 2, 3, 6, 7)$

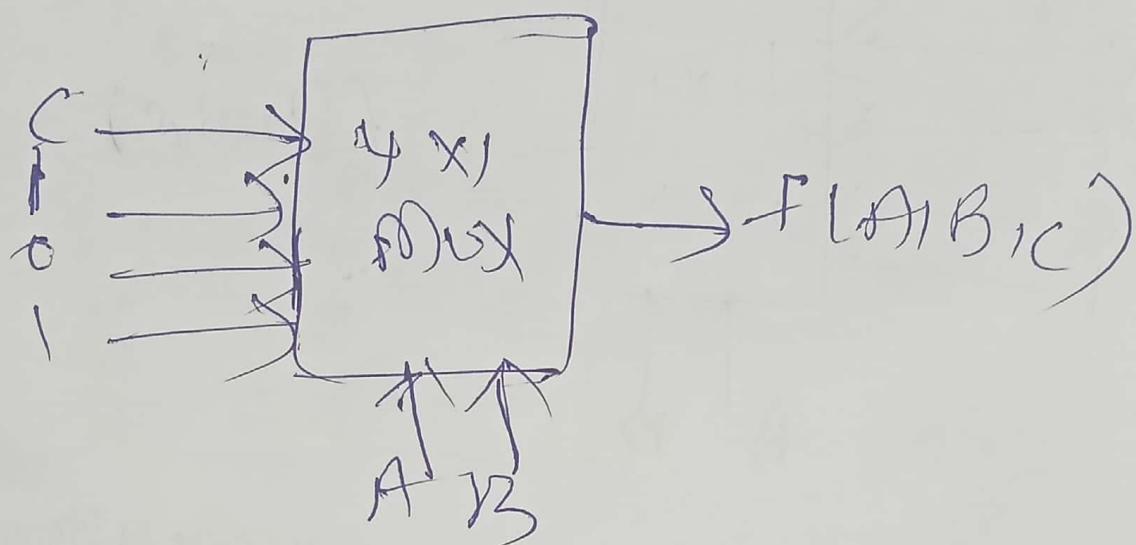
Ans: Given  $f(A, B, C) = \sum m(1, 2, 3, 6, 7)$



A	B	C	$f(A, B, C)$
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

## Implementation table

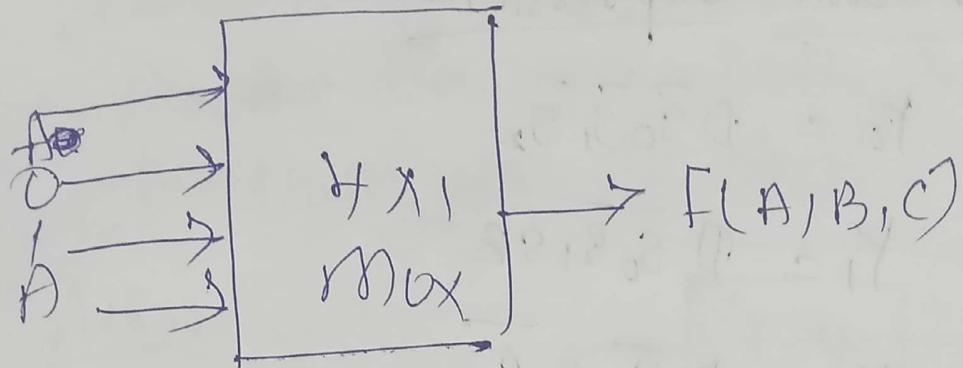
	$\bar{A}B$	$\bar{A}\bar{B}$	$A\bar{B}$	$AB$
$C=0$	0	2	y	6
$C=1$	1	3	5	7
	C	I	D	T



3) Design the function  $F(A, B, C) = \sum m(1, 4, 7)$  using 4x1 mux considering 'A' as output, B, C as selection levels.

Ans: Given,  $F(A, B, C) = \sum m(1, 4, 5, 7)$

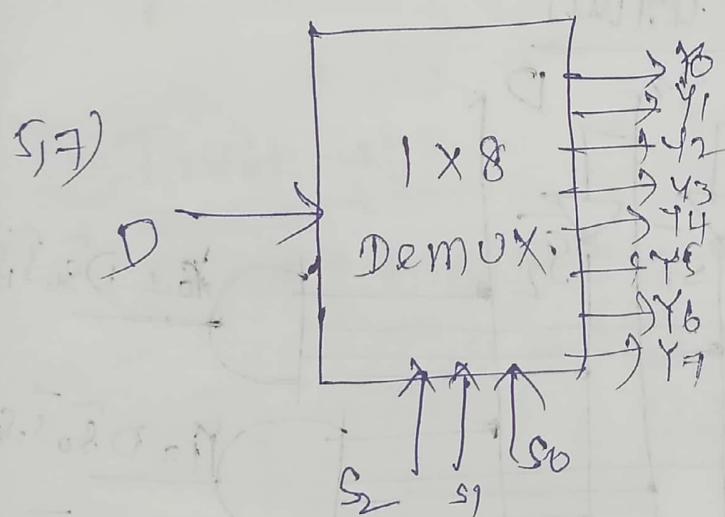
	$\bar{B}\bar{C}$	$\bar{B}C$	$B\bar{C}$	$BC$
$\bar{A}=0$	00	01	10	11
$\bar{A}=1$	0	2	4	6
	1	3	5	7



Q) Construct 1-to-8 De-multiplexer  
and discuss its truth table operation.

Ans : 1:8 Demultiplexer

① Block Diagram ② Truth-table



③ Truth table

D	S <sub>0</sub>	S <sub>1</sub>	S <sub>2</sub>	Y <sub>0</sub>	Y <sub>1</sub>	Y <sub>2</sub>	B	Y <sub>4</sub>	Y <sub>5</sub>	Y <sub>6</sub>	Y <sub>7</sub>
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	0

### ③ Boolean expression

$$Y_0 = D \bar{S}_0 \bar{S}_1 \bar{S}_2$$

$$Y_1 = D \bar{S}_0 \bar{S}_1 S_2$$

$$Y_2 = D \bar{S}_0 S_1 \bar{S}_2$$

$$Y_3 = D \bar{S}_0 \bar{S}_1 \bar{S}_2$$

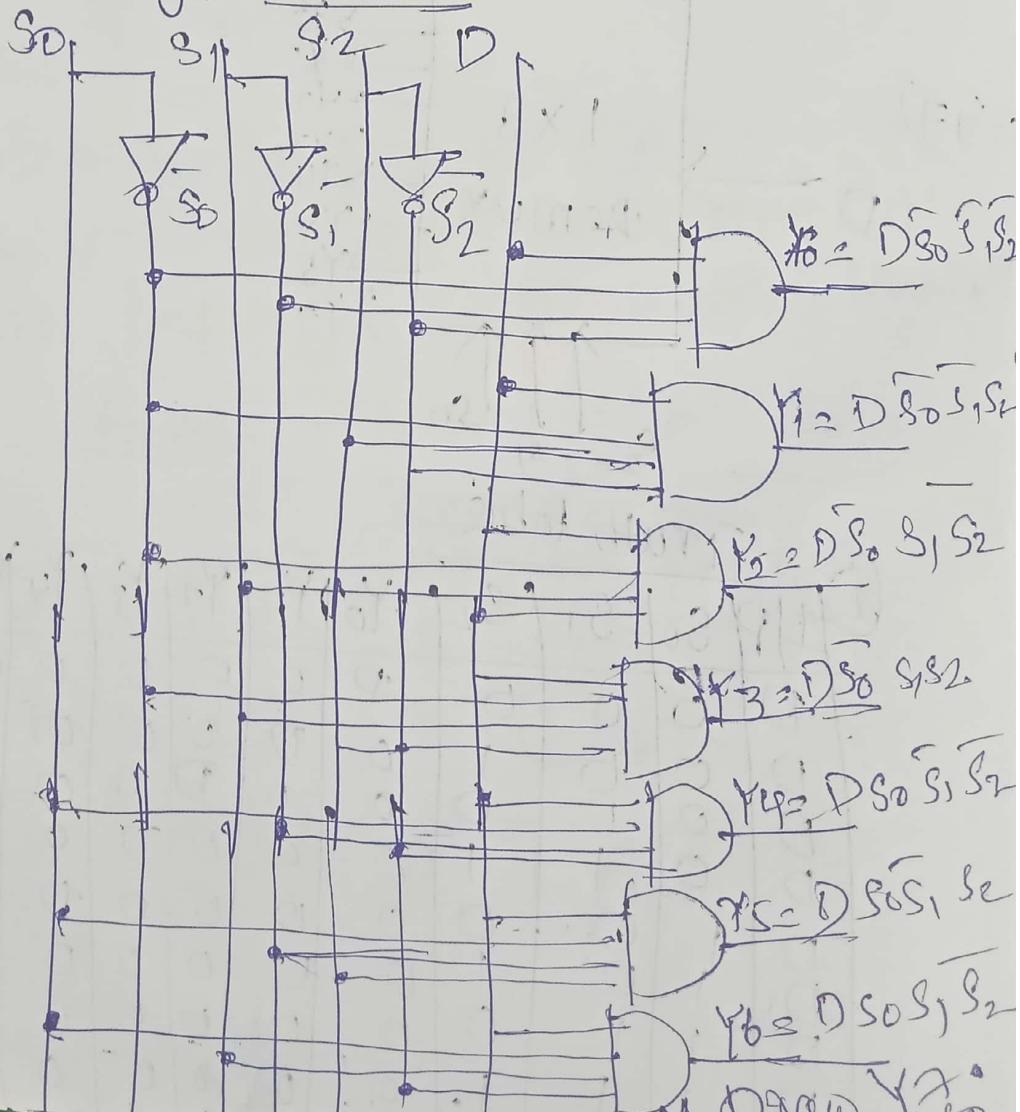
$$Y_4 = D \bar{S}_0 S_1 S_2$$

$$Y_5 = D S_0 \bar{S}_1 \bar{S}_2$$

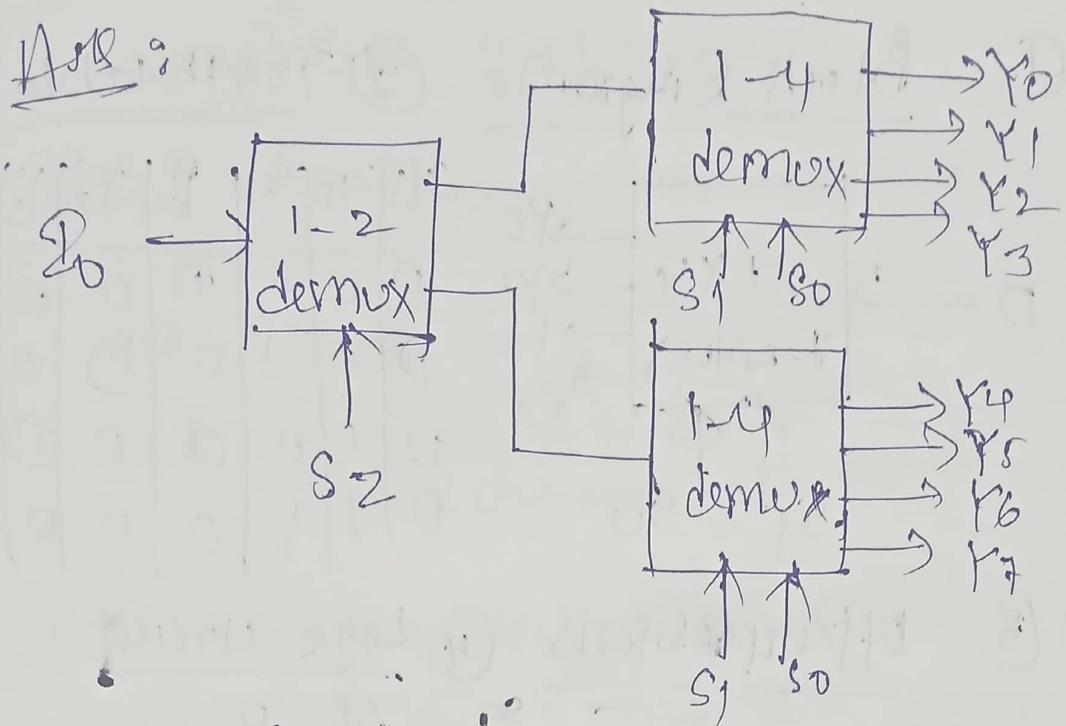
$$Y_6 = D S_0 S_1 \bar{S}_2$$

$$Y_7 = D S_0 S_1 S_2$$

### ④ Logic circuit



5) Construct 1-to-8 demultiplexer using  
1-to-4 demultiplexer blocks and discuss  
its truth table operation.



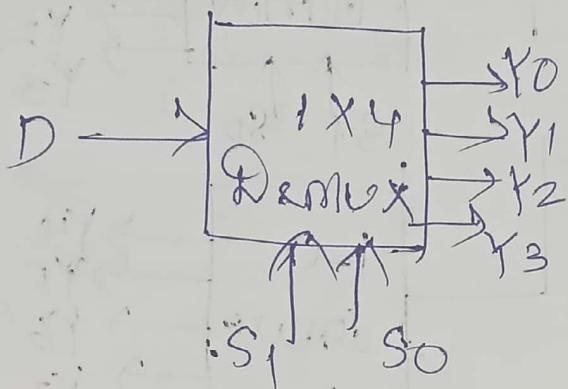
Truth table:

Input	S <sub>0</sub>	S <sub>1</sub>	S <sub>2</sub>	Y <sub>0</sub>	Y <sub>1</sub>	Y <sub>2</sub>	Y <sub>3</sub>	Y <sub>4</sub>	Y <sub>5</sub>	Y <sub>6</sub>	Y <sub>7</sub>
D	0	0	0	D	0	0	0	0	0	0	0
D	0	0	1	0	D	0	0	0	0	0	0
D	0	1	0	0	0	D	0	0	0	0	0
D	0	1	1	0	0	0	D	0	0	0	0
D	1	0	0	0	0	0	0	D	0	0	0
D	1	0	1	0	0	0	0	0	D	0	0
D	1	1	0	0	0	0	0	0	0	D	0
D	1	1	1	0	0	0	0	0	0	0	D

6) construct 1-to-4 Demultiplexer  
and draw its truth table operation

Ans 1-to-4 demultiplexer

① Block Diagram



② Truth table

S1	S0	D	Y0	Y1	Y2	Y3
0	0	0	0	0	0	0
0	1	0	0	1	0	0
1	0	0	1	0	0	0
1	1	0	1	1	0	0

③ DPF Expressions

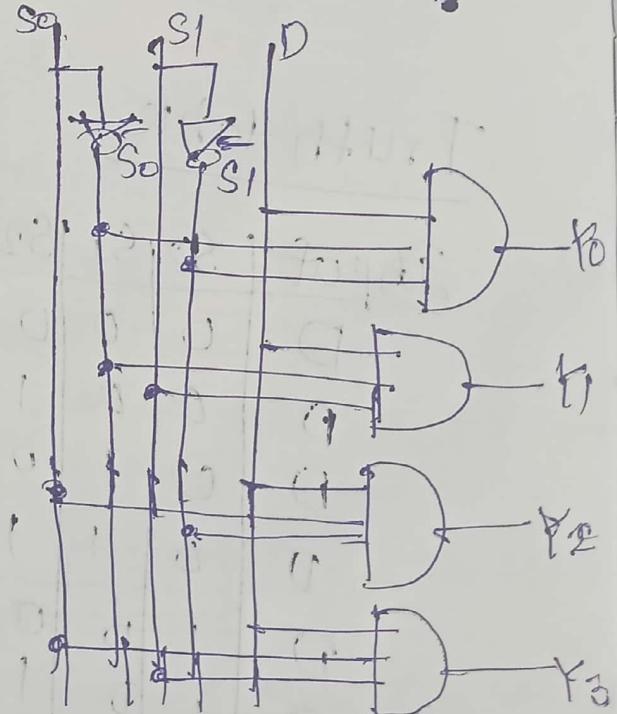
$$Y_0 = D \bar{S}_0 \bar{S}_1$$

$$Y_1 = D \bar{S}_0 S_1$$

$$Y_2 = D S_0 \bar{S}_1$$

$$Y_3 = D S_0 S_1$$

④ Logic circuit

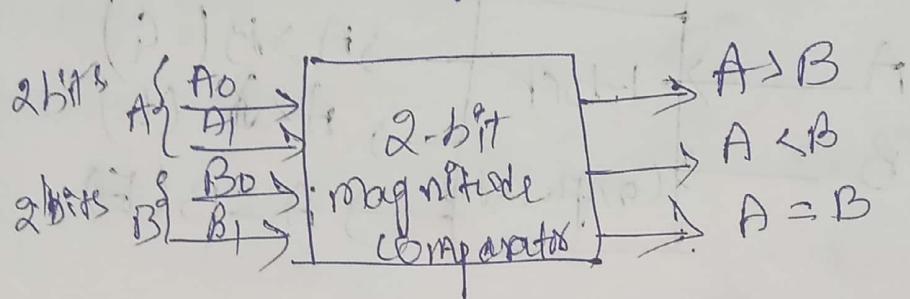


## Magnitude Comparator

Sol.

- i) Illustrate the operation of a 2-bit magnitude comparator.

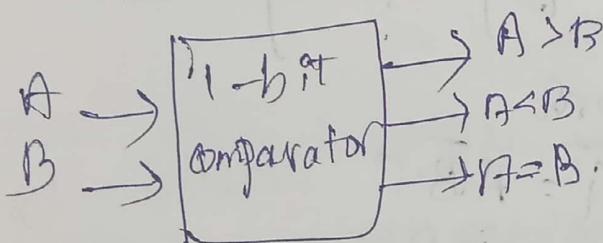
Ans: 2-bit magnitude comparator



- ii) Sketch the block diagram and logic circuit of single bit magnitude comparator.

Ans: Single bit magnitude comparator.

Block Diagram.



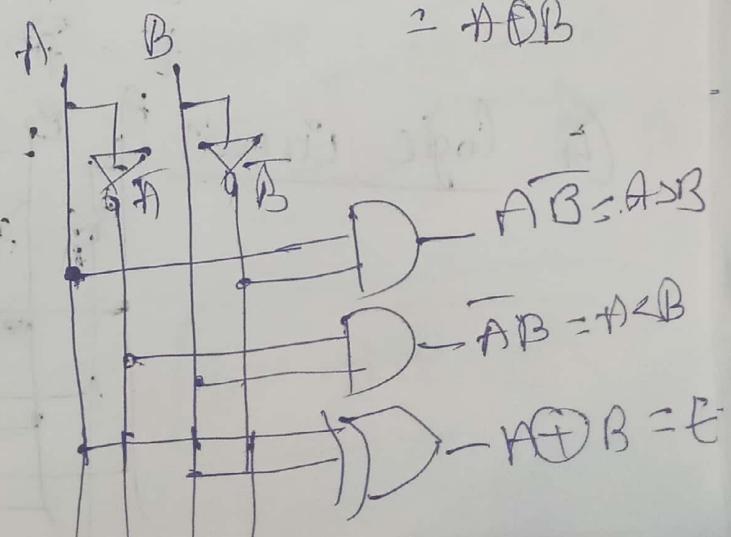
Logic circuit

$$A > B = A \bar{B}$$

$$A < B = \bar{A} B$$

$$(A = B) = \bar{A} B + A \bar{B}$$

$$= A \oplus B$$

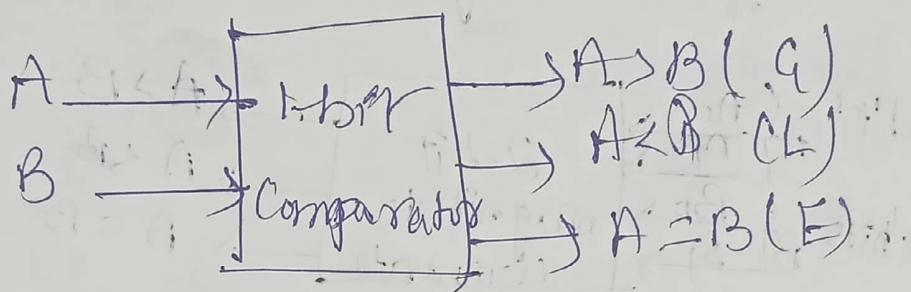


Q18

Q) Derive the logic equations for a 1-bit comparator with neat logic circuit.

Ans: 1-bit comparator

① Block Diagram



② Truth Table

A	B	$A > B$	$A \leq B$	$A = B$
0	0	0	1	1
0	1	0	1	0
1	0	1	0	0
1	1	0	0	1

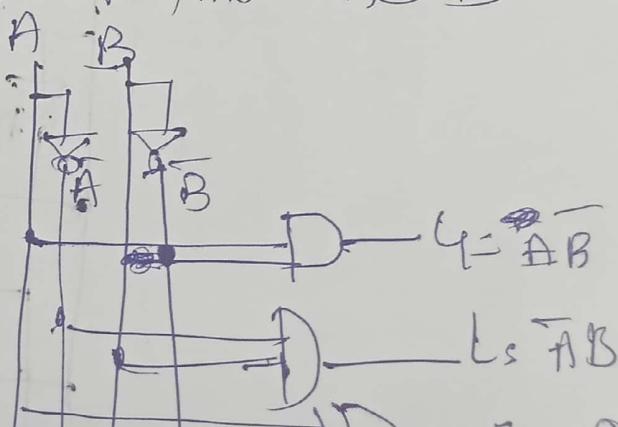
③ D.F. Expressions

$$G = A\bar{B}$$

$$L = \bar{A}B$$

$$E = \bar{A}\bar{B} + A\bar{B} = A \oplus B$$

④ Logic Circuit



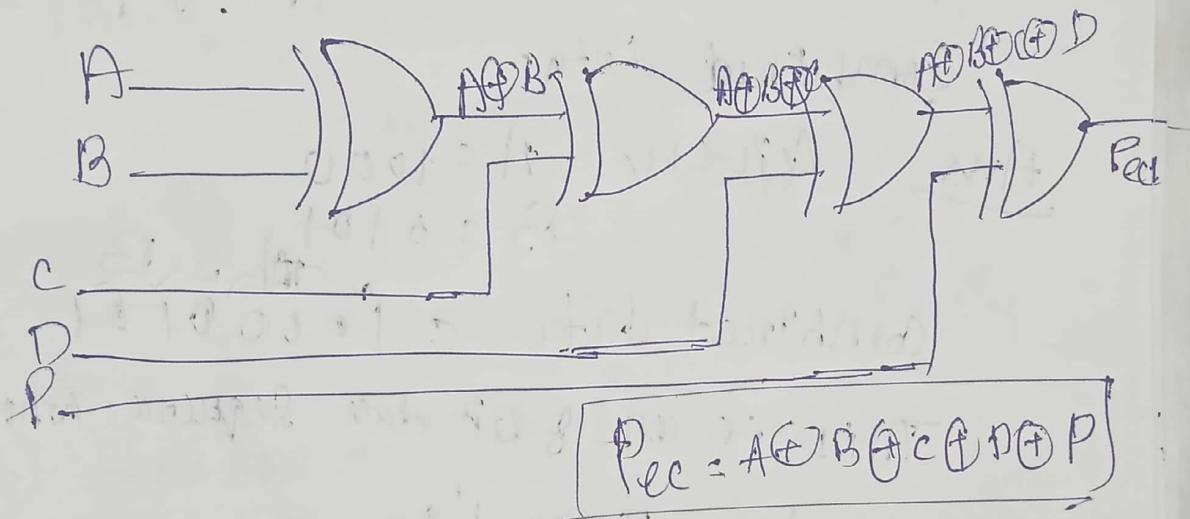
# Parity Generators & checkers

Ques

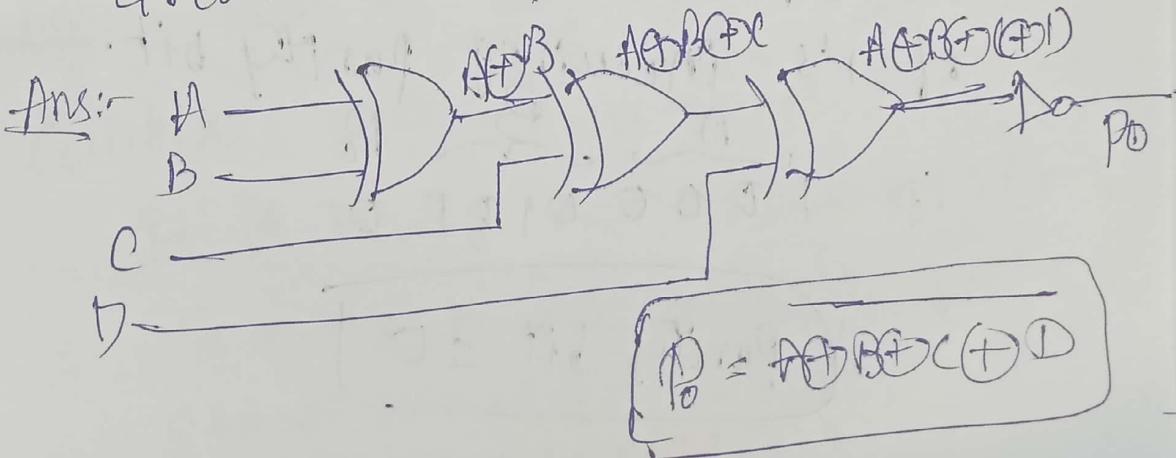
- i) Sketch 4-bit even parity checker circuit and explain its function.

Ans : Parity checker : A circuit that checks parity in the receiver is called Parity checker.

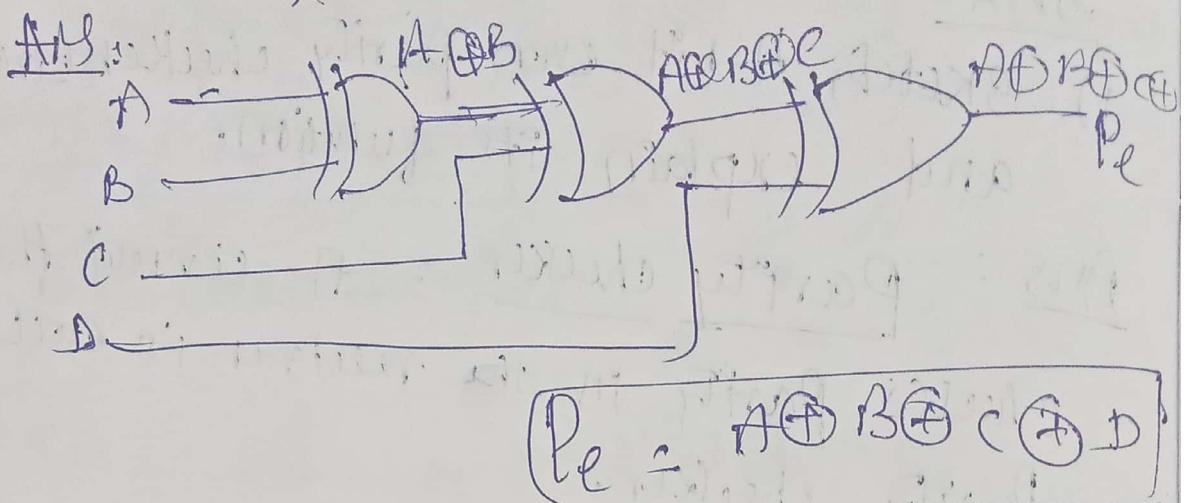
4-bit even parity checker circuit



- ii) Sketch 4-bit odd parity generator circuit and explain.



3) Sketch 4-bit even parity generator & explain.



4) Compute Parity bit for  $A = 1000$ ,  
 $B = 0101$  to obtain odd parity for  
 Combined data.

Ans: Given,  $A = 1000$   
 $B = 0101$

Combined data = ~~A + B~~  $10000101$ .

This is an 8-bit data sequence which has three 1's, we need to obtain odd parity, so, the sequence should have odd number of 1's including parity bit.

$\therefore \overbrace{10000101}^{\text{A } \text{B}} \text{ P}_o$

Parity bit = 0

5)  $A = 1010$ ;  $B = 1101$ . Add the parity bit and convert data into even.

Ans:  $A = 1010$ ;  $B = 1101$

Combined data =  $\underbrace{1010}_{A} \underbrace{1101}_{B}$

$10101101$

It is having odd number of 1's i.e 5

To make it even we need to add parity bit. The sequence is:

The sequence is,

$10101101\boxed{1}$  → even

Parity

6) Show how a parity bit is added to  $A = 0011$  and  $B = 0111$  to obtain even parity.

Ans: Given  $A = 0011$ ;  $B = 0111$

Combined data =  $\underbrace{0011}_{A} \underbrace{0111}_{B}$

It is having odd number of 1's i.e 5.

To make it even a parity bit '1'

should be added.

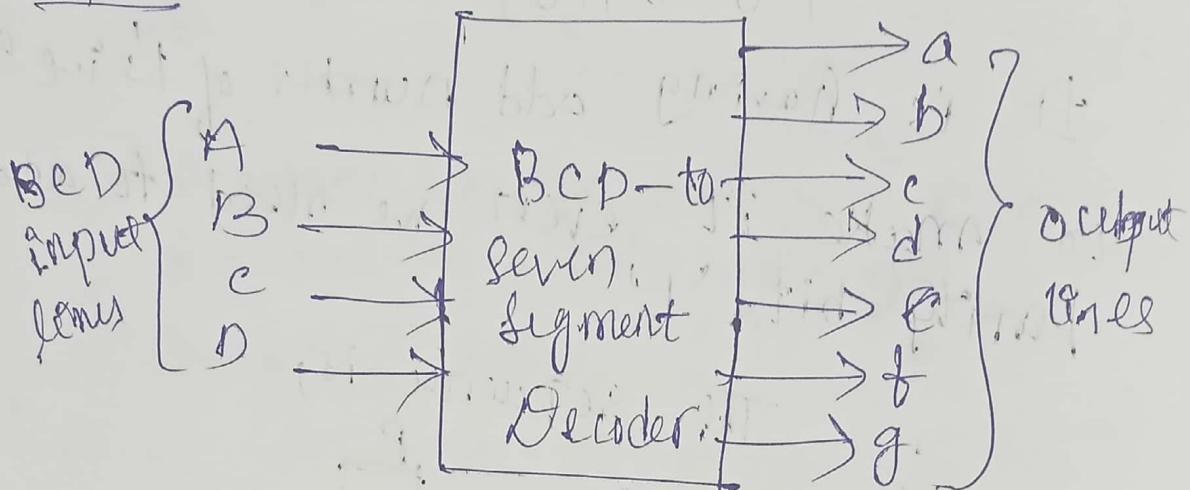
$00110111\boxed{1}$

## BED → 7 segment Decoder

SQP

- 1) Draw the connection diagram for BCD to seven segment Decoder.

Ans:



- 2) List the practical applications of BCD to Seven segment decoder.

Ans:

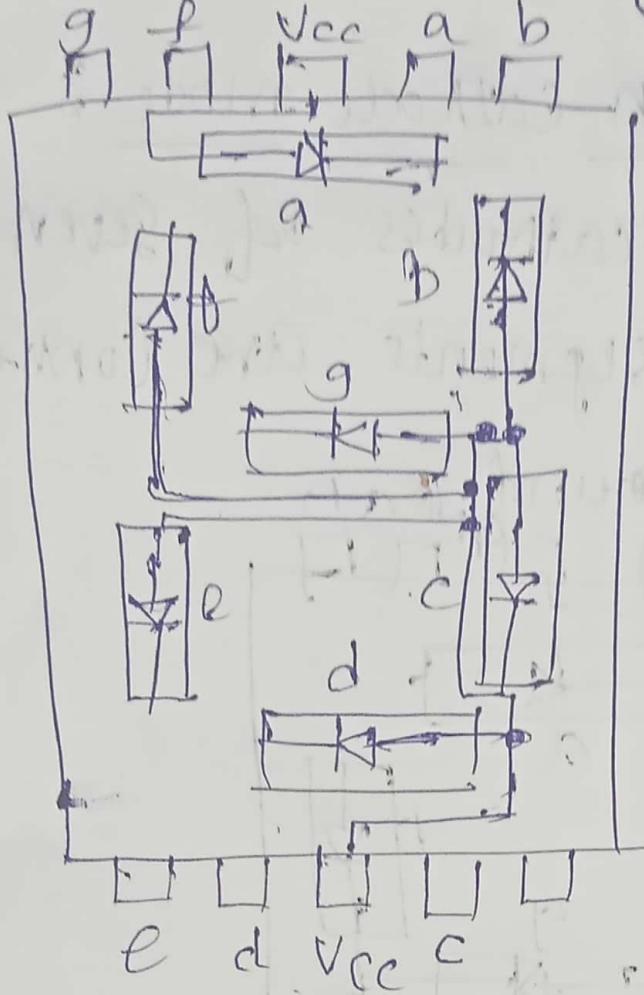
- Digital clocks, watches
- calculators
- Score Boards.

HQ

- 1) Illustrate BCD to Seven segment decoder common anode mode.

Ans: Common anode mode: In common anode mode, the five terminals of

anodes of Seven LEDs are connected to a common 've' voltage. (+ve).

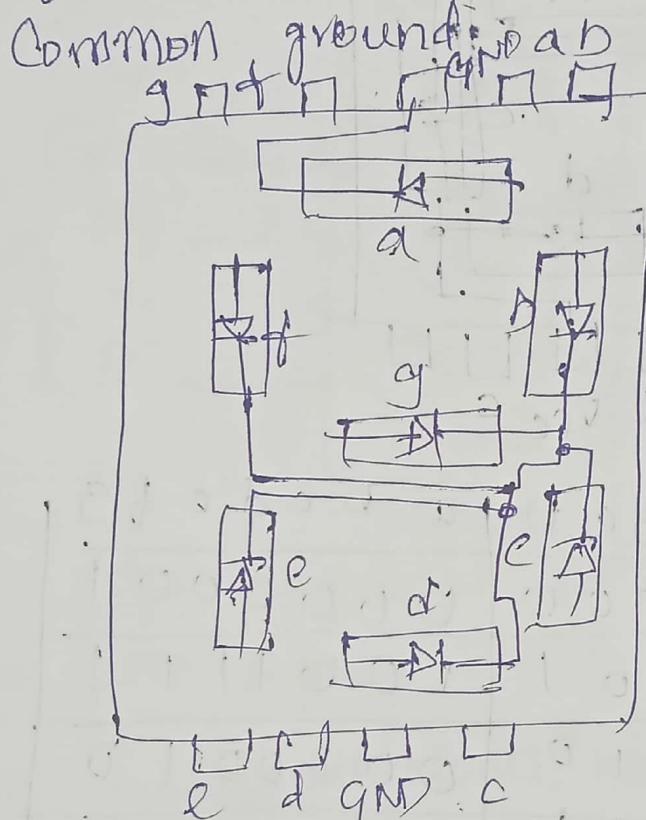


Digit	A B C D	a b c d e f g
0	0 0 0 0	0 0 0 0 0 0 1
1	0 0 0 1	1 0 0 1 1 1 1
2	0 0 1 0	0 0 1 0 0 1 0
3	0 0 1 1	0 0 0 1 1 1 0
4	0 1 0 0	1 0 0 1 1 0 0
5	0 1 0 1	0 1 0 0 1 0 0
6	0 1 1 0	0 1 0 0 0 0 0
7	0 1 1 1	0 0 0 1 1 1 1

Q2) Illustrate the BCD-to Seven Segment decoder. Common Cathode mode.

Ans: Common cathode mode

All the cathodes of seven LEDs of Seven segments are connected to common ground.



Digit	A B C D	a b c d e f g
0	0 0 0 0	1 1 1 1 1 1 0
1	0 0 0 1	0 1 1 0 0 0 0
2	0 0 1 0	1 1 0 1 1 0 1
3	0 0 1 1	1 1 1 1 0 0 1
4	0 1 0 0	0 1 1 0 0 1 1
5	0 1 0 1	1 0 1 1 0 1 1
6	0 1 1 0	1 0 1 1 1 1 1
7	0 1 1 1	1 1 1 0 0 0 0
8	1 0 0 0	1 1 1 1 1 1 1
9	1 0 0 1	1 1 1 1 0 1 1