Journal of Graphic Era University
Vol. 5, Issue 2, 58-68, 2017
ISSN: 0975-1416(Print), 2456-4281(Online)

Design of 16X16 SRAM Array Using 7T SRAM Cell for Low Power Applications

Rashmi Bisht*, Ashutosh Pranav

Department of Electronics and Communication Engineering
Graphic Era University, Dehradun, India
*Corresponding author: rshmbist@gmail.com

(Received July 12, 2016; Accepted September 1, 2016)

Abstract
Static Random Access Memory (SRAM) plays a vital role in various applications like cache memories, microprocessors and portable devices. As the technology's node scaling down, leakage power is the major problem in SRAM cell concerned for the low power applications. So, there is a requirement of low power adequate memory design. The main goal of this paper is to design a low power 16X16 SRAM array using 7T SRAM cell. The proposed architecture of 16X16 SRAM array is similar to 16X16 SRAM array using conventional 6T SRAM cell, only one additional NMOS transistor is placed between pull down transistors and ground node. This architecture reduces static power in standby mode. Cadence (version 6.1.5) simulation tool is used for designing. Comparative analysis is performed in terms of total power consumption. Peripheral components of complete 16X 16 SRAM array has been designed such as SRAM cell, write driver circuit, precharge circuit, row /column decoder and sense amplifier. For noise reduction during read operation, Differential type sense amplifier is used that has the ability of common mode noise voltage rejection. Power Consumption of 16X16 SRAM array using 7T SRAM cell is 20.04mW is measured that is 18.4% less compared to 16X16 SRAM array using 6T SRAM array. Transient analysis of write and read operations for both logic -0 and logic -1 is performed. For designing standard GPDK (generic process design kit) 180nm library is used.

Keywords- SRAM, WE, WL, SE.

1. Introduction

With the advancement in semiconductor technology, use of handheld devices and consumer electronics has been increased and they have need of high packaging density, low power consumption and high storage capacity. System on Chip (SOC) designs made feasible reduction in the cost. Static Random Access Memory (SRAM) is the main component of SOC design, used for storing large quantities of digital information. SRAM is a major component that is used for cache memory in microprocessors and memory in portable devices owing to its high speed and low power consumption. SRAM cell consists of latch circuit and data is stored as long as the power supply remains on. SRAM does not require refresh operation like dynamic RAM (DRAM).

Current trend of technology node's scaling is facing various challenges like leakage currents and increased power density (Shukla et al., 2011). As the device scaling, modern high performance microprocessors shows increase in leakage. These factors have also affected

Journal of Graphic Era University
Vol. 5, Issue 2, 58-68, 2017
ISSN: 0975-1416(Print), 2456-4281(Online)

SRAM cell stability. Thus power reduction along with long term device reliability needs low power SRAM design. Reduction in static power dissipation can be achieved using cross coupled CMOS inverters. Other merits of this design are low operating voltage and high noise immunity. Full CMOS SRAM cells were found to be more stable than resistive load SRAM cells at low supply voltage (Kiran and Saxena, 2015). The 7T SRAM cell is proposed for simultaneously reducing the leakage power. In idle mode, 7T SRAM cell cut off the ground path from supply voltage that prevents the cell from leakage through transistors. In active mode, this cell can operates similar to conventional 6T SRAM cell for read and write operation.

This paper has five sections along with the current introduction section. Section 2 covers architecture of SRAM array. Section 3 discusses design and simulation of SRAM along with brief introduction of simulation tool used, i.e., Cadence tool (version 6.1.5). Section 4 consists of all possible outcomes and their discussions. Finally, Section 5 summaries important conclusions of the research work carried out.

2. SRAM Architecture

Figure 1 shows the block diagram of SRAM array. It consists of SRAM cell, write driver circuit, precharge circuit, sense amplifier and row/ column decoder. A SRAM cell is capable of storing one bit of binary information (Bellerimath and Banakar, 2013). SRAM cells are arranged in an array of horizontal rows and vertical columns. In array architecture, there are 2^N rows that are called as word lines and 2^M columns that are called as bitlines. So, the total number of memory cells in the array is $2^{(N+M)}$. In this paper there are 2^4 rows and 2^4 columns.

For fast read and write operation separate write driver circuit and sense amplifier dedicated to each column (Shah et al., 2013). Due to differential writing and sensing technique, this architecture possesses fast read and write operation.

3. SRAM Cell

Cadence simulation tool (version 6.1.5) is used for SRAM designing. Standard gpdk180 library is used. The term ‘180’ defines minimum channel length (180 nm) that can be used for transistor design. In this paper, power supply of 1.8 V. Channel length of 200nm to avoid short channel effects is considered throughout the whole paper. Designing of 32bytes memory array is done using Schematic Editor Virtuoso.

3.1 6T SRAM Cell

Conventional SRAM cell consists of a CMOS latch (i.e., NM1, NM2, PM1 and PM2, two inverters connected back to back) and two complementary access transistors (NM3 and NM4). This cell can store one of its two possible states (0 or 1), as long as the power is supplied. When word line (WL) asserted high, access transistors are turned on for read and write operations (Shah et al., 2015). This connects the cell to two complementary bitlines columns (BL and BLB). Figure 2 shows the circuit diagram of 6T SRAM cell. Additional components give an

Journal of Graphic Era University
Vol. 5, Issue 2, 58-68, 2017
ISSN: 0975-1416(Print), 2456-4281(Online)

advantage to perform read and write operations simultaneously in one bit cell (Kang and Leblibici, 2003).

Thus, there is a need of some additional circuitry to perform this operation's simulation by using one circuit. Performance of the cell depends on Pull up Ratio (PR) and Cell Ratio (CR). PR is defined as a ratio of W/L of pull up transistor (PM1 or PM2) and W/L of access transistor (NM3 or NM4). It primarily controls the write ability of the cell. CR is defined as a ratio of W/L of pull down transistor (NM1 or NM2) and W/L of access transistor. It primarily controls the cell stability during a read operation.

When WL=0 cell is being inaccessible from both bitlines, keeping it in standby mode. This keeps prior stored value in the cell unchanged.

For read operation, WL=1 along with precharging of bitlines to supply voltage (V_{DD}). Bitlines will charge or discharge corresponding to the data stored in the cell. Voltage difference on bitlines is compared by the sense amplifier to determine the stored value. For write operation, data is fed to bitlines. Then WL =1 and with variation in bitlines, desired data will be written in the cell. In this research paper, cell ratio of 2 and pull up ratio of 0.66 is considered. The dimensional parameters of PMOS, NMOS and access transistors used in this paper are listed in Table 1.

As the scaling down of transistors is done, device leakage increases exponentially. In SRAM cell, leakage power is a main source of standby power consumption. Components of leakage power are subthreshold leakage, gate leakage and junction leakage. In conventional 6T SRAM cell, leakage power plays a significant role for low power applications. Reduction of leakage power is the main focus of this paper.

3.2 7T SRAM Cell: Proposed Design

For leakage reduction 7T SRAM Cell is presented. Figure 3 shows the circuit diagram of 7T SRAM Cell. As the name refers, there are seven transistors are used in this structure. It is similar to a 6T SRAM Cell and an additional NMOS transistor is placed between pull down transistors and ground node. Input of additional transistor NM5 is WL. Leakage currents mainly contribute subthreshold leakage and gate tunneling (Mishra et al., 2012).

Leakage power is depending on the storage of the cell. Subthreshold current flows when gate voltage of a transistor is below the threshold voltage of transistor. In standby mode, when WL is asserted low, both access transistors (NM3 and NM4) are off. Due to the stored value (logic 0) in SRAM cell, subthreshold leakage current flows through off transistors. The additional bottom transistor NM5 is likely to cut off the ground path. Thus reduces the leakage paths through the SRAM cell sources. In active mode, when WL asserted high, bottom transistor NM5 turns on. Thus read and write operations performed like 6T SRAM cell. Due to an additional transistor write access time is increased that is negligible. But there is an increase of

Journal of Graphic Era University
Vol. 5, Issue 2, 58-68, 2017
ISSN: 0975-1416(Print), 2456-4281(Online)

size and for large arrays the size of array will be larger. Dimensional parameters of 7T SRAM cell are similar to 6T SRAM cell and the channel width of NM5 is 6µm and channel length is 200nm is considered.

3.3 Precharge Circuit

The precharge circuit is the main component that is used in SRAM array. Figure 4 shows the circuit diagram of precharge circuit. Precharge circuit consists of three PMOS transistors. Two upper transistors are used for precharging and the lower one is used for equalization (Ho et al., 2006).

The main role of precharge circuit is to charge both the bitlines up to V_{DD} = 1.8V before a read and write operations. The width of PMOS transistors are 2µm and length 200nm is considered. Each column has a single precharge circuit in the array.

3.4 Write Driver Circuit

The main role of write driver circuit is to complete discharge one of the bitlines from the precharge level. Write driver is enabled by a Write Enable (WE) signal. Only one write driver circuit is required for each column in the array. Write driver circuit shows in Figure 5. It consists of two inverters (I1 and I2) and four NMOS (NM0, NM1, NM2 and NM3) transistors. Channel length of NMOS transistor is 5µm and channel width is 200nm is considered.

3.5 Sense Amplifier

Sense amplifier is an essential component of SRAM. Figure 6 shows the circuit diagram of Differential Type Sense Amplifier (DTSA). It is also known as voltage mode sense amplifier (Seevinck et al., 1987). In DTSA dynamic design mode is used that continuously checks the difference between bitlines and modify its output accordingly. The main goal of sense amplifier is to perform reliably during a read operation and should be noise resistant within the system. There are various types of sense amplifiers found in the literature (Mohammad et al., 2012). Among all sense amplifiers, DTSA performs properly and it also resists noise from the system. It consists of a biasing current source (NM2) and differential pair (NM0 and NM1) with an active current mirror load (PM0 and PM1). Bitlines are connected to the differential pair as a input and output is taken from the drain of NM0 or PM0. Sense amplifier is enabled by a Sense Enable (SE) signal during a read operation.

Differential amplifier is resistant to noise due to its ability to reject common mode voltages and differences between the inputs are amplified. Channel length for all transistors in DTSA is 1µm is considered. To keep NM3 in saturation region, a bias voltage of 0.6V is required during a read operation. The dimensional parameters of transistors used in DTSA are listed in Table 2.

Journal of Graphic Era University
Vol. 5, Issue 2, 58-68, 2017
ISSN: 0975-1416(Print), 2456-4281(Online)

3.6 Row/Column Decoder

In memory design address decoder is used to decode the given address and enable the particular row or column. Row and column decoder is used to select a particular WL and WE of a SRAM array, respectively.

Figure 7 shows the block diagram of decoder that have four inputs (a, b, c, and d) and 16 outputs (X0 - X15). In this paper AND gate based decoder is used. Table 3 shows the outputs of 4:16 decoder that select specific WL and WE for corresponding row and column of SRAM array.

3.7 SRAM Array using 7T SRAM Cell

In this paper 16X16 SRAM array using 7T has been designed that store 32 bytes. This array consists of 16 write driver circuits, 16 precharge circuits and 16 sense amplifiers. Row and column decoder is used to select a particular WL and WE signal of write driver circuit, respectively. Figure 8 shows the schematic of 16X16 SRAM array using 7T SRAM cell.

4. Results and Discussion

This section describes about the simulation results of 16X16 SRAM array using 7T SRAM cell. This work is carried out on Cadence simulation tool. Comparison of 16X16 SRAM array using 6T and 7T SRAM cell in terms of total power consumption is shown in Table 4. In this paper leakage parameters are minimized by using 7T SRAM cell.

Power Comparison of different 16X16 SRAM array are shown in Figure 9 and improvements shown in the proposed design. There are three designs: proposed, conventional and reference number 3 have been compared.

Transient response of 16X16 SRAM array for write-1 and read-1 operations is shown in Figure 10. For write-1 operation, bit lines are precharged to V_{DD} for a short duration. Based on input address of row decoder and column decoder corresponding WL9 and WE9 is selected for read and write operations. The corresponding outputs are q9 and vo9 for write and read operations, respectively, that are shown in below figure. Write -1 operation is performed, when WE signal goes high and data input signal of write driver goes high. Thus q9 output of SRAM cell goes high and therefore logic -1 is written in the memory. For read operation, SE9 signal goes high and whatever the data is stored in the cell is shown at the output of sense amplifier. Thus vo9 output of sense amplifier goes high. Therefore, logic -1 is read into the memory.

Transient response of 16X16 SRAM array for write-0 and read-0 operations is shown in Figure 11. For write-0 operation, bit lines are precharged to V_{DD} for a short duration Based on input address of row decoder and column decoder corresponding WL9 and WE9 is selected for read and write operations. The corresponding outputs are q9 and vo9 for write and read operations, respectively, that are shown in Figure 11. Write -0 operation is performed, when WE signal goes high and data input signal of write driver goes low. Thus q9 output of SRAM cell goes

Journal of Graphic Era University
Vol. 5, Issue 2, 58-68, 2017
ISSN: 0975-1416(Print), 2456-4281(Online)

low and therefore logic -0 is written in the memory. For read operation, SE9 signal goes high and whatever the data is stored in the cell is shown at the output of sense amplifier. Thus vo9 output of sense amplifier goes low. Therefore, logic -0 is read into the memory.

5. Conclusion

Low power 16x16 SRAM array is designed that store 256 bits. Complete array that includes peripheral components like SRAM cell, write driver circuit, precharge circuit, address decoder and sense amplifier are designed. In this paper 16X16 SRAM array is designed using 6T and 7T SRAM cell and compared in terms of total power consumption. Power consumption of 24.58mW has been analyzed in 16X16 SRAM array using conventional 6T SRAM cell. The proposed 16X16 SRAM array using 7T SRAM cell consumes 20.04mW that is less than conventional 6T SRAM array. Supply voltage of 1.8V is considered for complete SRAM array designing. Transient responses have been analyzed for both read and write operations. Low power SRAM array is designed using Cadence tool (version 6.1.5) and gpdk (generic process design kit) 180nm library is used for designing.

Parameters	**Devices**		
	PM1, PM2	**NM1, NM2**	**NM3, NM4**
Channel Length (L) (in nm)	200	200	200
Channel Width (W) (in µm)	2	6	3

Table 1. Dimensional parameters of SRAM cell design

Parameters	**Differential Pair**		**Active Current Mirror Load**		**Biasing Current Source**
	NM1	**NM2**	**PM1**	**PM2**	**NM3**
Channel Width (W) (in µm)	7	7	84	84	9

Table 2. Dimensional parameters of sense amplifier design

Journal of Graphic Era University
Vol. 5, Issue 2, 58-68, 2017
ISSN: 0975-1416(Print), 2456-4281(Online)

Inputs				Output Selection (As WL/WE Selection)
d	*c*	*b*	*a*	
0	0	0	0	x0
0	0	0	1	x1
0	0	1	0	x2
0	0	1	1	x3
0	1	0	0	x4
0	1	0	1	x5
0	1	1	0	x6
0	1	1	1	x7
1	0	0	0	x8
1	0	0	1	x9
1	0	1	0	x10
1	0	1	1	x11
1	1	0	0	x12
1	1	0	1	x13
1	1	1	0	x14
1	1	1	1	x15

Table 3. Decoder four-to-sixteen and output selection

Parameters	Proposed 7T SRAM	Conventional 6T SRAM	Ref.3
Total power consumption (in mW)	20.04	24.48	49.94

Table 4. Comparison of 16X16 SRAM array in terms of total power consumption

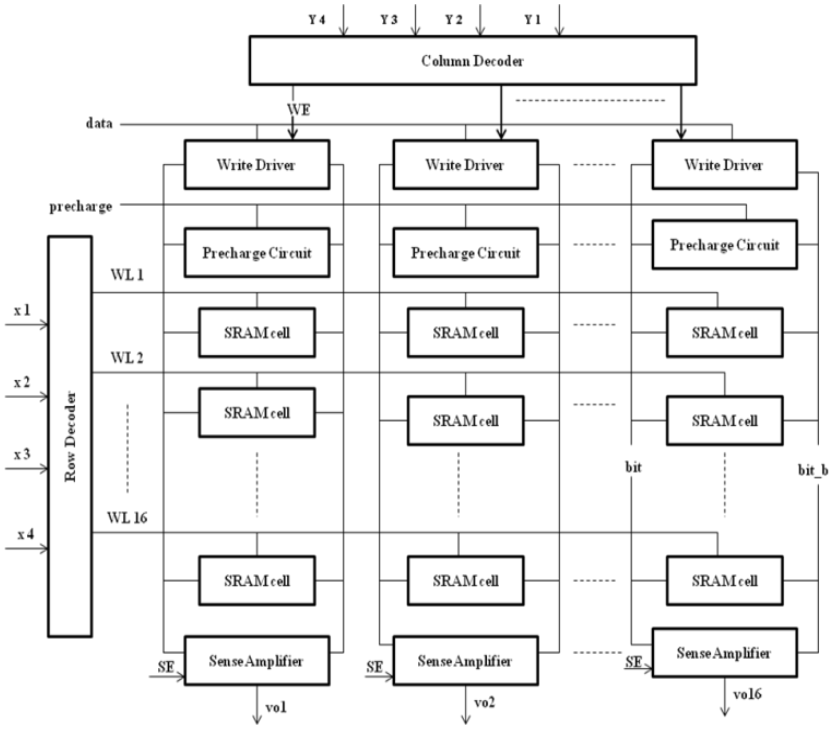

Figure 1. Block diagram of SRAM architecture

Journal of Graphic Era University
Vol. 5, Issue 2, 58-68, 2017
ISSN: 0975-1416(Print), 2456-4281(Online)

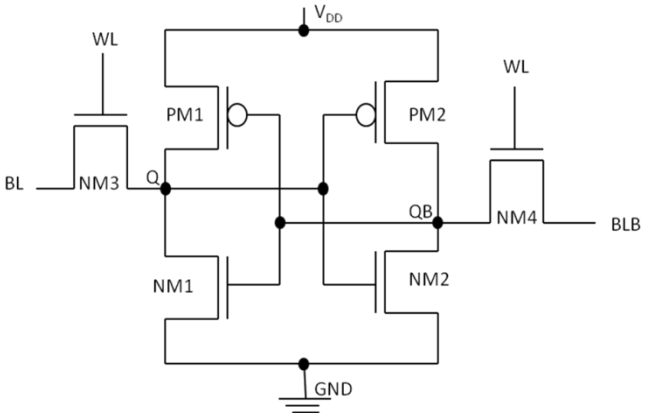

Figure 2. Circuit diagram of 6T SRAM Cell

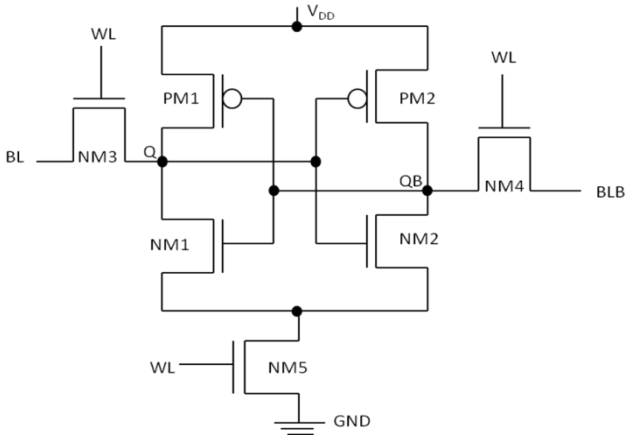

Figure 3. Circuit diagram of 7T SRAM Cell

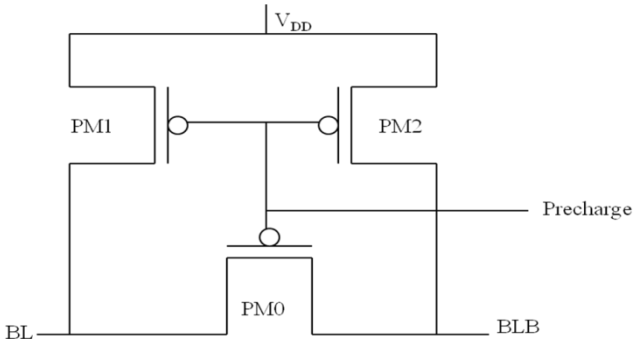

Figure 4. Circuit diagram of precharge circuit

Journal of Graphic Era University
Vol. 5, Issue 2, 58-68, 2017
ISSN: 0975-1416(Print), 2456-4281(Online)

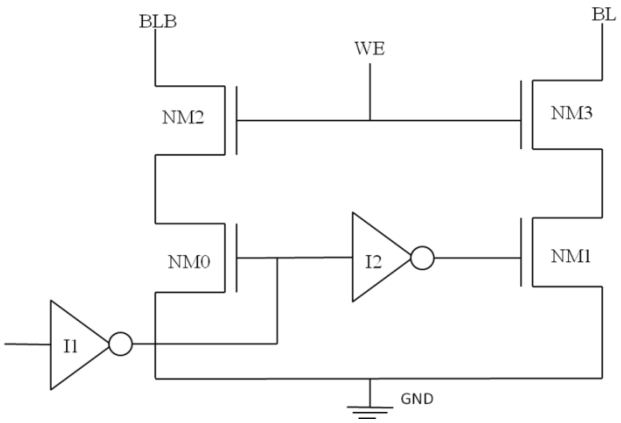

Figure 5. Circuit diagram of write driver circuit

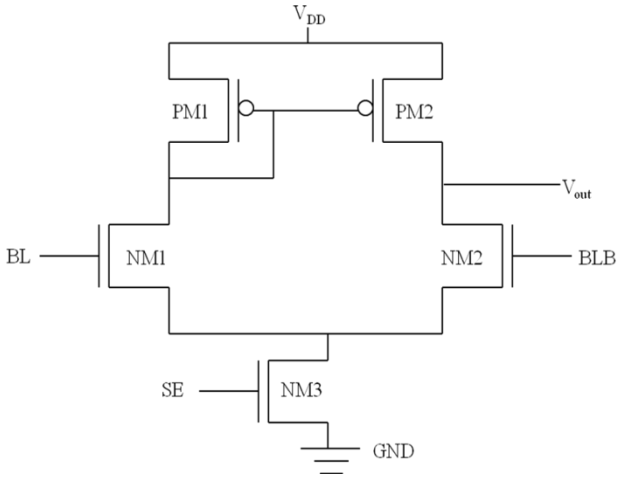

Figure 6. Circuit diagram of sense amplifier

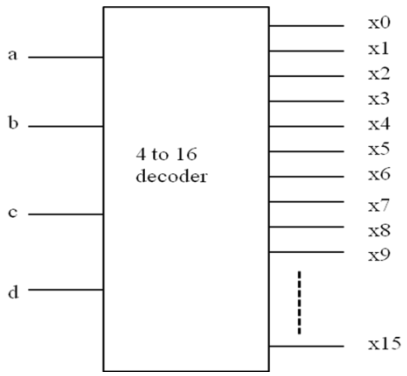

Figure 7. Block diagram of 4:16 decoder

Journal of Graphic Era University
Vol. 5, Issue 2, 58-68, 2017
ISSN: 0975-1416(Print), 2456-4281(Online)

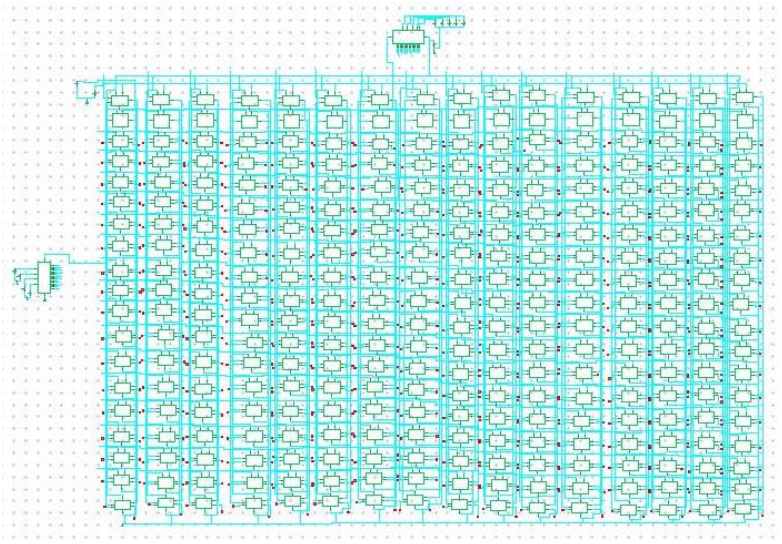

Figure 8. Schematic of 16X16 SRAM array using 7T SRAM array

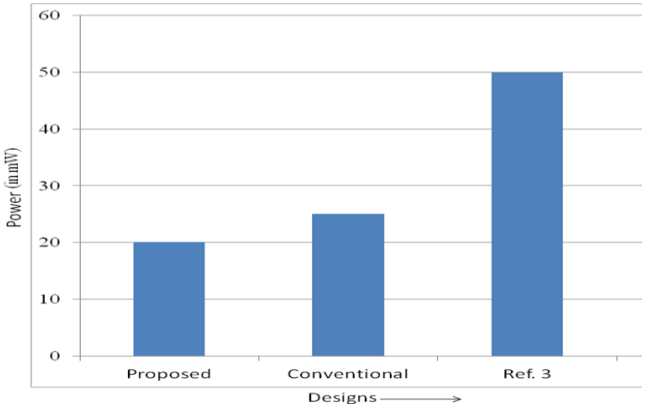

Figure 9. Bar chart for power comparison of 16X16 SRAM array

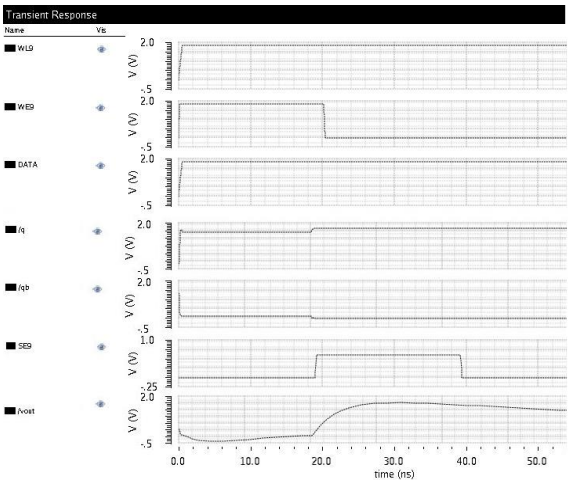

Figure 10. Transient response of 16X16 SRAM array using 7T SRAM cell (for write-1 and read-1 logic)

Journal of Graphic Era University
Vol. 5, Issue 2, 58-68, 2017
ISSN: 0975-1416(Print), 2456-4281(Online)

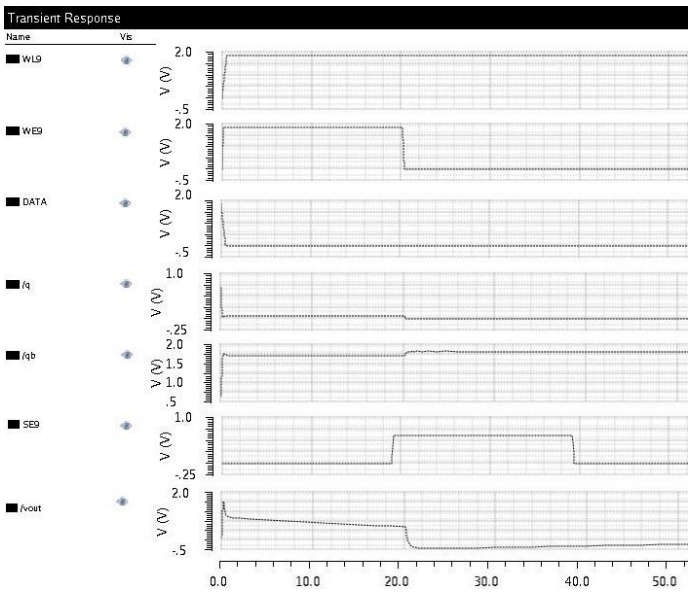

Figure 11. Transient response of 16X16 SRAM array using 7T SRAM cell (for write-0 and read-0 logic)

References

Bellerimath, P. S., & Banakar, R. M. (2013). Implementation of 16X16 SRAM memory array using 180nm technology. International Journal of Current Engineering and Technology, Special Issue, 288-292.

Ho, D., Iniewski, K., Kasnavi, S., Ivanovi, A., & Natarajan, S. (2006). Ultra low power 90nm SRAM cell for wireless sensor network applications. IEEE Symposium on Circuits and Systems, 4131-4134.

Kang, S. M., & Leblibici, Y. (2003). CMOS (Third edition). Tata McGraw Hill.

Kiran, P. V., & Saxena, N. (2015, February). Design and analysis of different types SRAM cell topologies. In Electronics and Communication Systems (ICECS), 2015 2nd International Conference on (pp. 1060-1065). IEEE.

Mishra, M., Majumdar, S., Malviya, D., & Bansod, P. P. (2012). Design of SRAM cell in 0.18µm technology. International Conference on Information Communication and Embedded Systems, 457-463.

Mohammad, B., Dadabhoy, P., Lin, K., & Bassett, P. (2012, December). Comparative study of current mode and voltage mode sense amplifier used for 28nm SRAM. In 2012 24th International Conference on Microelectronics (ICM) (pp. 1-6). IEEE.

Seevinck, E., List, F. J., & Lohstroh, J. (1987). Static-noise margin analysis of MOS SRAM cells. IEEE Journal of Solid-State Circuits, 22(5), 748-754.

Shah, K. C., Gandhi, D. N., & Nagpara, B. H. (2013). Design and analysis of 256 bit SRAM in deep submicron CMOS technologies. Journal of Information, Knowledge and Research in Electronics and Communication Engineering, 2(2), 812-817.

Shah, R. K., Hussain, I., & Kumar, M. (2015). Performance comparison for different configurations of SRAM cells. International Journal of Innovative Research in Science, Engineering and Technology, 4(1), 18543-18545.

Shukla, N. K., Singh, R. K., & Pattanaik, M. (2011). Design and analysis of a novel low power SRAM bit- cell structure at deep sub micron CMOS technology for mobile multimedia applications. International Journal of Advanced Computer Science and Applications, 2(5), 43-49.