# 16x16 Low Power SRAM Array

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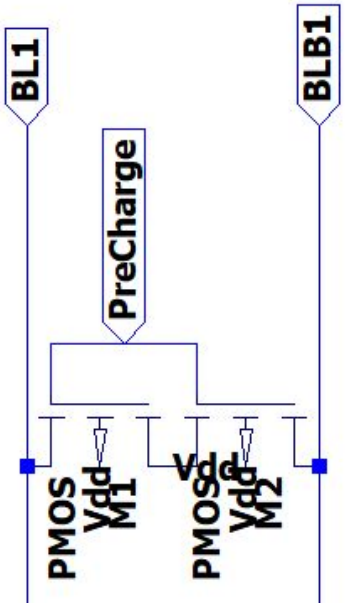
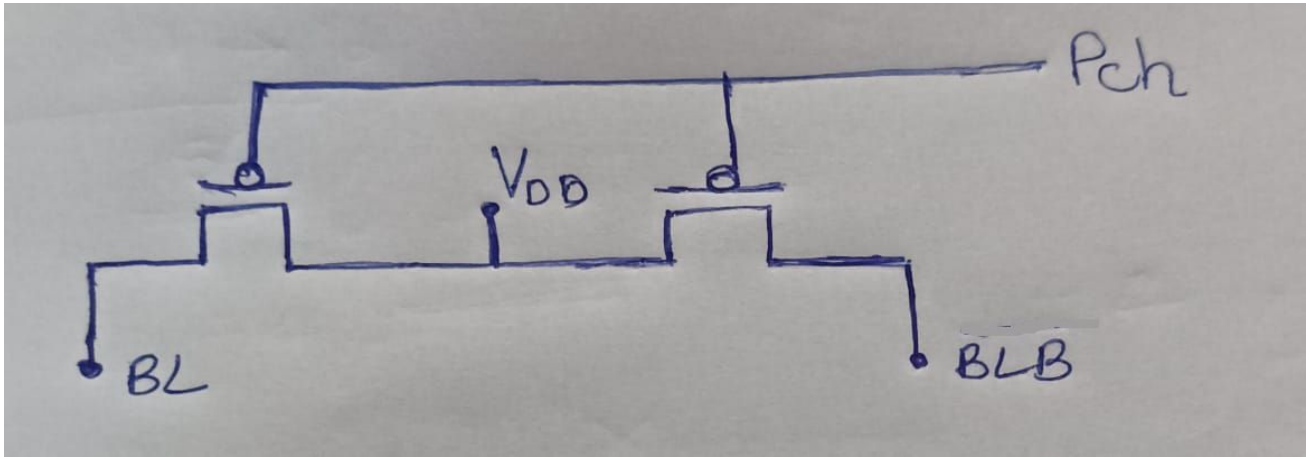
# To achieve Low power consumption

- Decoder→ Nand based decoder
- Sense Amplifier→ Latch based (2 cross coupled inverter)
- Maximum possible minimum sized transistors

# Periphery circuitry- Precharge circuit

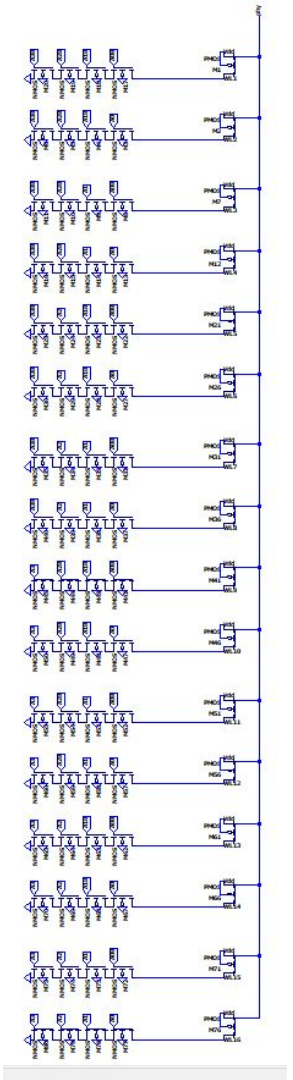
- The bit line and bit line bar are pre-charged to known value (Vdd).
- To prevent bit flip due to noise.
- Based on the cell voltage either BL or BLB will have delta difference amplified by the sense amplifier during read operation.



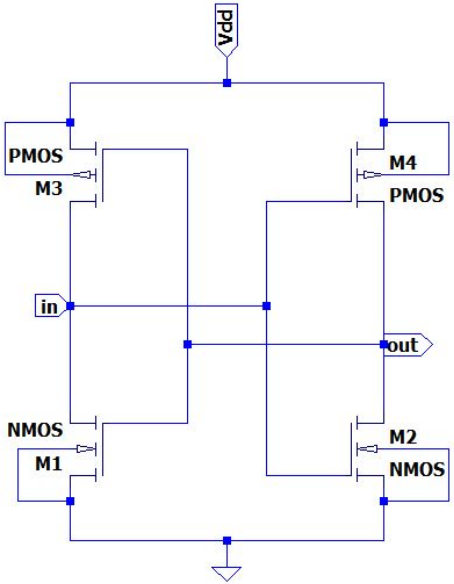



# Periphery circuitry- Decoder

- Nand based decoder to achieve low power.
- Low power→ less leakage power.
- In one decoder→8 inputs (A0-A3 and Ab0-Ab3) and 16 outputs
- A0-A3 → Column decoder (BL andBLB)
- A4-A7 → Row decoder (WL)

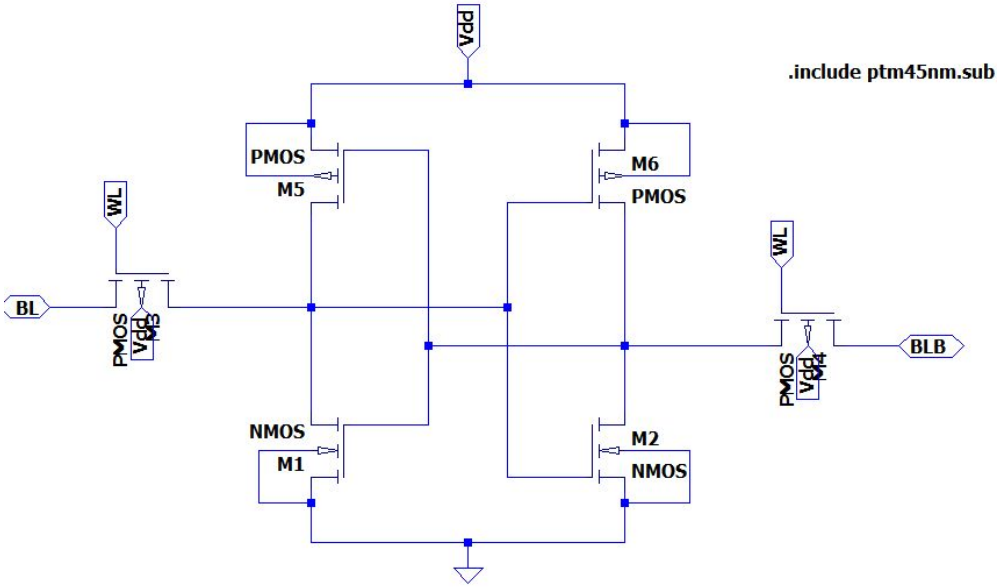


# Periphery circuitry- Sense Amplifier




- Double ended sensing -latch based sense amplifier.
- Positive feedback- faster.
- Low power as inverters are only used.
- Inverter based (large signal) can be used as only 16x16- less capacitance but requires 2 inverters to have true and complement values.
- Hence we choose latch based sense amplifier.

# 6T SRAM cell




- Important consideration→ Cell Ratio and Beta Ratio as same port used for both read and write operation.

  $K_{PDN} > K_{access} > K_{PUN}$

- Length -minimum
- 45 nm for the 45 nm PTM model
- $V_{DD}$=1 V

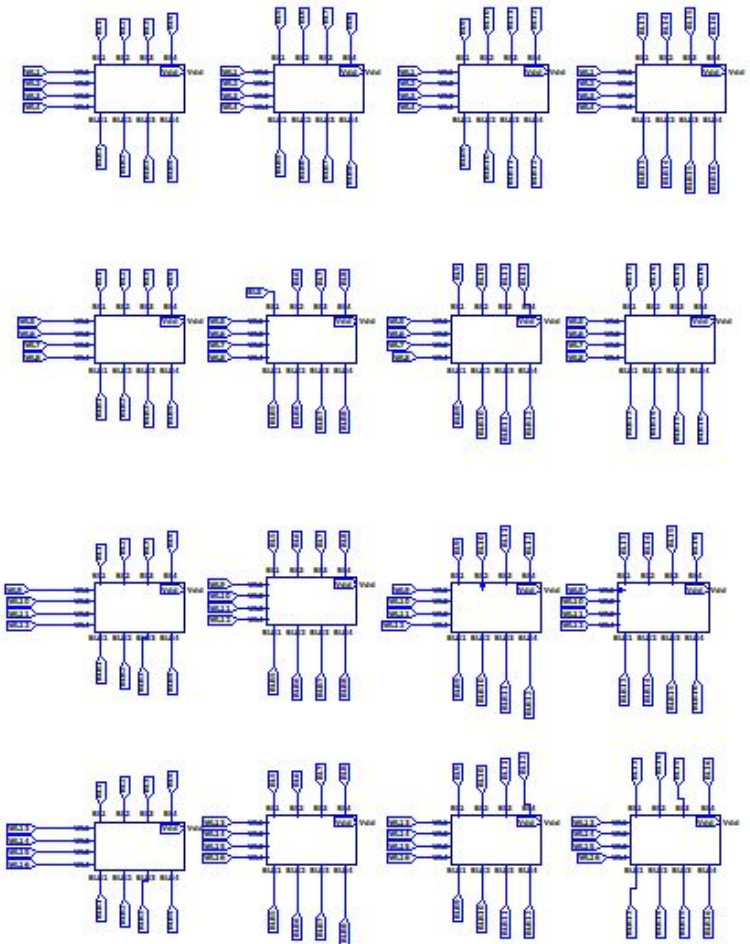
# 6T SRAM cell- Design factors

- Beta ratio (Cell Ratio)- I(PD)/I(PG)=1-2
- CR=180nm/135nm=1.33
- Gamma ratio (Pull-Up Ratio)- I(PU)/I(PG)=0.5-1
- PR=90nm/135nm=0.667
- Considered width→

- PDN=180 nm
- PG=135 nm (NMOS) and PG=270 nm(PMOS)
- PUN=180 nm

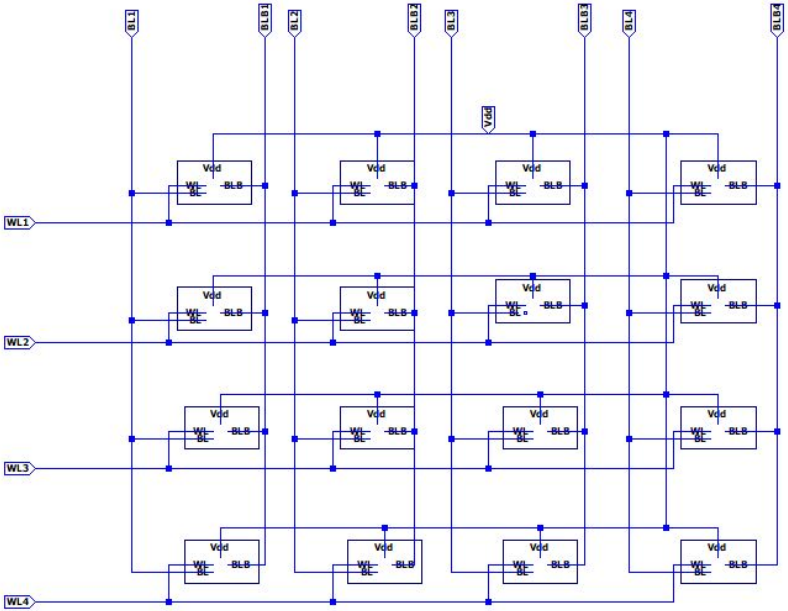
- Length = 45 nm
- Mobility of electron= 2 times mobility of holes

# SRAM cell Array

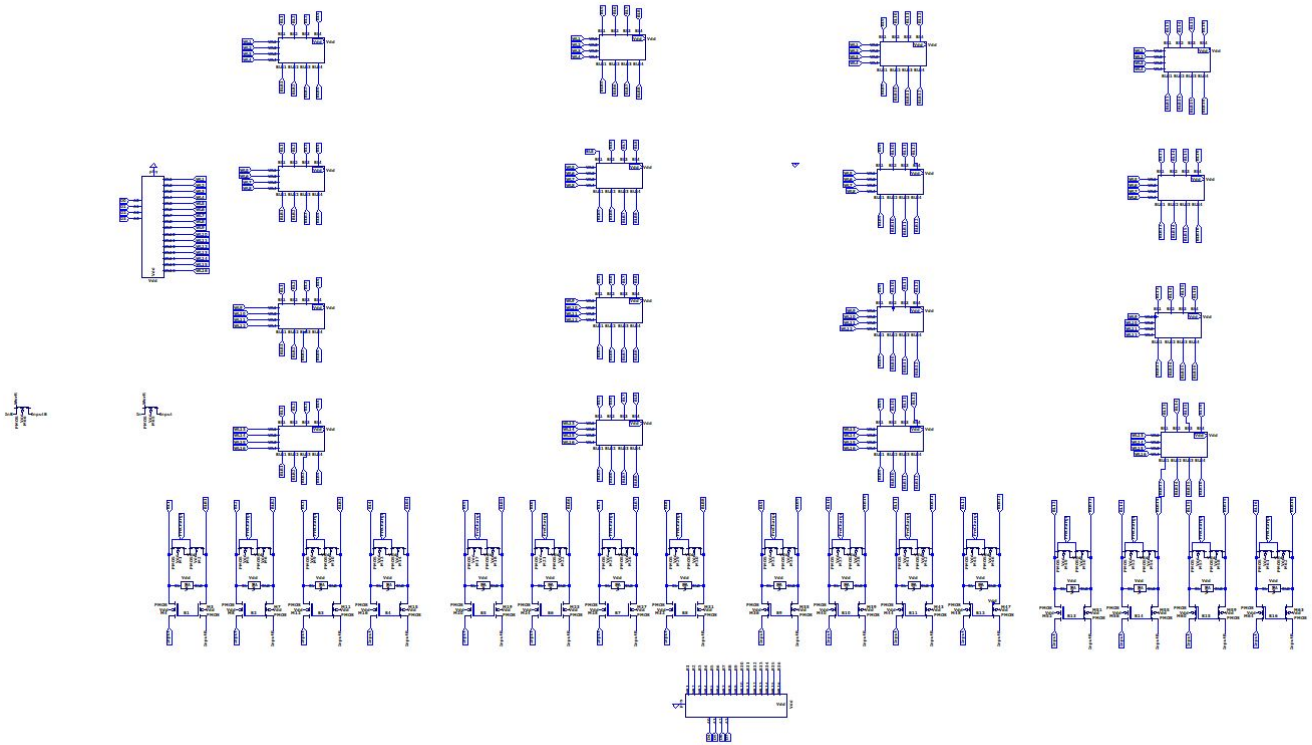


For the design→

- 6T
- 4x4 SRAM Array
- Extended to 16x16 SRAM array

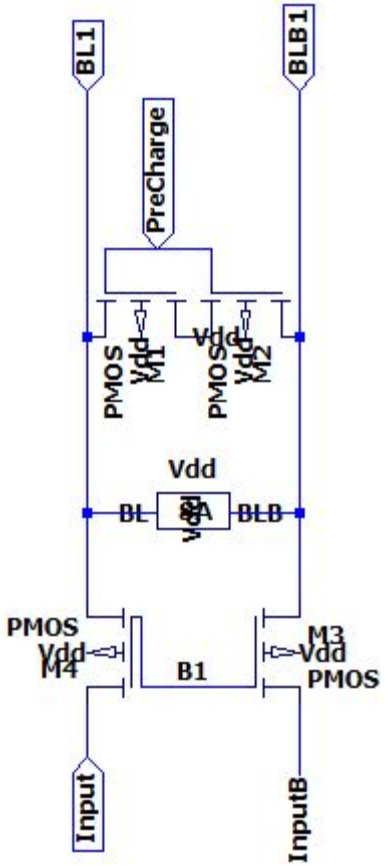


# Final design



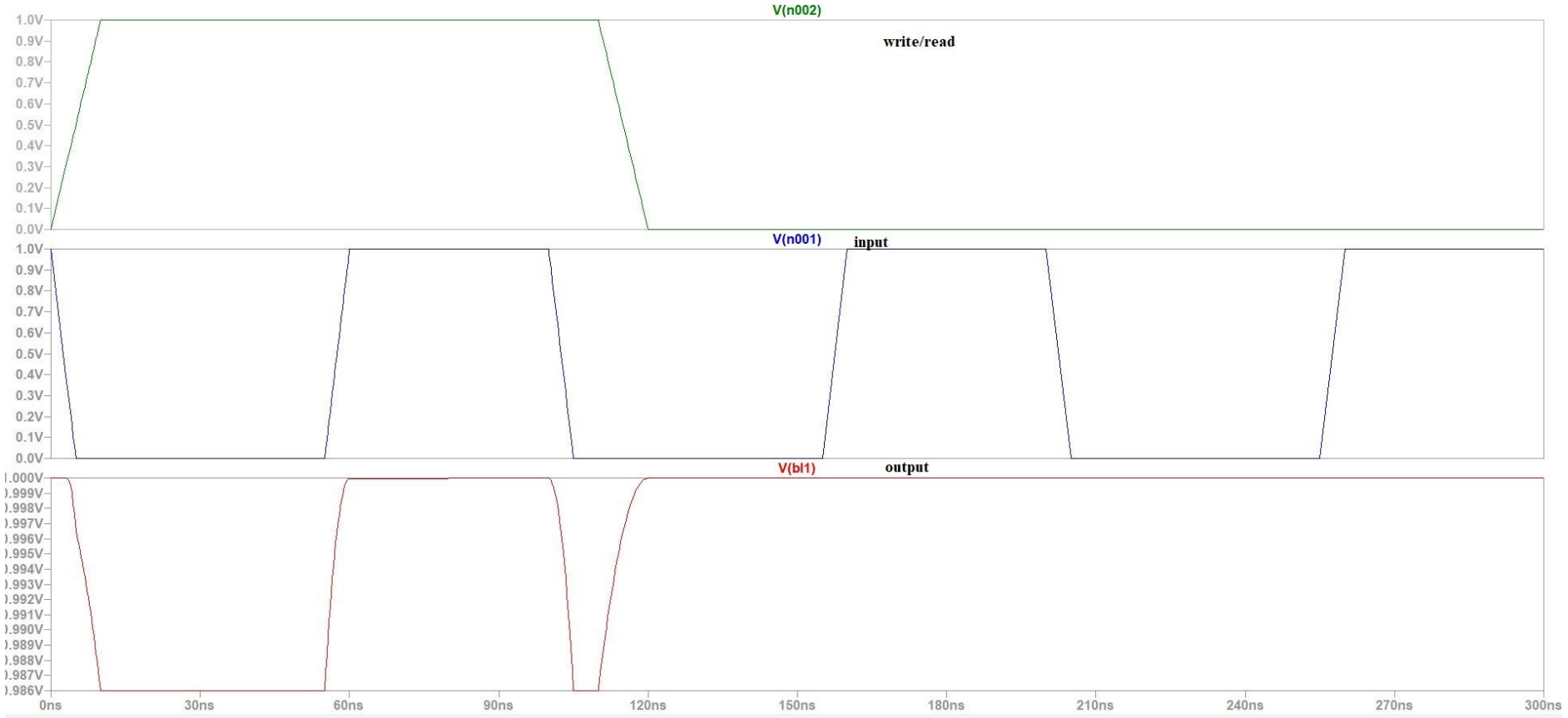
# Periphery circuitry

- Decoder output
- Sense Amplifier
- Precharge circuit

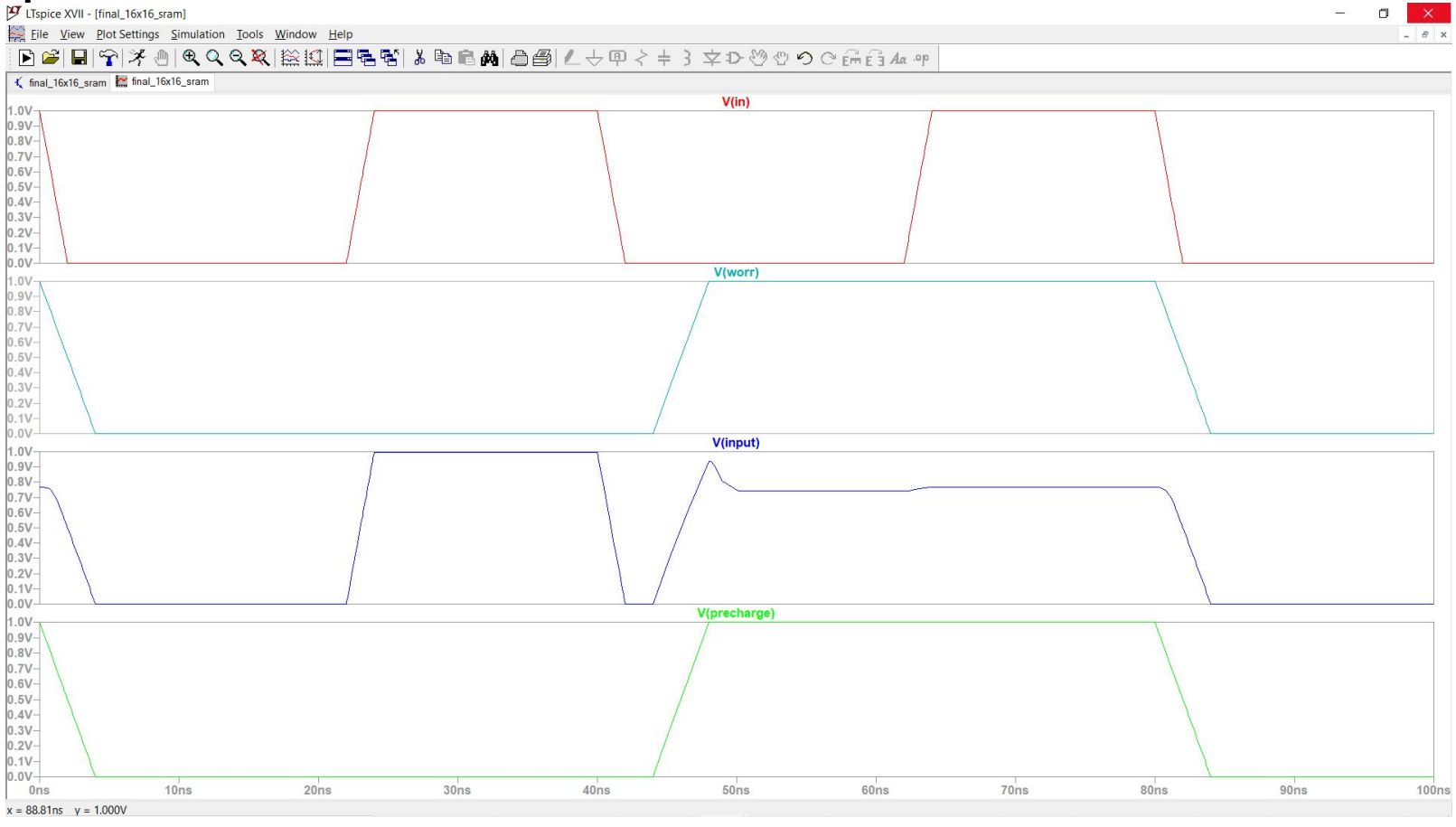


# Zero Write/Read operation

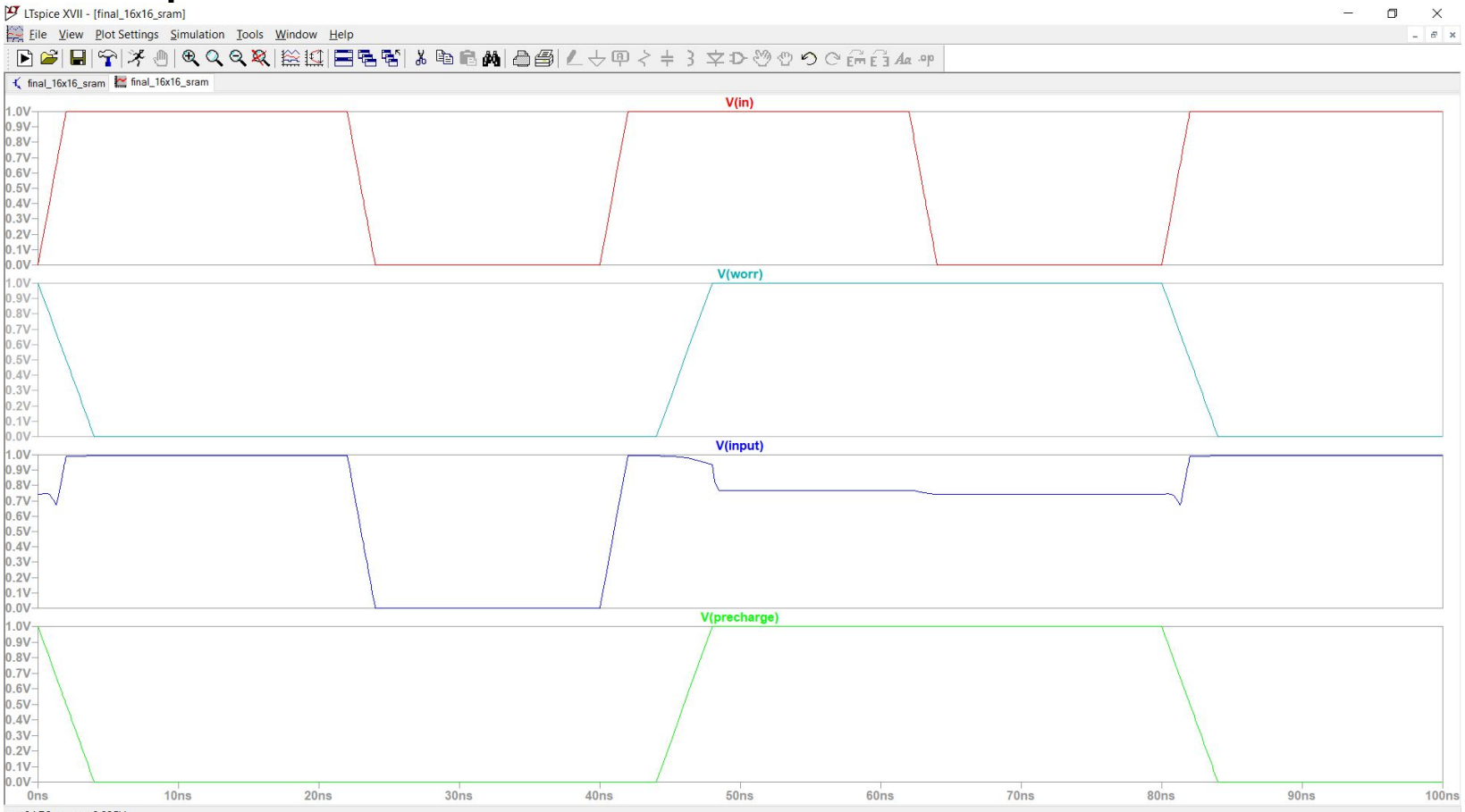
# One Write/Read operation



# 16x16 with Periphery circuit- Zero and One Write/Read operation



# 16x16 with Periphery circuit- One and Zero Writer/zero Read operation



# Thank you