512-point FFT Accelerator

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IIT PALAKKAD

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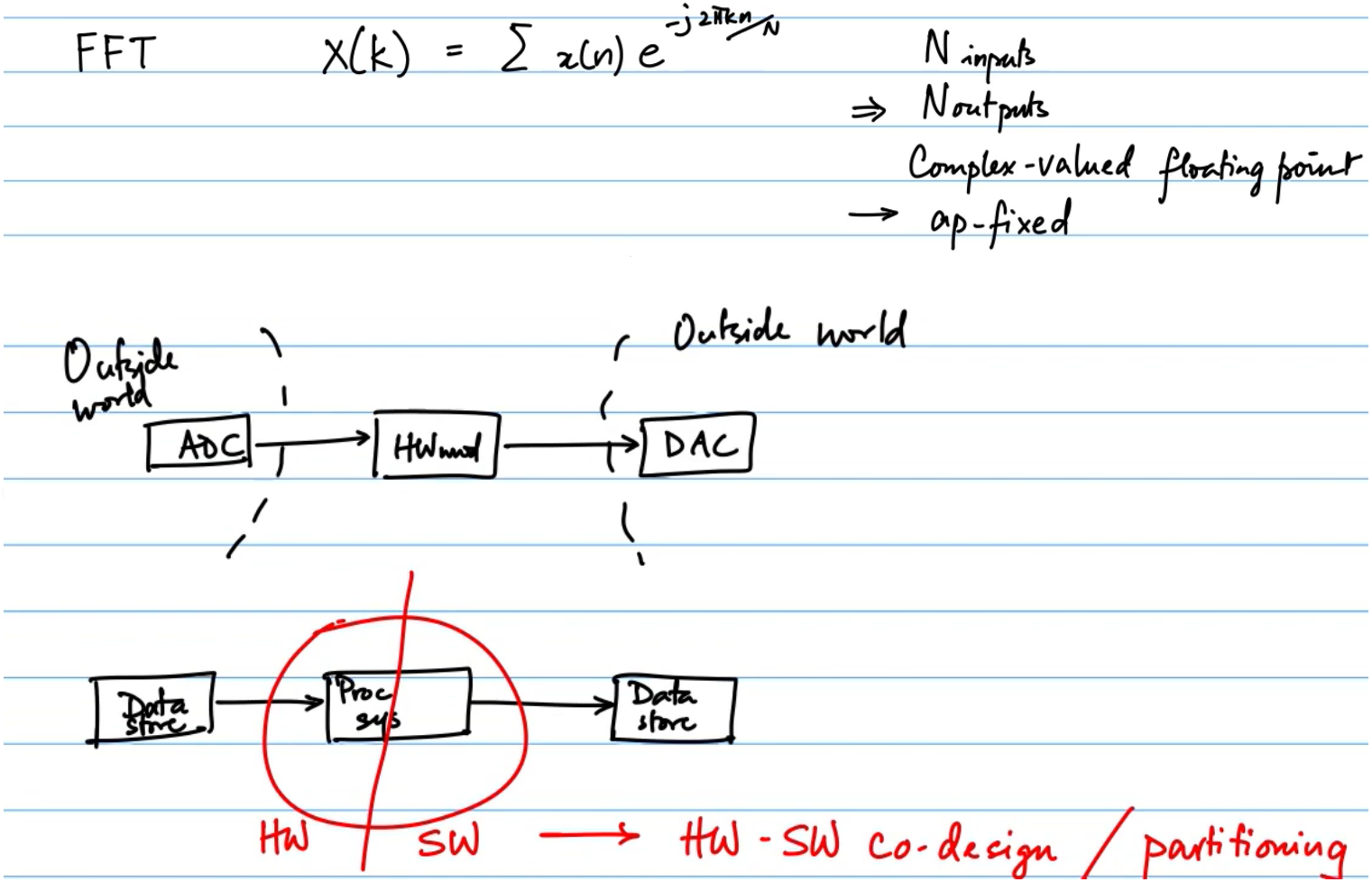
Section 1

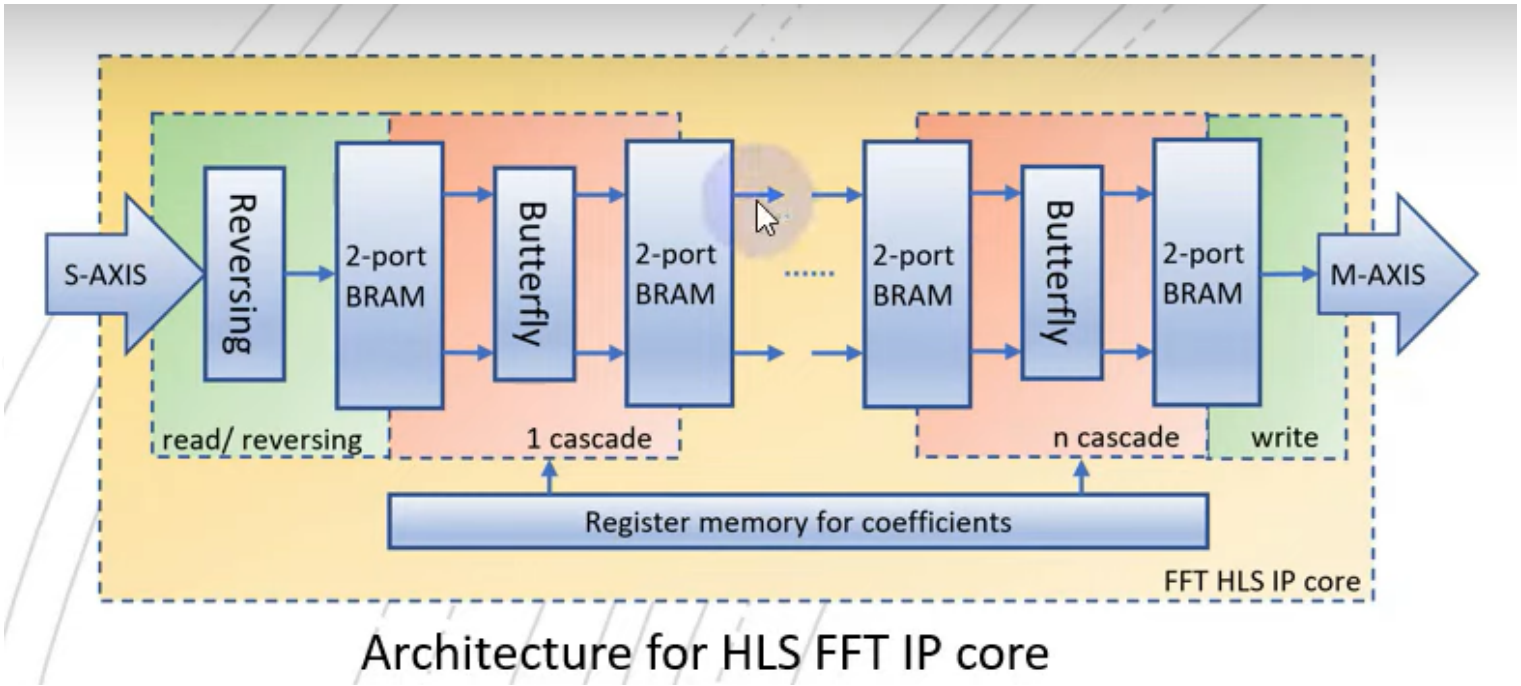
512 point DIT- FFT Hardware Accelerator



1. Design 512 FFT, which can help detect the peaks in PPG signals by identifying dominant pulse rate frequencies.

Section 2

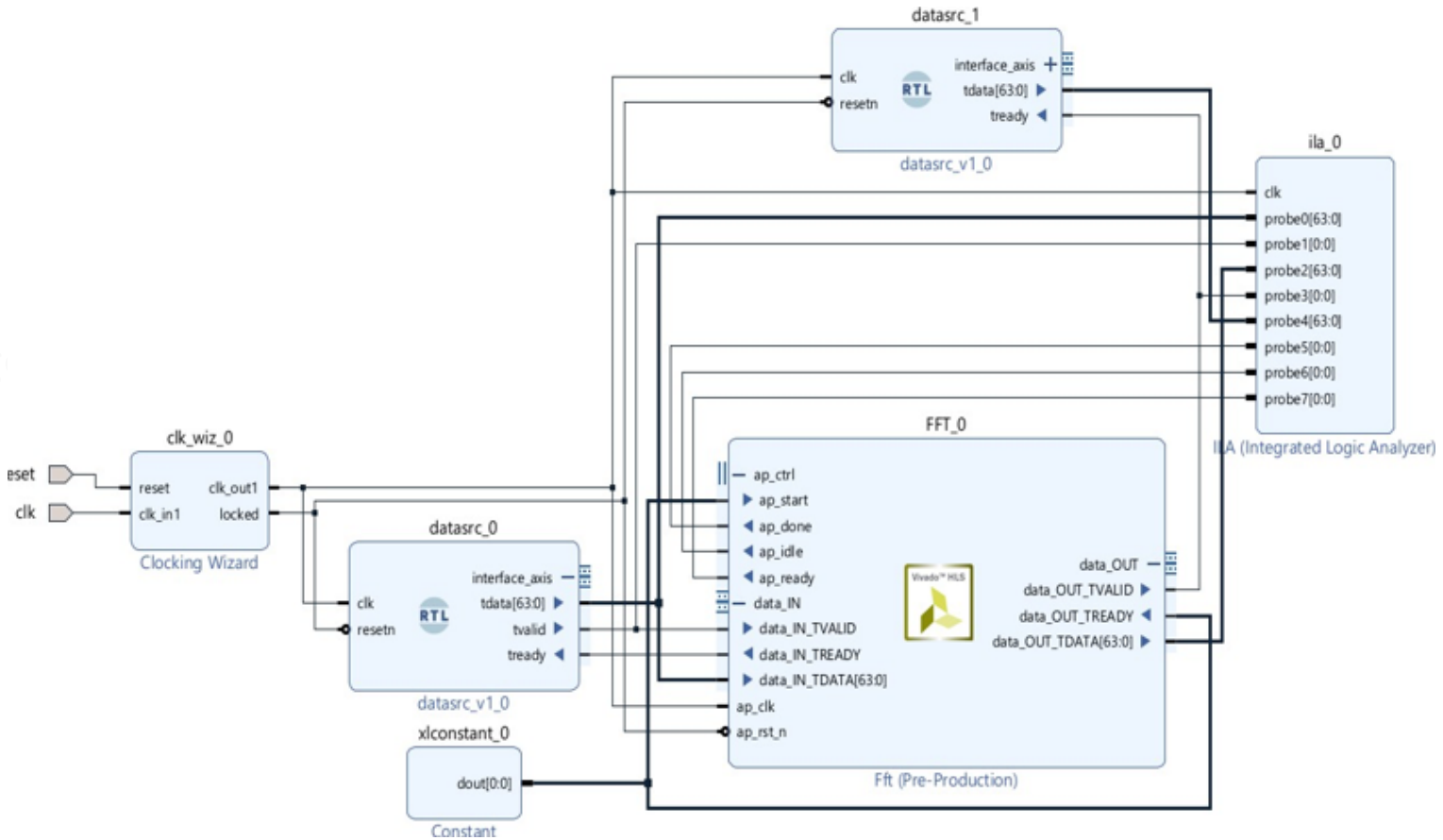
Architecture of 512-point FFT



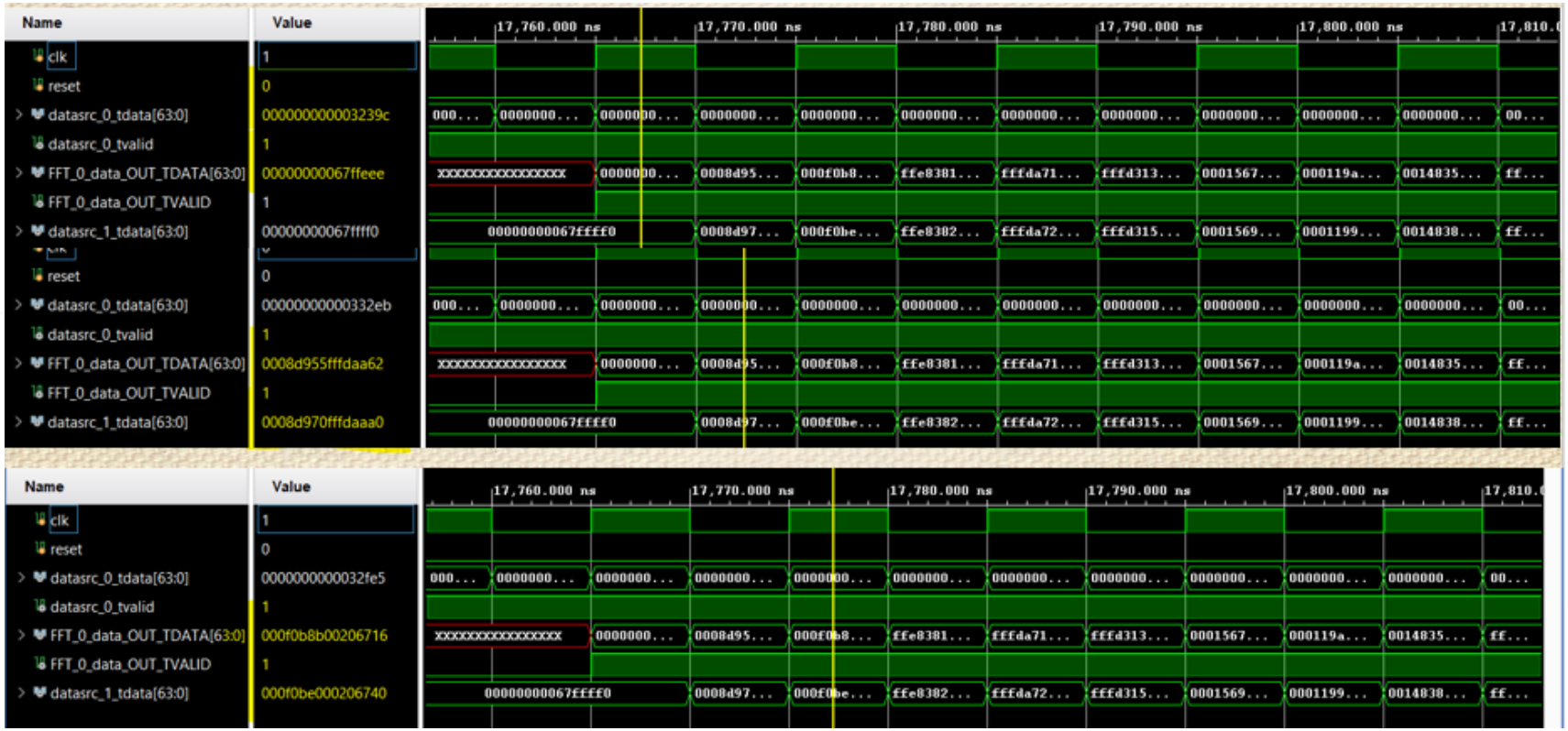
Architecture for HLS FFT IP core

Section 3

Block Diagram of 512-Point FFT using IP generated from HLS

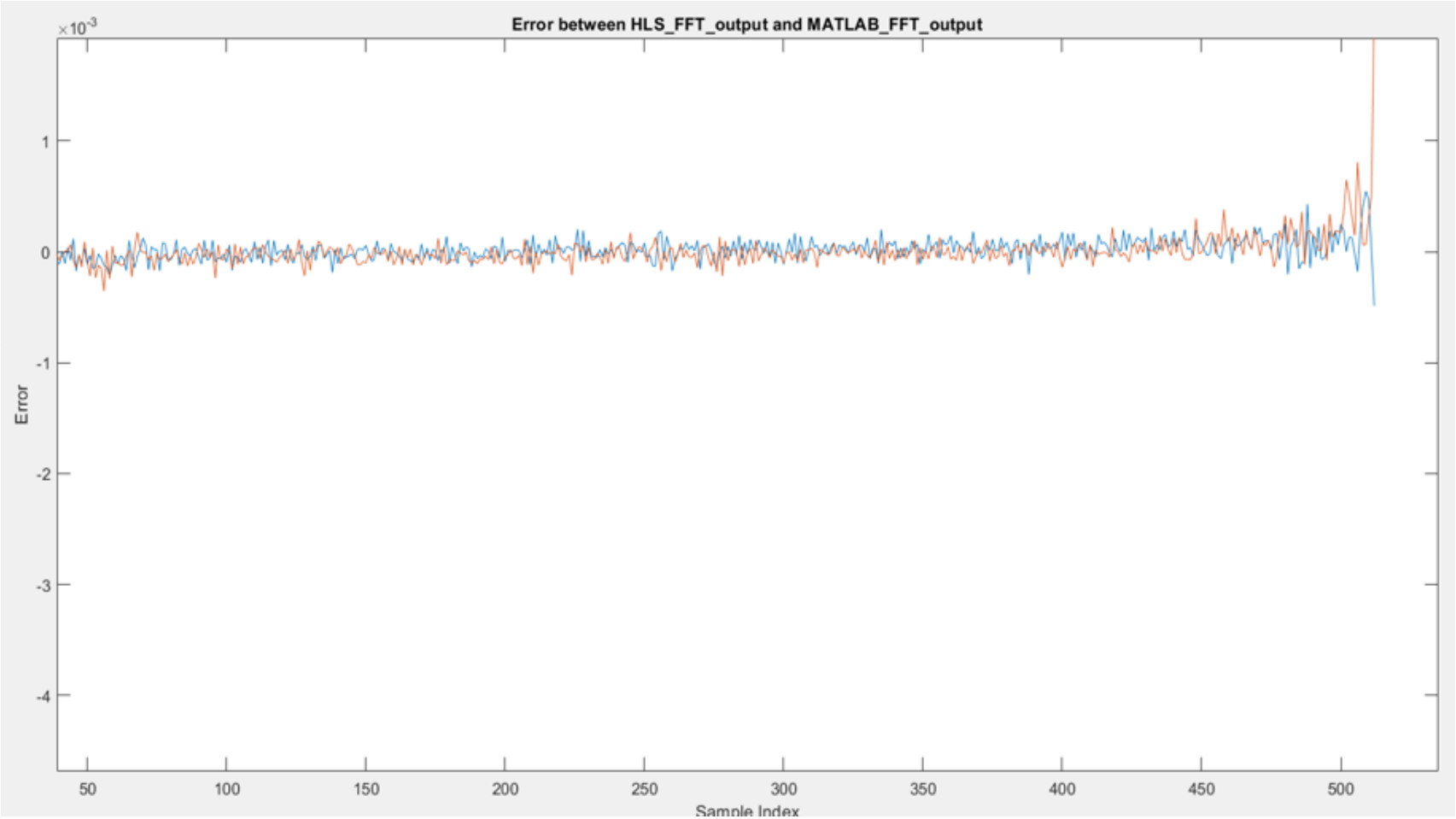


Simulation waveform for 512-Point FFT from Vivado

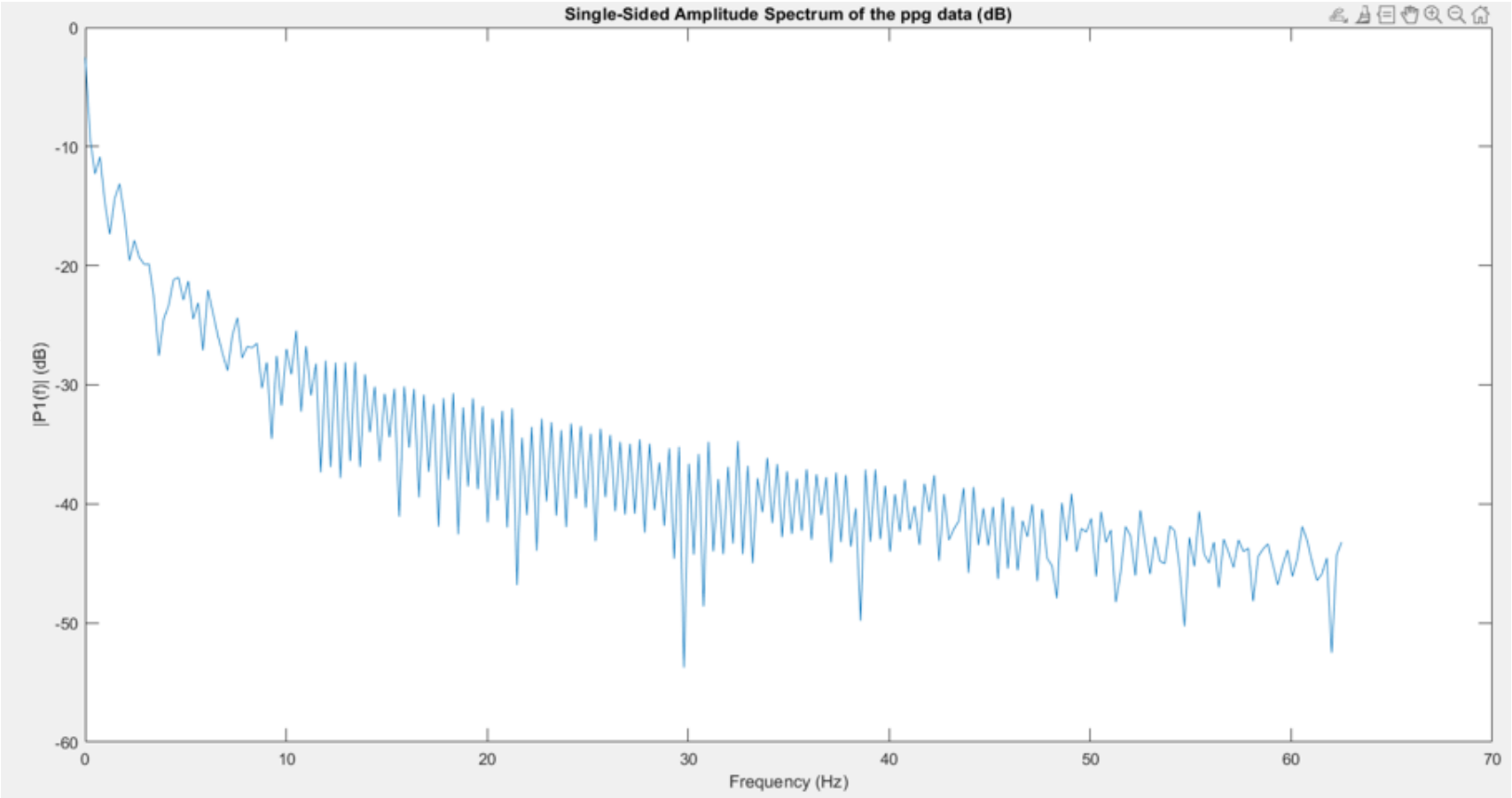


Section 4

Error plot comparing MATLAB FFT and HLS FFT



Magnitude of Amplitude spectrum of FFT for 125 Hz sample rate



Co-Simulation Report

Result

		Latency			Interval		
RTL	Status	min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	5428	5684	5941	1026	1026	1026

Export the report(.html) using the Export Wizard

Simulation report

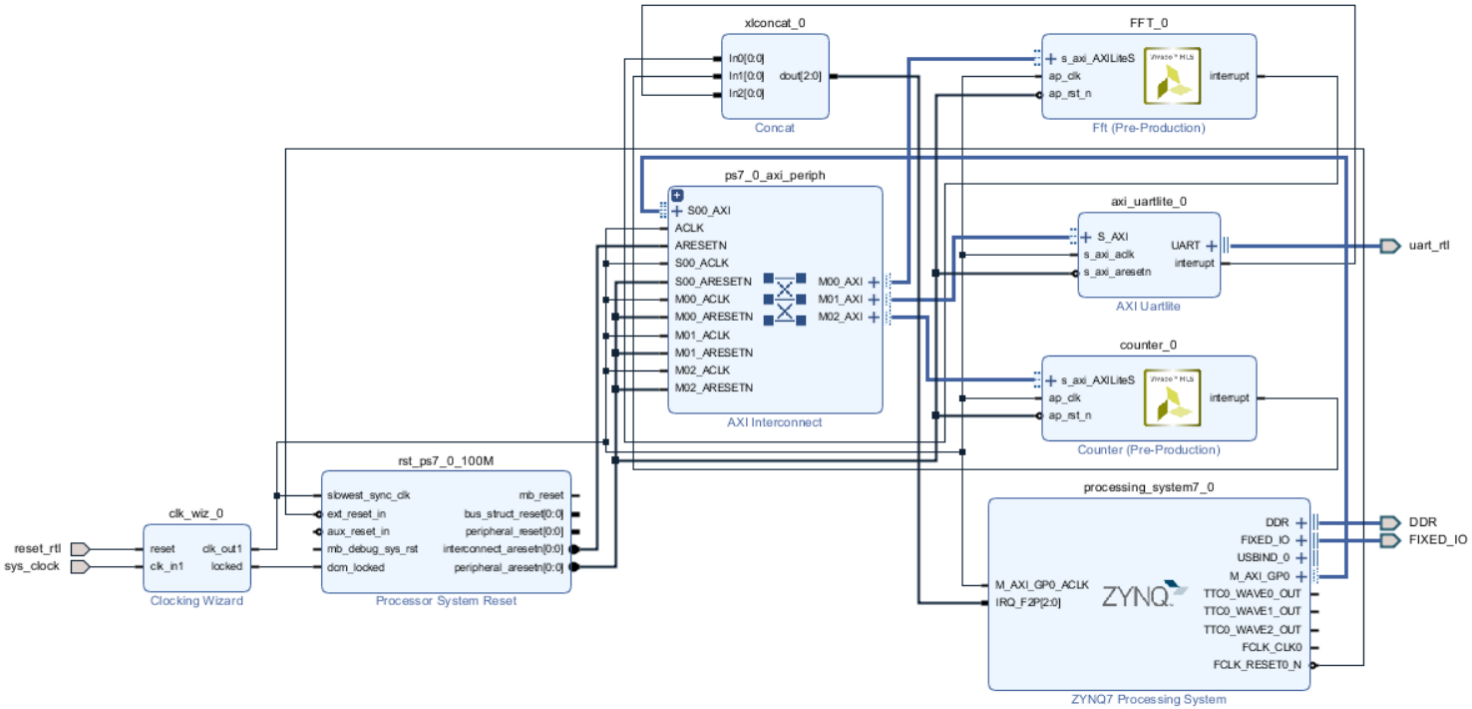
Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT
DSP	-	-	-	-
Expression	-	-	0	67
FIFO	-	-	-	-
Instance	19	72	4115	5018
Memory	84	-	0	0
Multiplexer	-	-	-	22
Register	-	-	22	-
Total	103	72	4137	5107
Available	120	80	35200	17600
Utilization (%)	85	90	11	29

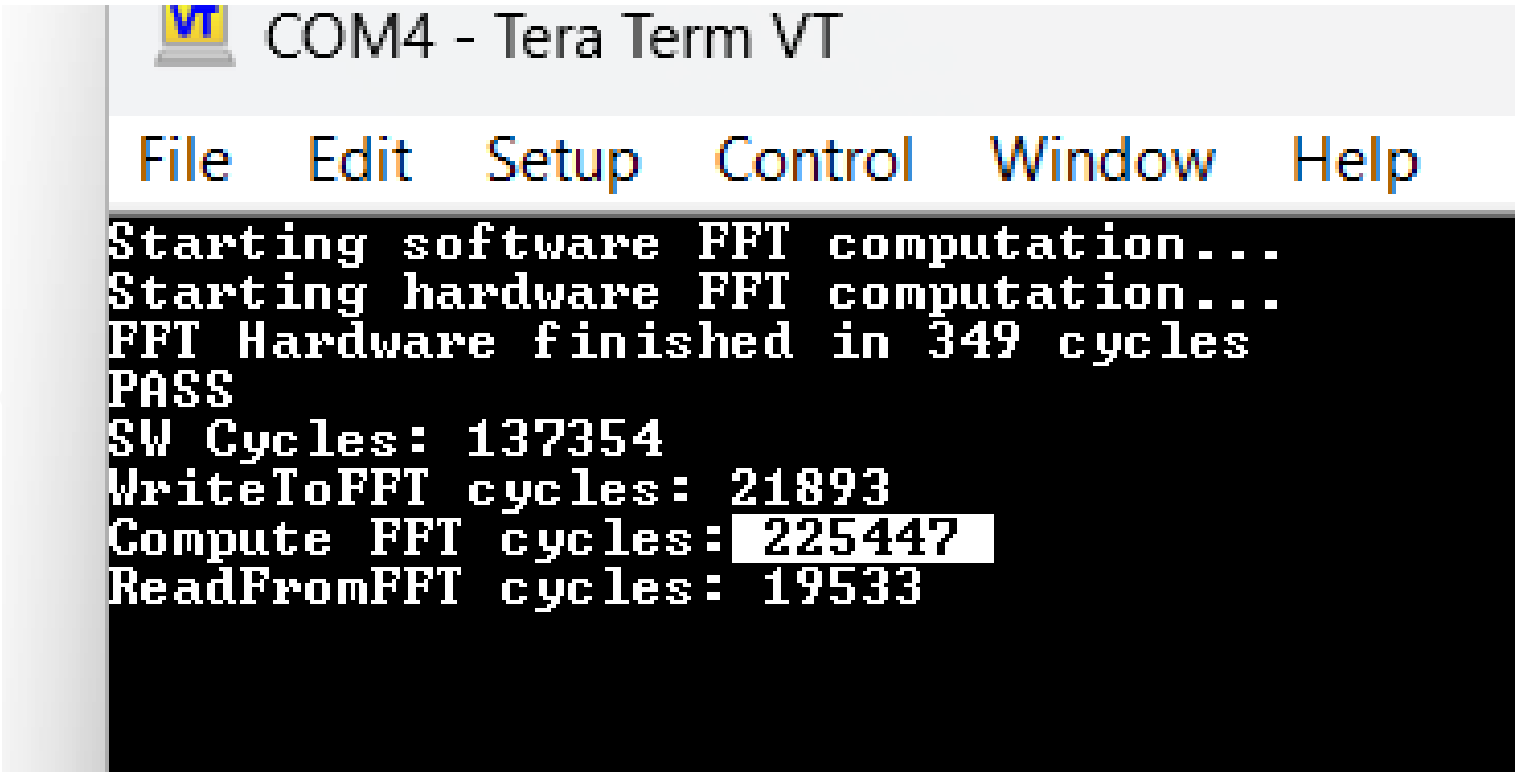
Section 5

SDK: Block Diagram of 512-Point FFT using ZYNQ PS



Section 6

Comparsion HW and SW



Section 7

Timing and Power report

DRC Violations

Summary: 101 warnings

Implemented DRC Report

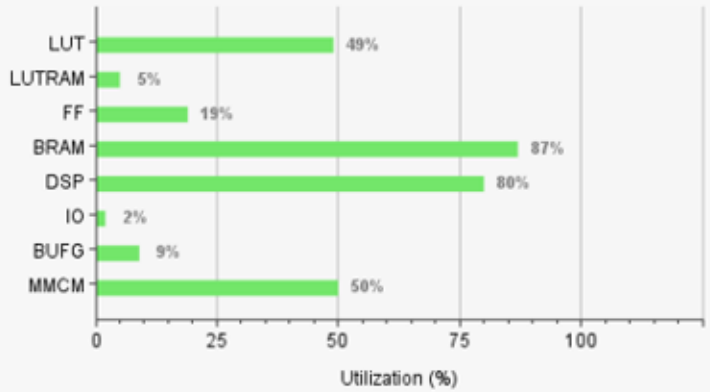
Timing Setup | Hold | Pulse Width

Worst Negative Slack (WNS):	2.379 ns
Total Negative Slack (TNS):	0 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	21444

Implemented Timing Report

Utilization Post-Synthesis | **Post-Implementation**

Graph | Table



Power **Summary** | On-Chip

Total On-Chip Power:	**0.457 W**
Junction Temperature:	**30.3 °C**
Thermal Margin:	54.7 °C (4.6 W)
Effective ϑJA:	11.5 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Medium

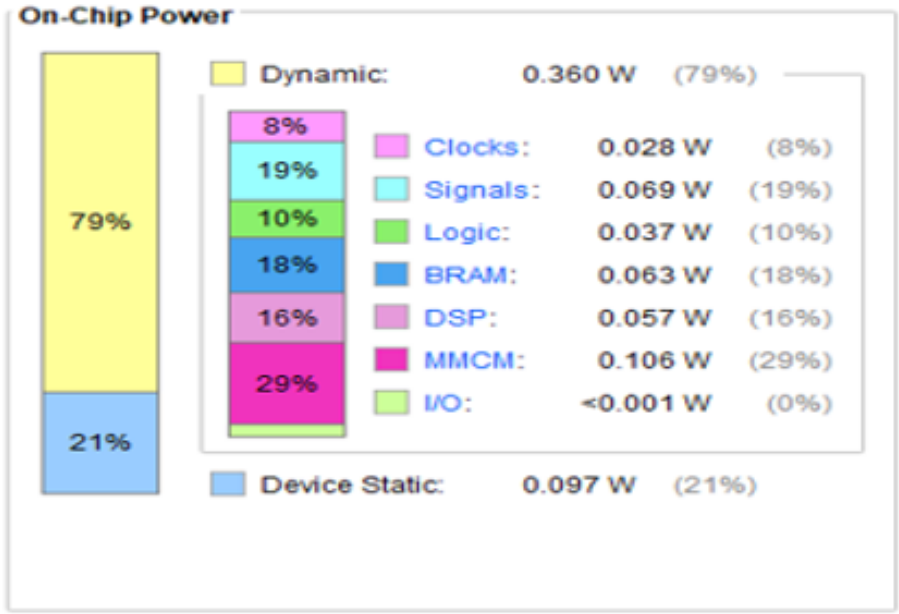
Implemented Power Report

Static and Dynamic Power report

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.457 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**30.3°C**
Thermal Margin:	54.7°C (4.6 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Medium

Launch Power Constraint Advisor to find and fix invalid switching activity



Area report

```
Report Cell Usage:
+------+---------+------+
|      |Cell     |Count |
+------+---------+------+
|1     |CARRY4   |    48|
|2     |CFGLUT5  |   156|
|3     |LUT1     |    36|
|4     |LUT2     |   230|
|5     |LUT3     |   108|
|6     |LUT4     |   136|
|7     |LUT5     |   106|
|8     |LUT6     |   573|
|9     |MUXF7    |    19|
|10    |RAMB18E1 |     1|
|11    |RAMB36E1 |     5|
|12    |SRL16E   |   201|
|13    |SRLC16E  |     2|
|14    |SRLC32E  |    17|
|15    |FDRE     |  2179|
|16    |FDSE     |    10|
+------+---------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:58 ; elapsed = 00:03:01 . Memory (MB): peak = 1860.633 ; gain = 972.688
---------------------------------------------------------------------------------
Synthesis finished with 0 errors, 0 critical warnings and 3231 warnings.
Synthesis Optimization Runtime : Time (s): cpu = 00:00:25 ; elapsed = 00:02:39 . Memory (MB): peak = 1860.633 ; gain = 972.688
Synthesis Optimization Complete : Time (s): cpu = 00:00:58 ; elapsed = 00:03:01 . Memory (MB): peak = 1860.633 ; gain = 972.688
INFO: [Project 1-571] Translating synthesized netlist
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.112 . Memory (MB): peak = 1860.633 ; gain = 0.000
```

Literature Survey

1. 32-bit posit FFTs can replace 64-bit float FFTs for many HPC tasks. Speed, energy efficiency, and storage costs can thus be improved by 2× for a broad range of HPC workloads.

References

Leong, S.H., Gustafson, J.L. (2023)
Lossless FFTs Using Posit Arithmetic.
https://doi.org/10.1007/978-3-031-32180-1_1

DSP Architecture NPTEL
Lecture: for Basics: 45, 46, 57, 58, 67, 68, 77, 80, 81, 83, For HLS design : 80, 82, For SDK: 89, 90, 91
https://www.youtube.com/watch?v=mkmWNUFBC5I&list=PLv78DAx1VAVlOVRc3kX62AsZ-igfw5D2q&index=91
https://gitlab.com/chandrachoodan/teach-fpga

Thank You!

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