UART Communication

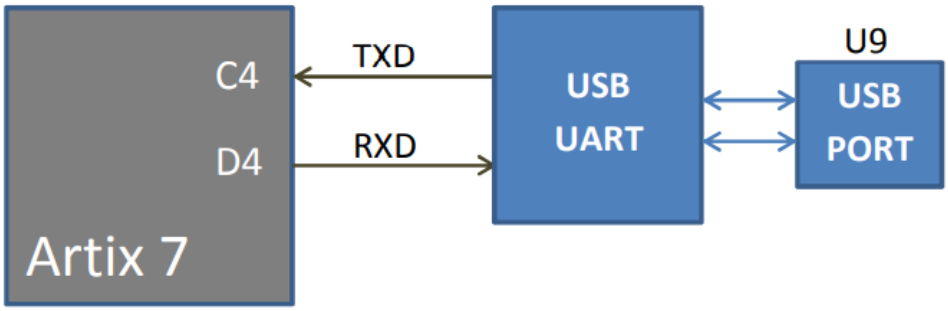
UART: Universal Asynchronous Receiver-Transmitter

It is one of the simplest and oldest forms of device-to-device digital communication. UARTs communicate between two separate nodes using a pair of wires and a common ground.

Why the name Asynchronous?

Interface with Edge Artix-7:

The EDGE Board includes FT2232H IC acts as USB UART Bridge to communicate board with windows PC COM port interface. The UART Transmitter and Receiver lines of FTDI chip is directly connected to the Artix 7 FPGA I/O pins for USB UART Communication.



Resource material:

1. https://www.analog.com/en/analog-dialogue/articles/uart-a-hardware-communication-protocol.html
2. https://www.electronicshub.org/basics-uart-communication/
3. https://www.allaboutcircuits.com/technical-articles/back-to-basics-the-universal-asynchronous-receiver-transmitter-uart/
4. https://electronoobs.com/eng_circuitos_tut26.php
5. https://youtu.be/lzQ9hJ-wevg?list=PLXHMvqUANAFOviU0J8HSp0E91lLJInzX1
6. https://youtu.be/J-nhxIiv2Uw?list=PLXHMvqUANAFOviU0J8HSp0E91lLJInzX1

UART-TxD Serial Communication using an FPGA Board | Verilog ➡ Step-by-Step Instructions

https://youtu.be/Fms2Qwkbu1g

UART-RxD Serial Communication using an FPGA Board ➡ Step-by-Step Instructions

https://youtu.be/XpfEHPg5AxU?list=PLqFzqzGMquZxGdkwBd9C2RSLIIlS5IxcK

Part-1:
Follow the above reference manual and resources design a module to transmit the data from FPGA to PC and using USB UART interface on Edge artix-7.

The modules are as follows:

1. Transmitter (Top level module)
2. Baud Rate Generator (uart_tx_clk)
3. UART transmission logic module (uart_tx)

The top level module as follows:

```
/*
This module is for transmitting 1 byte of data from FPGA to UART
Instructions:
1. Update XDC file
2. Generate Bitstream
3. Program FPGA
4. Make ld_tx_data high for load the data (and then low)
5. After loading the data make tx_enable high (to send the data)
6. Make reset high to reset the UART
*/

module transmiter(
   input clk,          //Connect this to System Clock
   input tx_enable,    //It will transmit the data when tx_enable is 1
   input reset,        //It will reset when posetive edge of reset is triggered
   input ld_tx_data,   //Positive edge of ld_tx_data will load tx_data to the transmitter
   output tx_empty,    //It is high when there is no data to send in the UART
   output tx_out       //This is TX of sender and connect this to RX of receiver
   );

wire [7:0]tx_data = 8'b01101100; //This data wil be send from UART

//---------------------- Uart TX ---------------------------------
uart_tx tx(reset,txclk,ld_tx_data,tx_data,tx_enable,tx_out,tx_empty);
uart_tx_clk clk_tx(clk,txclk);

endmodule
```

Part-2:
Follow the above reference manuals and resources design a module to receive the data from PC to FPGA and using USB UART interface on Edge artix-7.