EDGE Artix 7 FPGA Development Board

User Manual

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Introduction

EDGE Artix 7 FPGA Development board is the feature rich development board with Artix 7 FPGA, SPI FLASH, SRAM, HDMI, Micro SD, Wi-Fi, Bluetooth, ADC, DAC, LCD, 7 segment Display, VGA, , Stereo Jack, buzzer, Push Button, Slide Switch, LED, Temperature Sensor and LDR. The Board also provides additional interface like CMOS Camera and TFT Display at the expansion connectors.

The EDGE board provides USB JTAG interface for Programming and Debugging. It also provides USB UART interface.
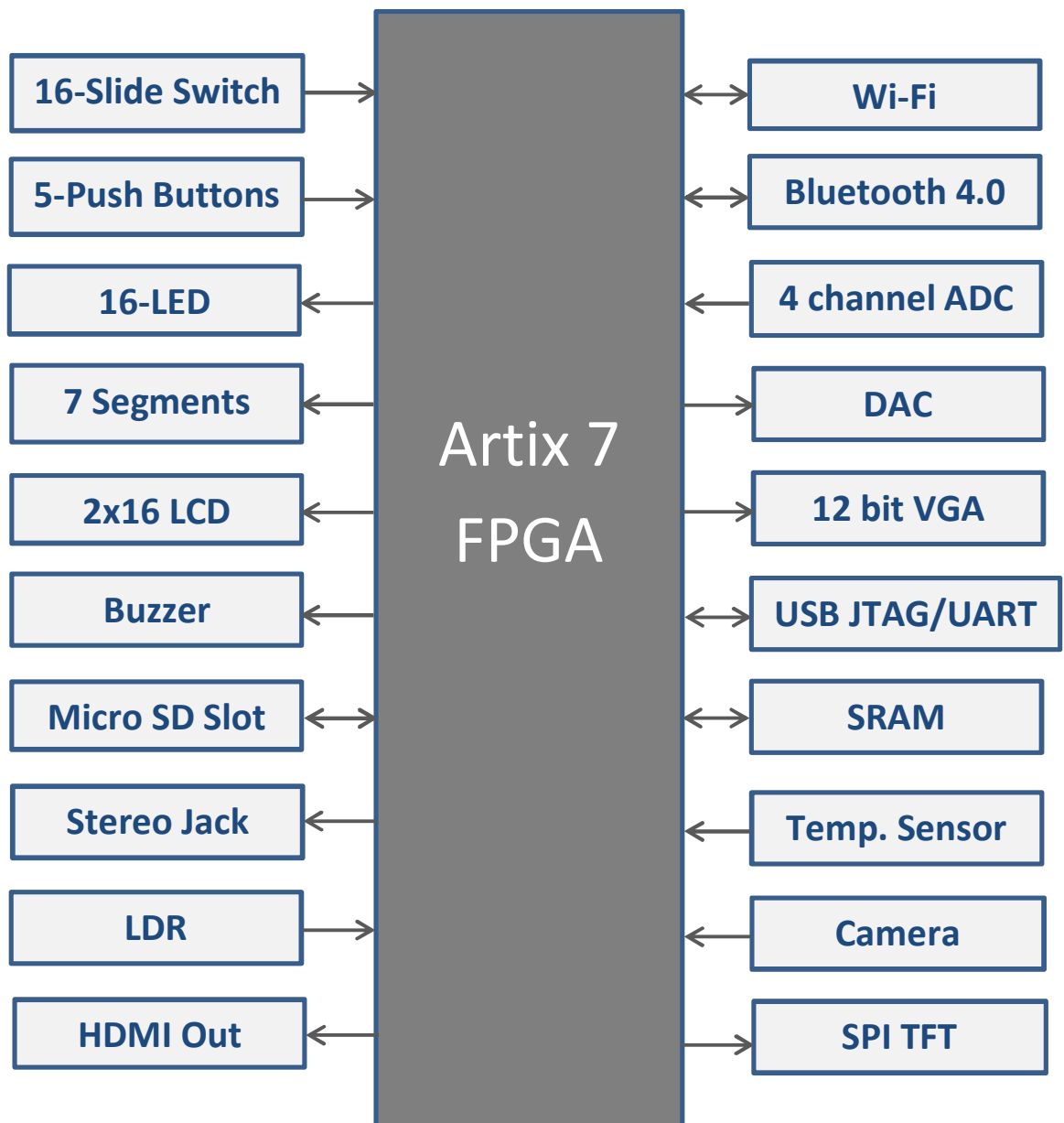
Board Applications

- Wireless control
- Environment monitor
- IoT (Internet of Things)
- Product Prototyping
- Image Processing

- Video Processing
- Audio Processing

Board Features

- Xilinx XC7A35T-1FTG256 Artix 7 FPGA
- 8MB SPI FLASH Memory
- 512 KB SRAM
- HDMI Out
- Micro SD Slot
- On-Board USB JTAG Programmer
- USB to UART Interface
- WIFI Interface
- Low Power Bluetooth Interface
- 12 bit VGA Interface
- 8 Channel SPI ADC
- Temperature Sensor
- LDR Interface
- SPI DAC
- 2×16 LCD Display
- 4 Digit Seven Segment Display
- 5v Buzzer
- CMOS Camera Interface
- TFT Display Interface

16-Slide Switch	→		←	Wi-Fi
5-Push Buttons	→		←	Bluetooth 4.0
16-LED	←		←	4 channel ADC
7 Segments	←		→	DAC
2x16 LCD	←	Artix 7 FPGA	→	12 bit VGA
Buzzer	←		↔	USB JTAG/UART
Micro SD Slot	↔		↔	SRAM
Stereo Jack	←		←	Temp. Sensor
LDR	→		←	Camera
HDMI Out	←		→	SPI TFT

Block Diagram of EDGE Artix 7 FPGA Development Board

Power Supply

EDGE Artix 7 development board can get 5V power from either USB JTAG Port U9 or External Power Supply connector J5. Switch **SW2** can be used to select the source of power from USB or External Power Supply.

Board consist of 3 Voltage regulators 3.3v, 1.8v and 1v. The Kit requires 3.3v supply for FPGA I/O, SRAM, Clock, USB, ADC, DAC, FLASH, and so on. The 1.8v Voltage is for FPGA Auxiliary supply and ADC. The 1v power supply is dedicated for FPGA Core and Block RAM voltage.

Caution: Only 5v Supply must be provided to the board either from external source or USB connector.

Programming hardware

FPGA can be configured either from USB JTAG using Xilinx Vivado software or by on-board SPI FLASH Memory.

FPGA configured through JTAG gets erased when the power supply is removed or by pressing reset button **SW1**.

To store the data permanently on FPGA, we have to store the configuration bit file to SPI FLASH Memory. It automatically reconfigures the FPGA after reset or Power on.

The EDGE Artix 7 FPGA Development board is fully compatible with Xilinx Vivado design suite with on-board USB JTAG Interface.

USB UART

The EDGE Board includes FT2232H IC acts as USB UART Bridge to communicate board with windows PC COM port interface.

The UART Transmitter and Receiver lines of FTDI chip is directly connected to the Artix 7 FPGA I/O pins for USB UART Communication.
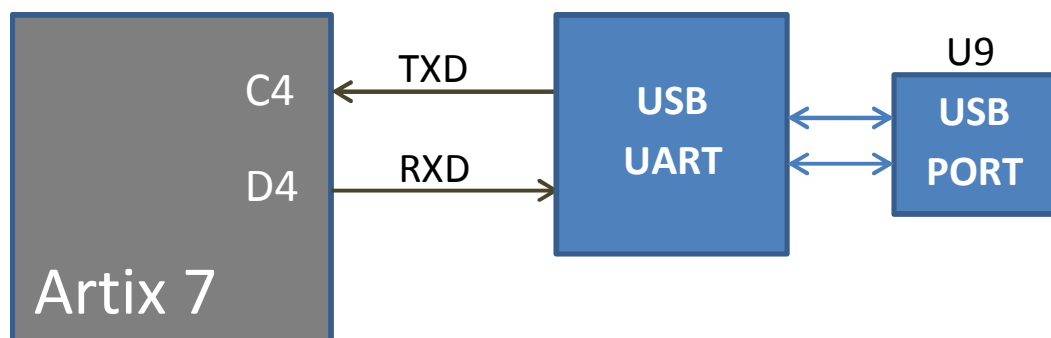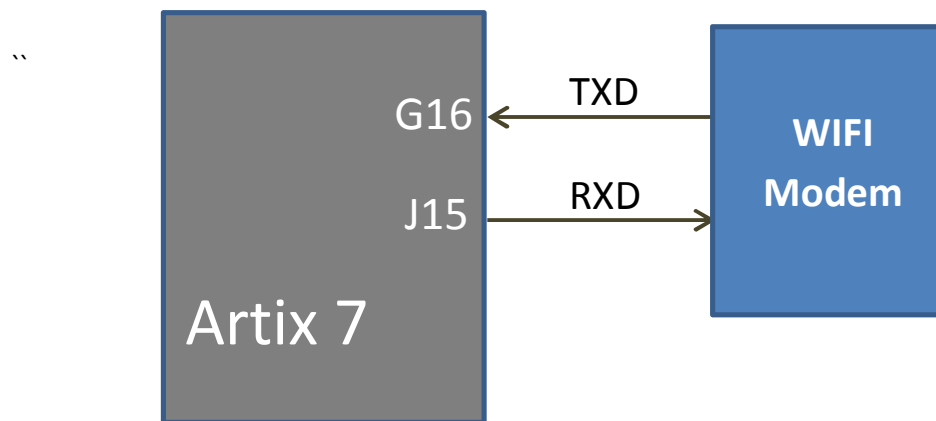
WIFI Communication

The EDGE Board contains On-board ESP8266 12F WIFI Module connected with Artix 7 FPGA through serial interface. The ESP WIFI Modem helps to communicate FPGA with cloud. The Data can be stored and retrieved from the cloud with the help of AT Commands. The range of communication for WIFI modem is 50 – 100 meter distance.

Note: To enable power supply to the WIFI Modem, place jumper at Enable and centre pin of J3. To disable power, place jumper at Disable and centre pin of J3.

J2 connector got TX, RX and GPIO0 Line of ESP12F WiFi module for testing and firmware update.


Bluetooth Communication

The EDGE contains low power Bluetooth 4.0 BLE interface on-board. The Bluetooth Module CC2541 is serially interfaced with FPGA with Transmit and Receive lines.

Note: To enable power supply to the Bluetooth Modem, place jumper at Enable and centre pin of J4. To disable power, place jumper at Disable and centre pin of J4.

J6 connector got TX, RX and Key Line of Bluetooth module for testing and firmware update.
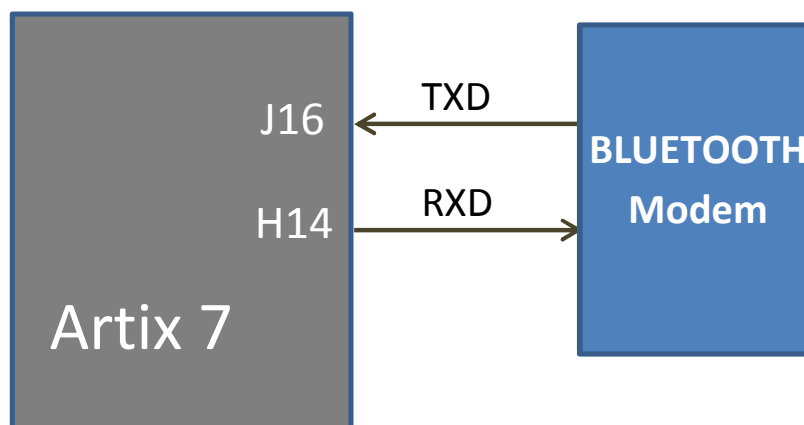
Slide Switches

The EDGE board includes 16 SPDT slide switches for digital input. These digital inputs are connected to Artix 7 FPGA through resistors for protection against short circuit. Slide switch outputs constant high or constant low based on the user changing its position.
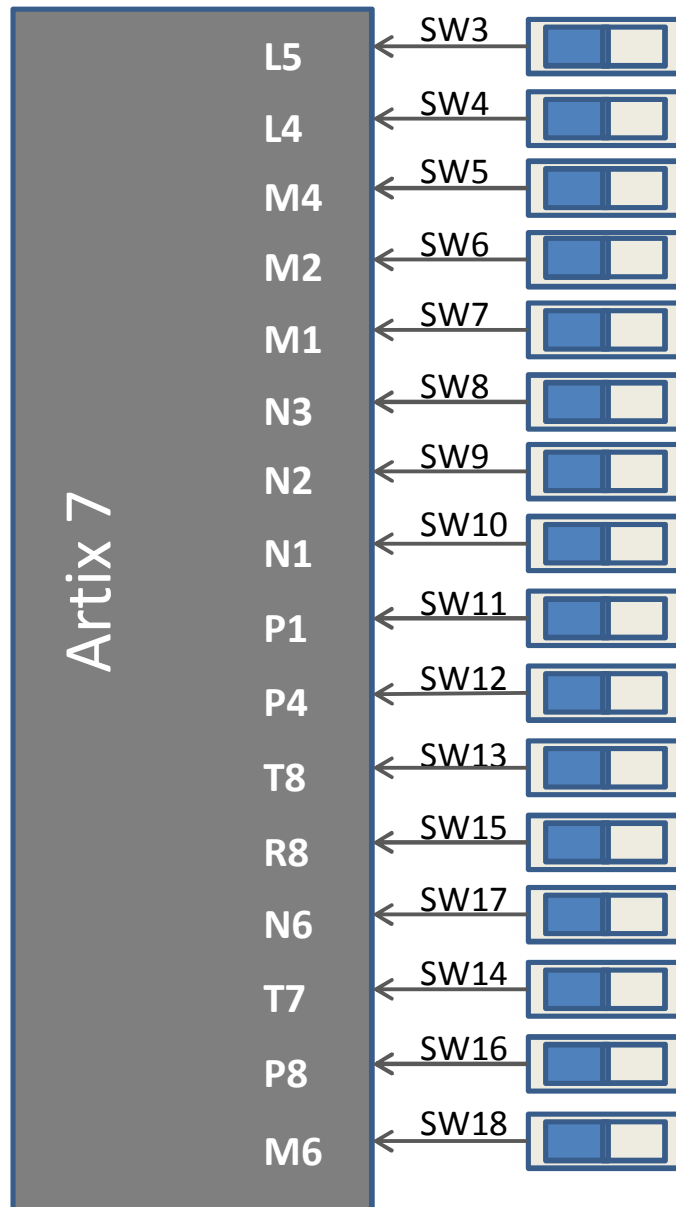
Push Buttons

The Board contains 5 Push buttons for providing momentary digital inputs. They are connected to FPGA lines through resistors to prevent short circuit. By default the switch is in Active low. When the user pressed the push button they are driven high.
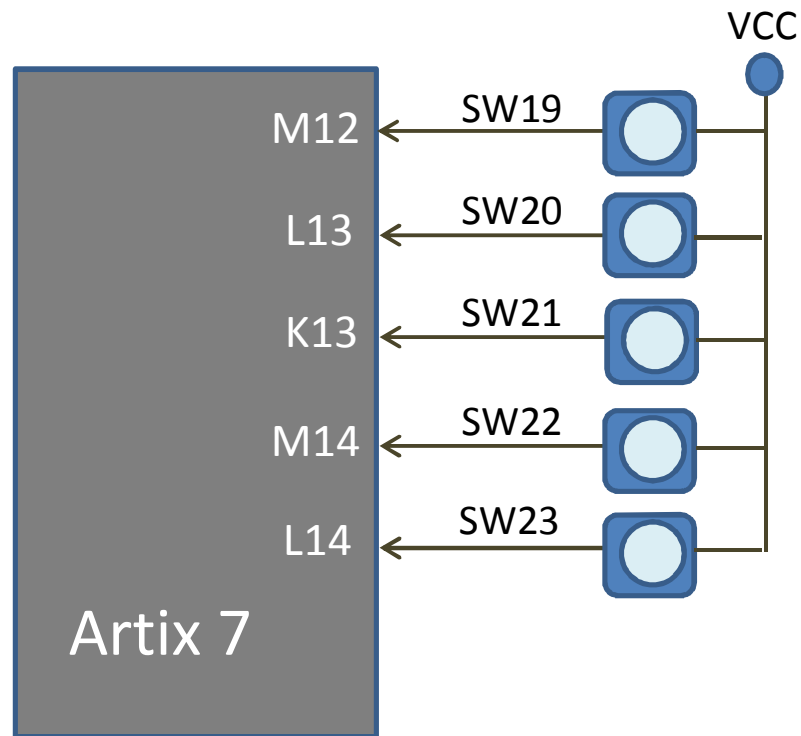
LEDs

The Kit consists of 16 LEDs for displaying digital outputs. These LED's are connected with FPGA through a series resistor. Logic High signal turns ON LED and Logic Low signal turns OFF LED to demonstrate the digital output.
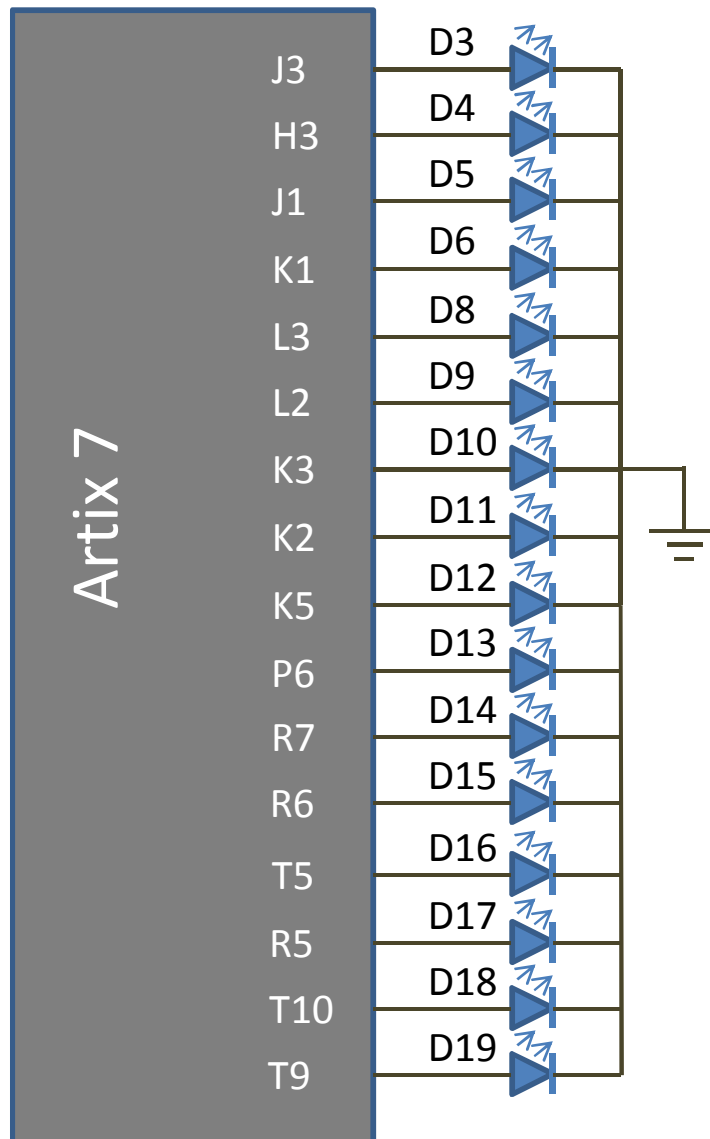
Seven segment Display

The EDGE Board consist of 4 digit 7 segment displays with common anode. Each of the seven segment contains LEDs can be turned on by sending active low signal.
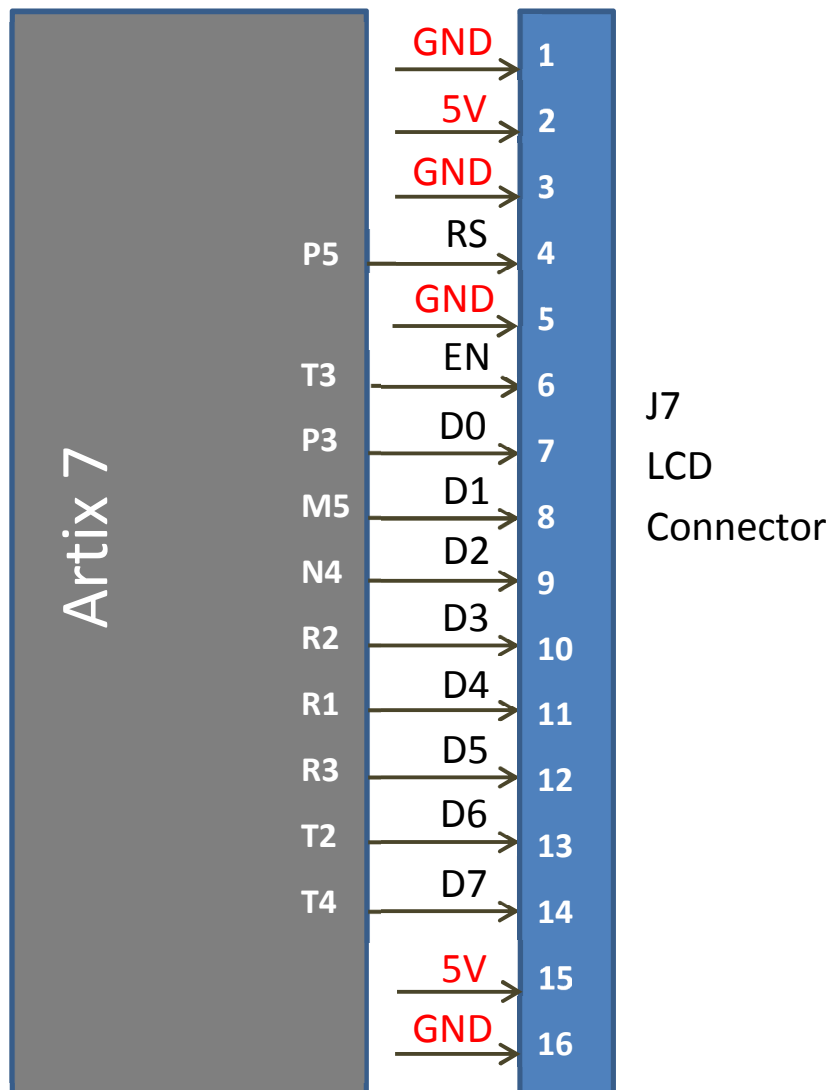
For example, to display digit 8 in the seven segments display. All the segments are enabled using active low '0' signal.
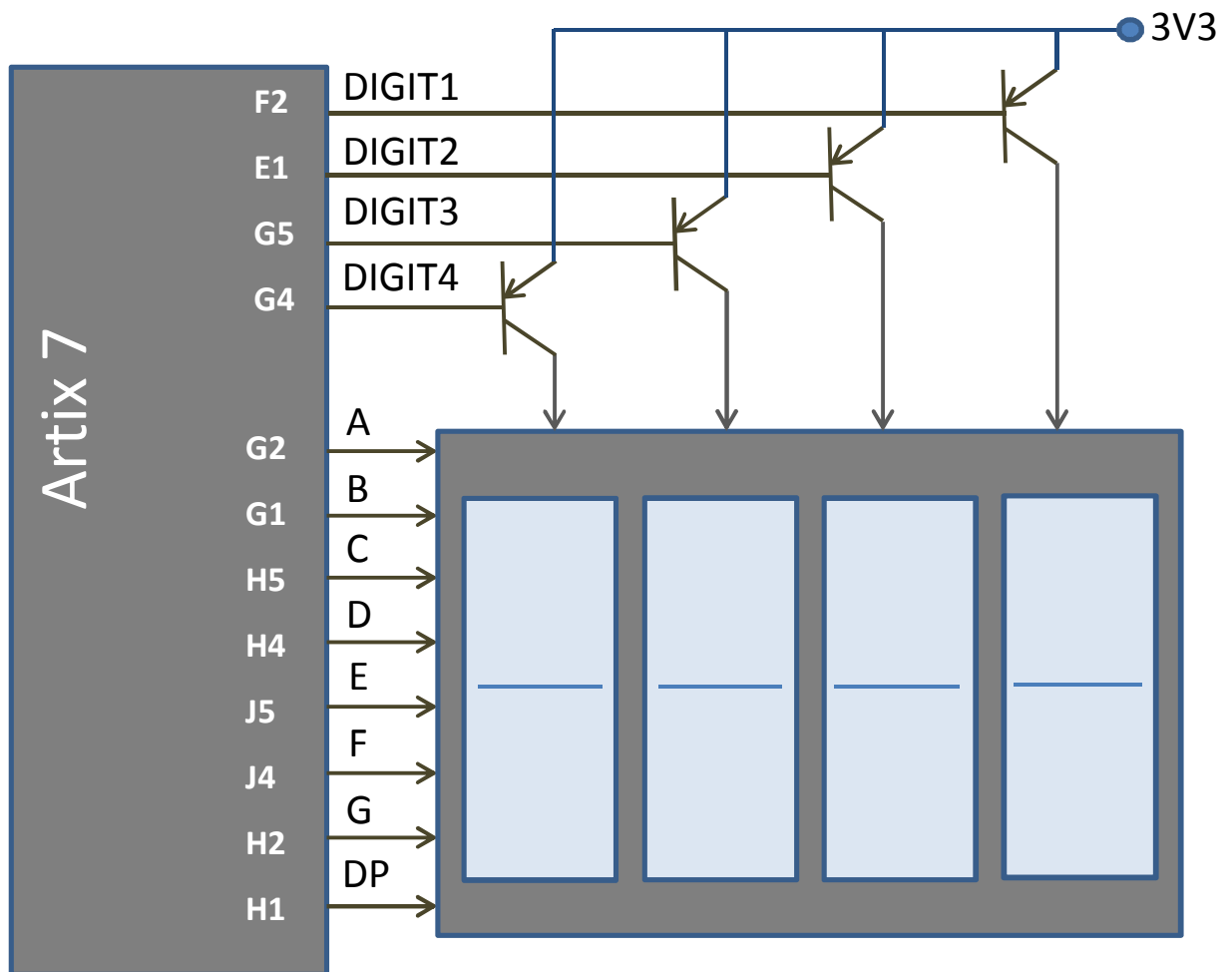
2x16 LCD

The EDGE board consist of 2x16 LCD interface at the female connector J7. LCD displays is interfaced in the 8 bit data mode, RS pin are used to select data/command mode and En are used to enable the LCD.

Note: R/W pin is connected to ground to keep LCD in always write mode.

| Artix 7 pin	Signal	J7 LCD Connector pin
	GND	1
	5V	2
	GND	3
P5	RS	4
	GND	5
T3	EN	6
P3	D0	7
M5	D1	8
N4	D2	9
R2	D3	10
R1	D4	11
R3	D5	12
T2	D6	13
T4	D7	14
	5V	15
	GND	16

Analog Input

Pins 5, 6, 7 and 8 of the J13 ADC connector are used as analog inputs to the XADC module of the Artix 7 FPGA. The FPGA expects that the inputs range from 0-1 V, so we use an external circuit to scale down the input voltage from 3.3V. This circuit is shown in Figure. This circuit allows the XADC module to accurately measure any voltage between 0V and 3.3V that is applied to these pins.

The XADC core within the Artix-7 is a dual channel 12-bit analog-to-digital converter capable of operating at 1 MSPS. Either channel can be driven by any of the two auxiliary analog inputs connected to the DIP pins. The XADC core is controlled and accessed from a user design via the Dynamic Reconfiguration Port (DRP). The DRP also provides access to voltage monitors that are present on each of the FPGA's power rails, and a temperature sensor that is internal to the FPGA. For more information on using the XADC core, refer to the Xilinx document titled 7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter.

External Temperature Sensor LM35 Input is available at the 9th pin of ADC Connector. To Connect Temperature sensor with XADC, Place a jumper between 7th and 9th pin of J13 Connector.

LDR input is available at the 10th pin of ADC Connector. To Connect LDR sensor with XADC, Place a jumper between 8th and 10th pin of ADC Connector.
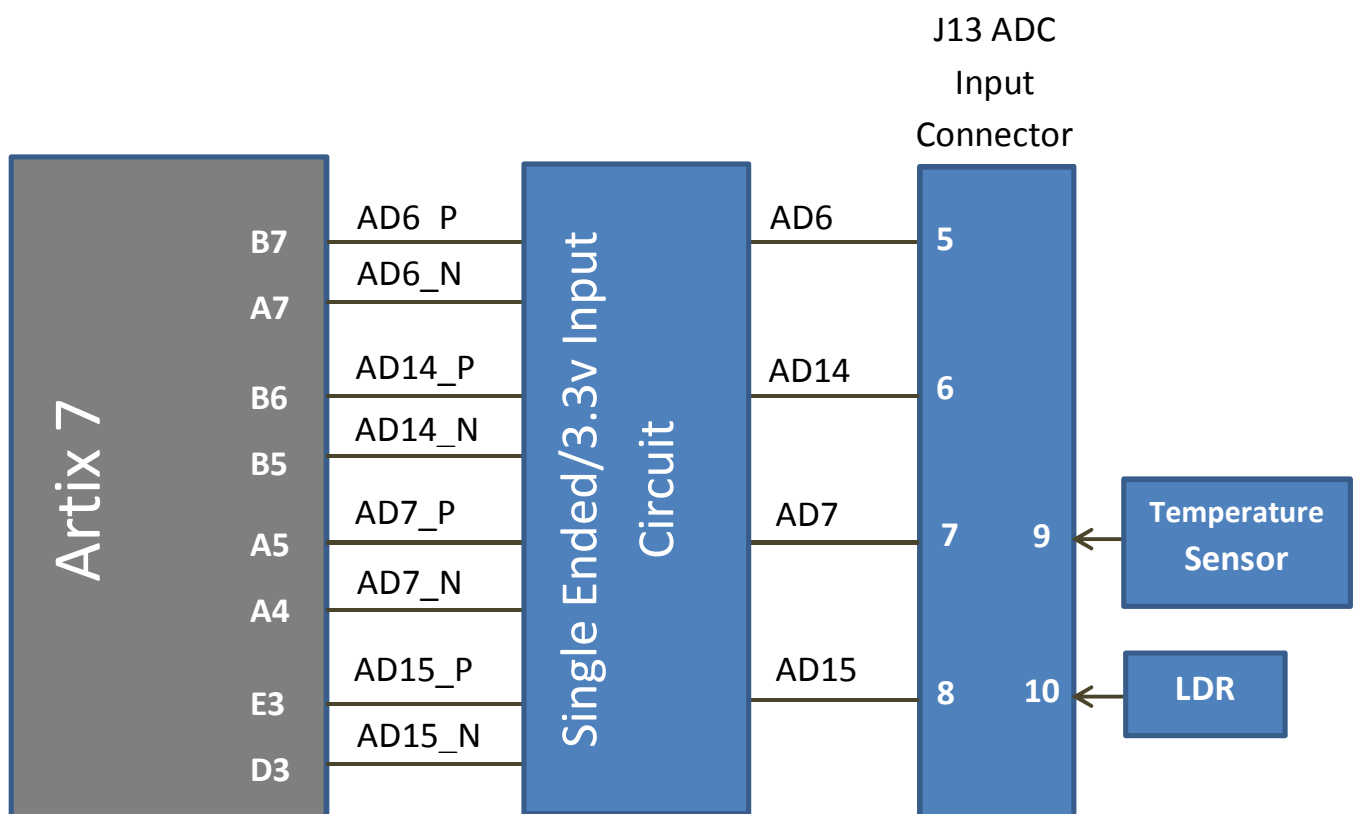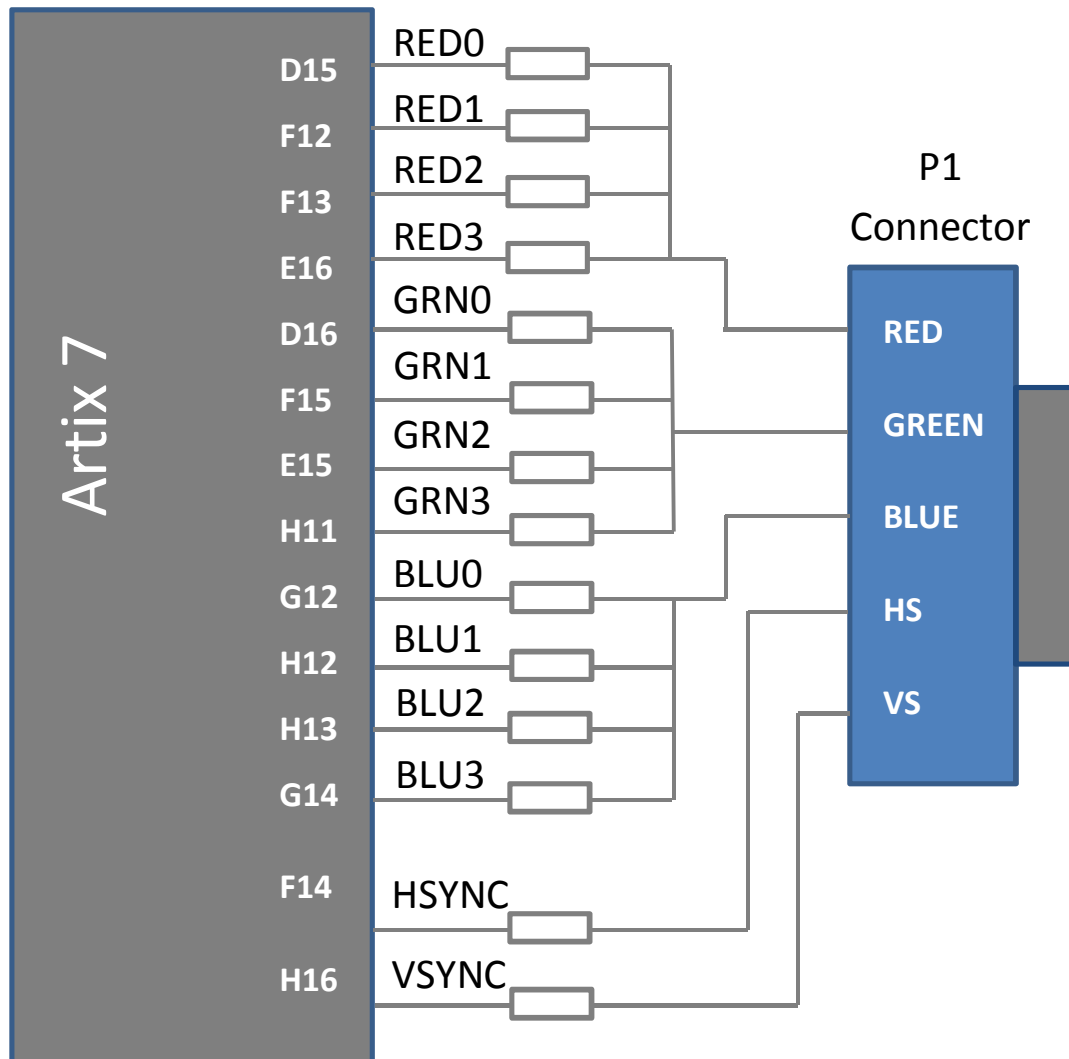
SPI DAC

The EDGE Board consist of Microchip MCP4921 SPI DAC to perform digital to analog conversion. The output is available at the male connector **J13**.

SPI interface provides Serial clock, Data input and chip select to FPGA with DAC. Artix 7 FPGA act as master and MCP4921 act as slave device.
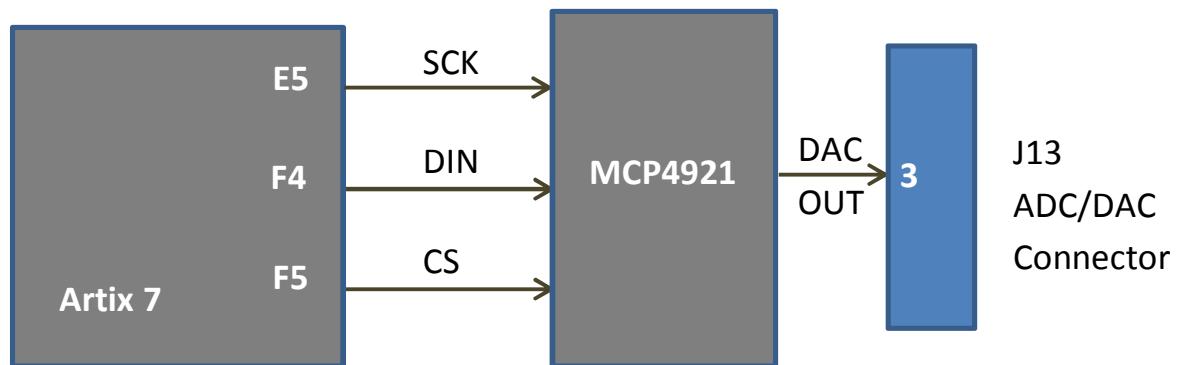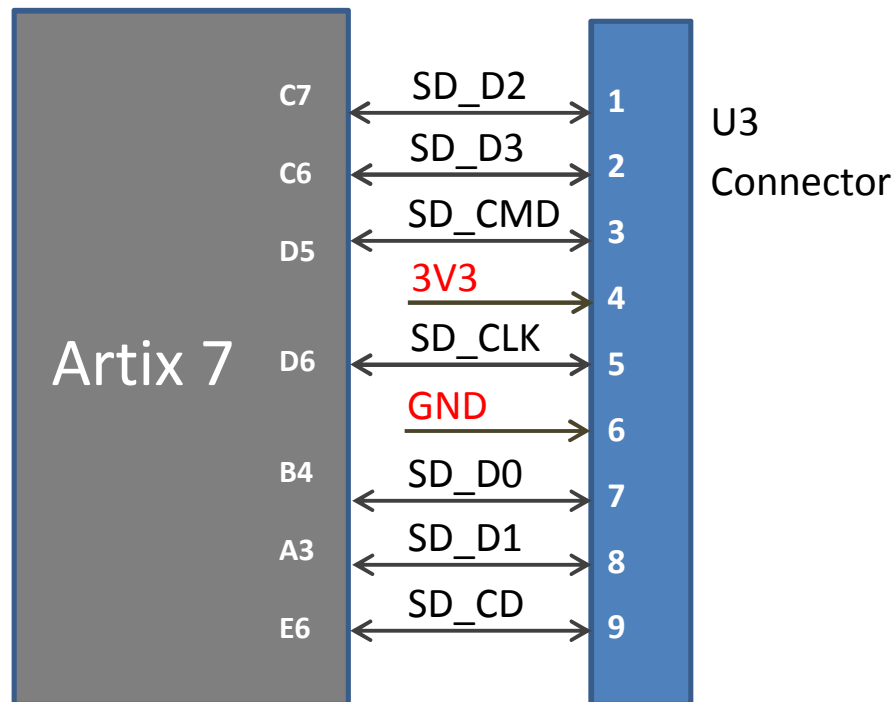
VGA

The EDGE Board contains 12 bit VGA interface to generate VGA signals from FPGA and display the output in the VGA monitor. The 12 bit VGA output the depth of 4096 colours in the Monitor. Series resistors are used to construct DAC to implement VGA interface.

Artix 7		P1 Connector
D15	RED0	
F12	RED1	
F13	RED2	
E16	RED3	RED
D16	GRN0	
F15	GRN1	
E15	GRN2	GREEN
H11	GRN3	
G12	BLU0	BLUE
H12	BLU1	
H13	BLU2	HS
G14	BLU3	
F14	HSYNC	VS
H16	VSYNC	

MicroSD Slot

The EDGE board provides a microSD slot (U3) for non-volatile external memory storage.

| Artix 7		U3 Connector
C7	SD_D2	1
C6	SD_D3	2
D5	SD_CMD	3
	3V3	4
D6	SD_CLK	5
	GND	6
B4	SD_D0	7
A3	SD_D1	8
E6	SD_CD	9

Stereo Jack

Stereo Audio Jack with low pass filter is connected on the FPGA I/O lines on the EDGE Board. Stereo Jack provides delta sigma audio output.

Artix 7		Stereo Jack — J1 Connector
G11	Audio L	
G15	Audio R	
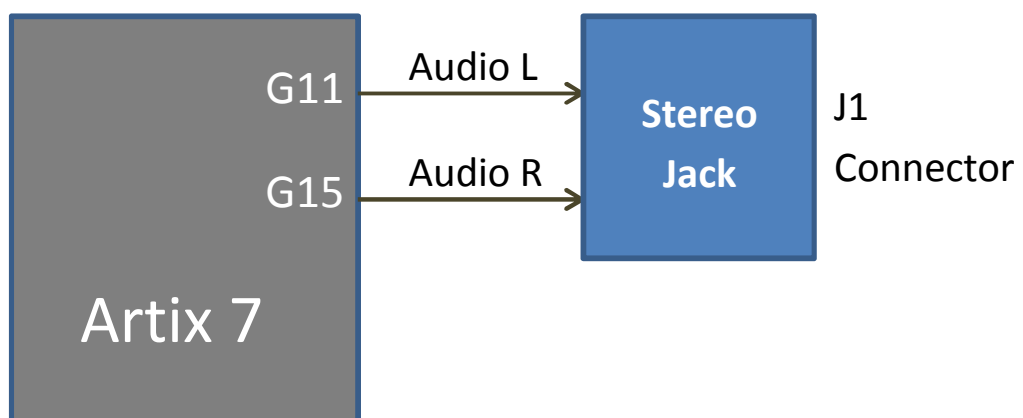
Buzzer

The Edge board contains piezo buzzer interface with FPGA through transistor. 5v Buzzer is used provide alert tone. Buzzer's resonant frequency is 3.8 kHz (where you can expect its best performance).

Note: To enable Buzzer, place jumper at Enable and centre pin of J6. To disable power, place jumper at Disable and centre pin of J12.
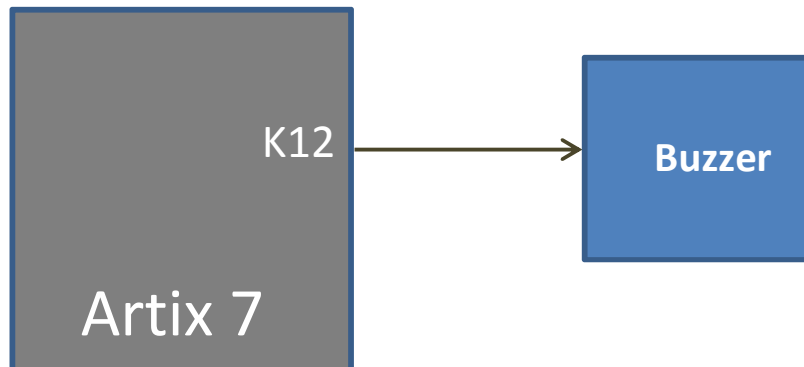

HDMI / DVI

Both HDMI and DVI systems use the same TMDS signaling standard, directly supported by Artix-7 user I/O infrastructure. Only Three differential data channels and one differential clock channel are connected with Artix 7 FPGA. Also, HDMI sources are backward compatible with DVI sinks.
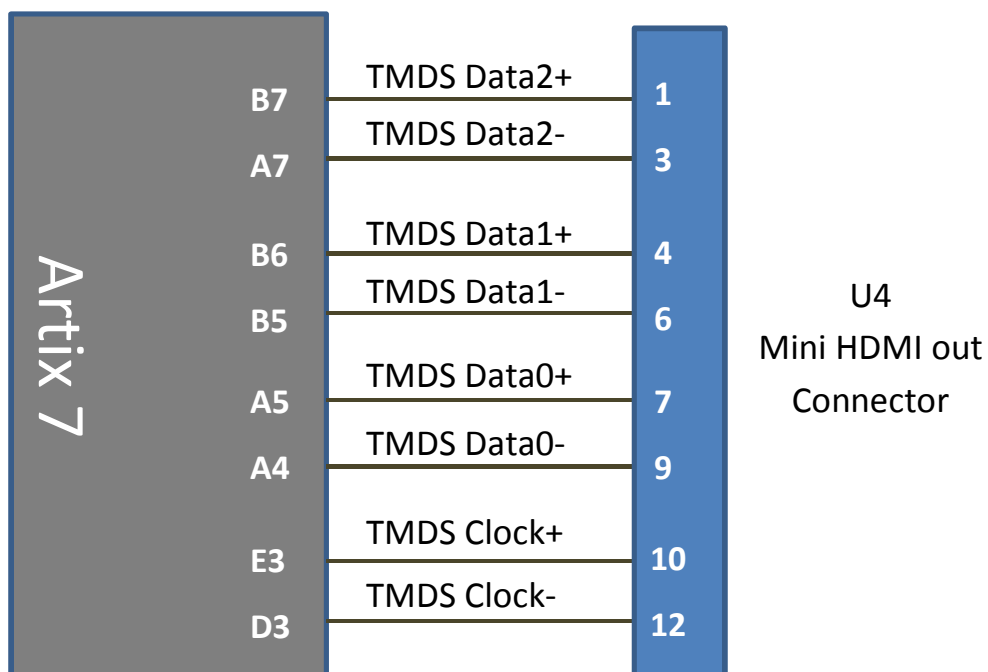
Clock

The Edge board contains 50 MHz Oscillator to provide clock input to the FPGA. The input clock can drive MMCMs or PLL to generate clocks of various frequencies and with known phase relationships that may be needed throughout a design.
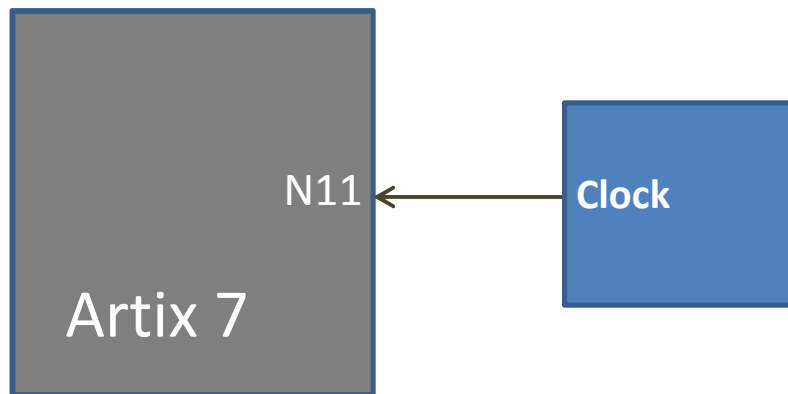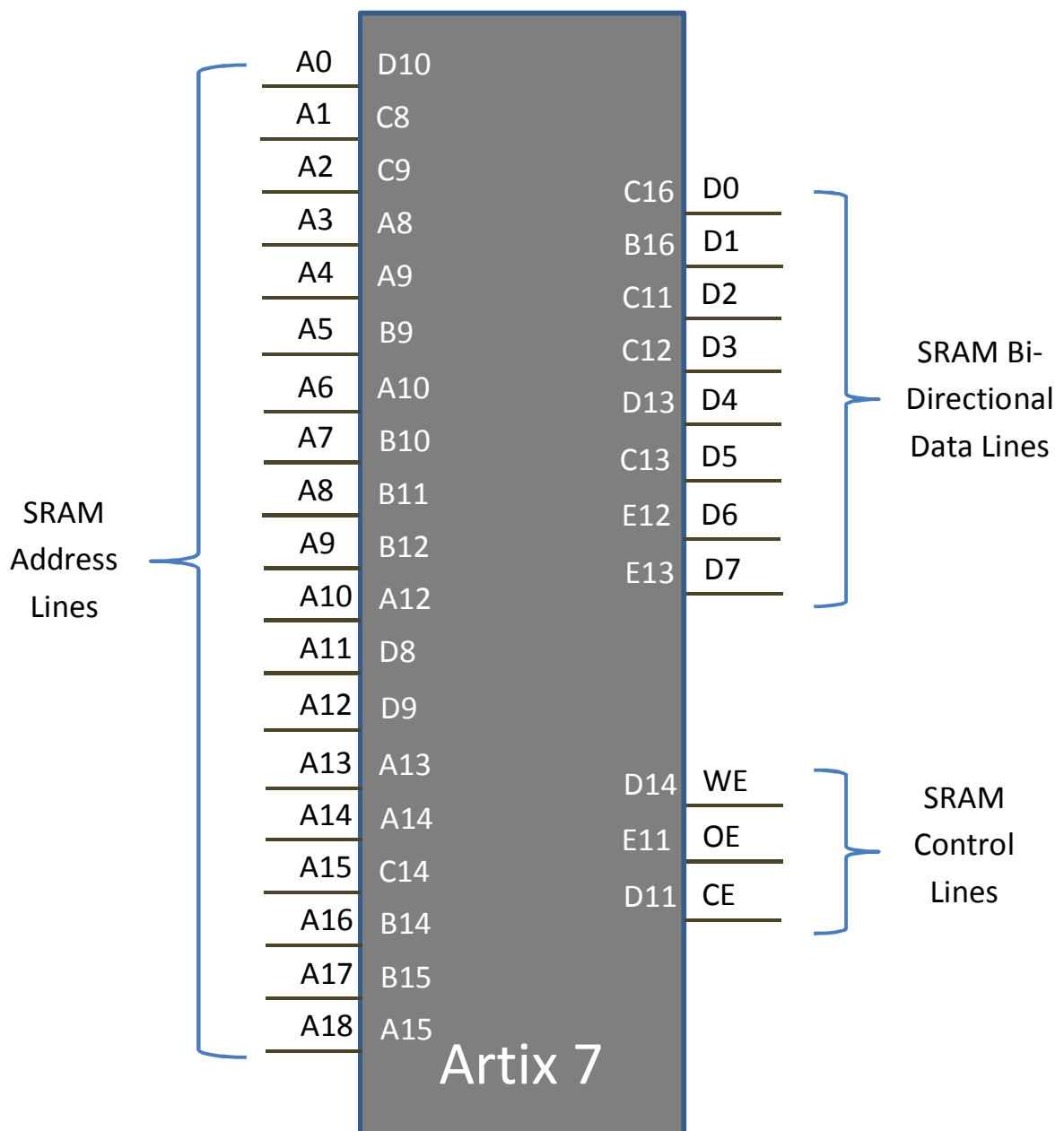

TFT Display

The EDGE Board contains TFT display interface at the J10 connector. TFT display communicates with FPGA through SPI protocol. SPI TFT is made of ST7732S SPI controller with 160x128 Display.
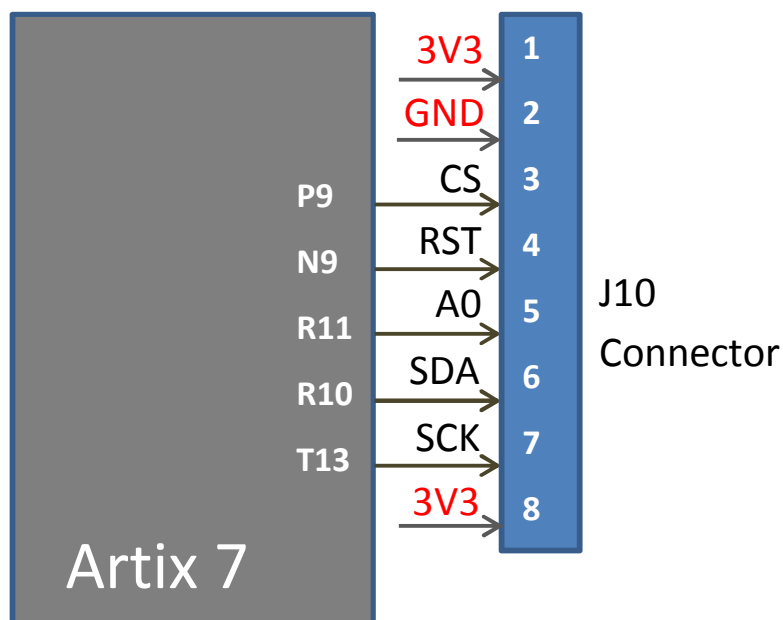
SRAM

The EDGE Board includes 512 KB of Static Random-Access Memory (SRAM). This memory has a standard, easy to use parallel interface with 19 address signals, 8 bi-directional data signals, and 3 control signals. The part used is the ISSI IS61WV5128BLL-10. The interface is fully documented in ISSI's datasheet for the part.
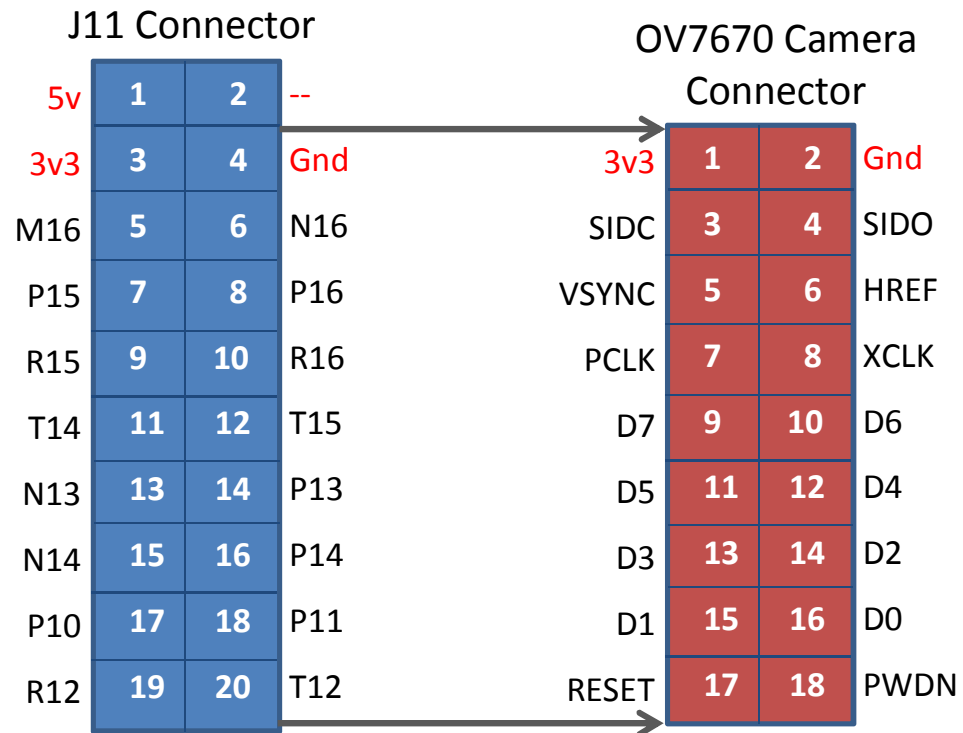
The onboard SRAM is very useful for microblaze designs that would like to provide the processor with additional memory. To do this, the SRAM can be controlled with Xilinx External Memory Controller IP core.

SRAM Address Lines	Artix 7 pin		Artix 7 pin	SRAM Bi-Directional Data Lines
A0	D10			
A1	C8			
A2	C9	C16	D0	
A3	A8	B16	D1	
A4	A9	C11	D2	
A5	B9	C12	D3	
A6	A10	D13	D4	
A7	B10	C13	D5	
A8	B11	E12	D6	
A9	B12	E13	D7	
A10	A12			
A11	D8			
A12	D9			
A13	A13	D14	WE	SRAM Control Lines
A14	A14	E11	OE	
A15	C14	D11	CE	
A16	B14			
A17	B15			
A18	A15			

Artix 7

20 Pin Expansion Connector / CMOS Camera Interface

Expansion connector J11 provides 16 I/O lines from Artix 7 FPGA to the external interface.

Note: To interface OV7670 CMOS Camera with EDGE Board. **Leave pin1 and pin2 unconnected**. Connect pin3 of expansion connector to pin1 of CMOS Camera.

J11 Connector

5v	1	2	--
3v3	3	4	Gnd
M16	5	6	N16
P15	7	8	P16
R15	9	10	R16
T14	11	12	T15
N13	13	14	P13
N14	15	16	P14
P10	17	18	P11
R12	19	20	T12

OV7670 Camera Connector

3v3	1	2	Gnd
SIDC	3	4	SIDO
VSYNC	5	6	HREF
PCLK	7	8	XCLK
D7	9	10	D6
D5	11	12	D4
D3	13	14	D2
D1	15	16	D0
RESET	17	18	PWDN

Driver Installation

Vivado design Suite automatically install drivers for EDGE Artix 7 Board. To verify it, Connect EDGE Artix 7 FPGA Kit to PC through USB cable and Turn On the kit.

Open **device manager** and check the following drivers are installed. **One** USB Serial Port Driver and **TWO** USB Serial Converter Driver as Shown below. Then you can skip driver installation procedure and start working with Configuring FPGA using Vivado.
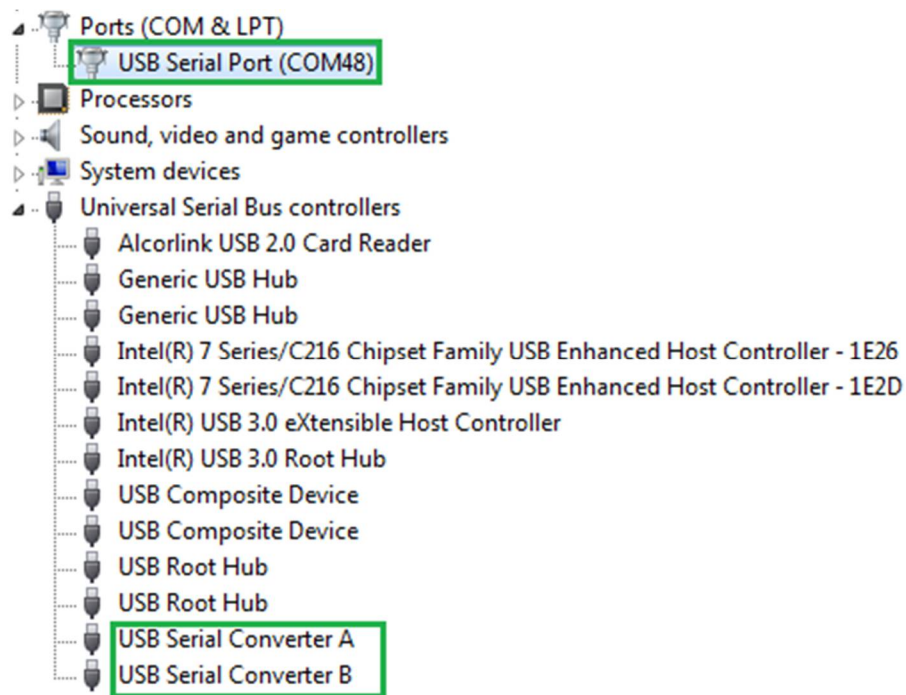
If the drivers are not installed you could see the USB device under Other Devices Category as shown below. Then you have to follow the driver installation steps given below.
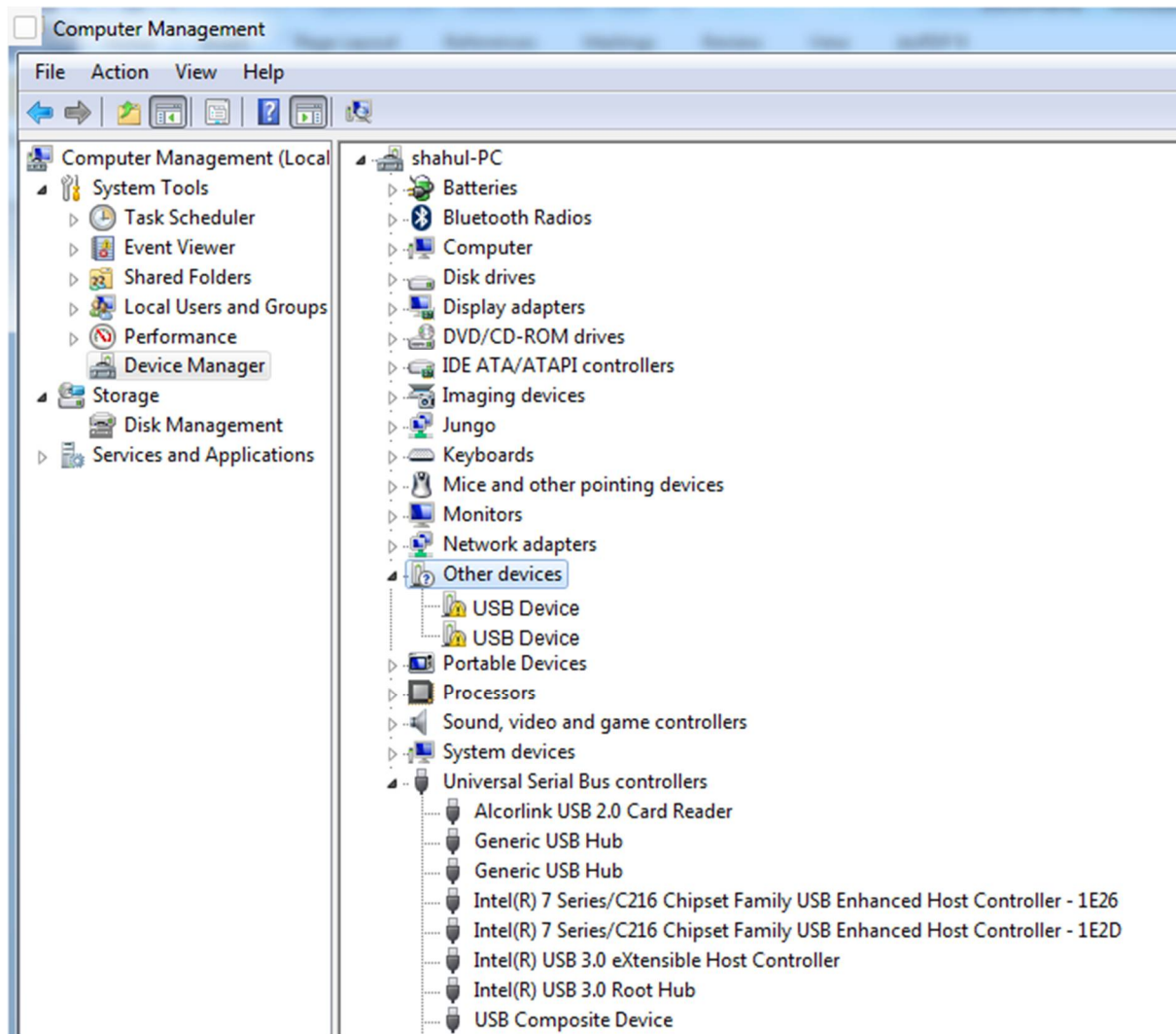
Step1: Download and install virtual com port USB Driver for FTDI Chip.

http://www.ftdichip.com/Drivers/VCP.htm

Step2: Install driver by right click downloaded file and run as **administrator**

Step3: Connect Micro USB cable to FPGA kit **U9 Port** and another end to PC USB Port.

Step4: Open Device Manager. There are 2 other devices detected without drivers as shown in figure.
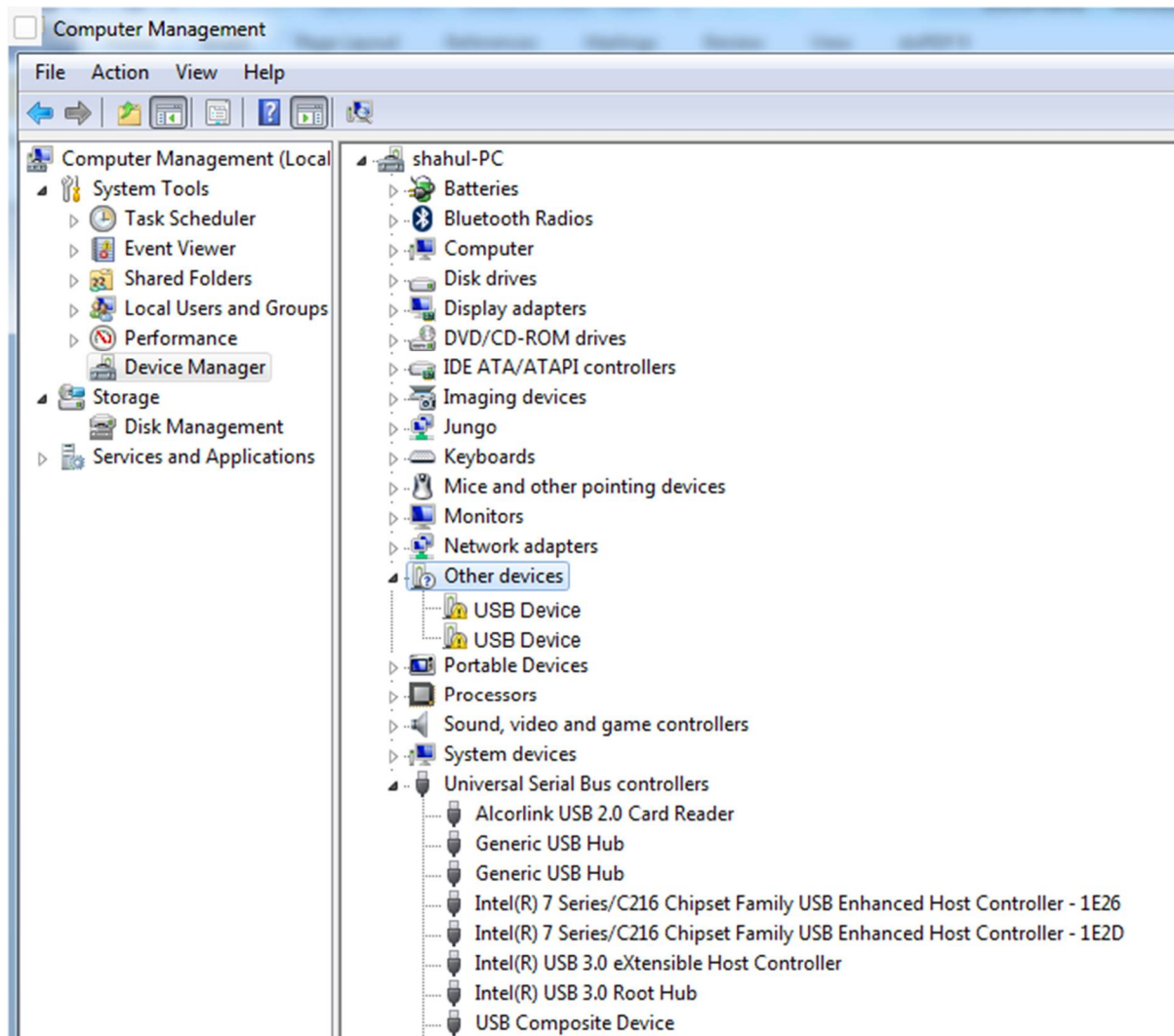
Step5: Right Click on the first USB device and select update driver.

Now select **Browse computer for driver software** and select let me pick from the list of device drivers from my computer as shown below.
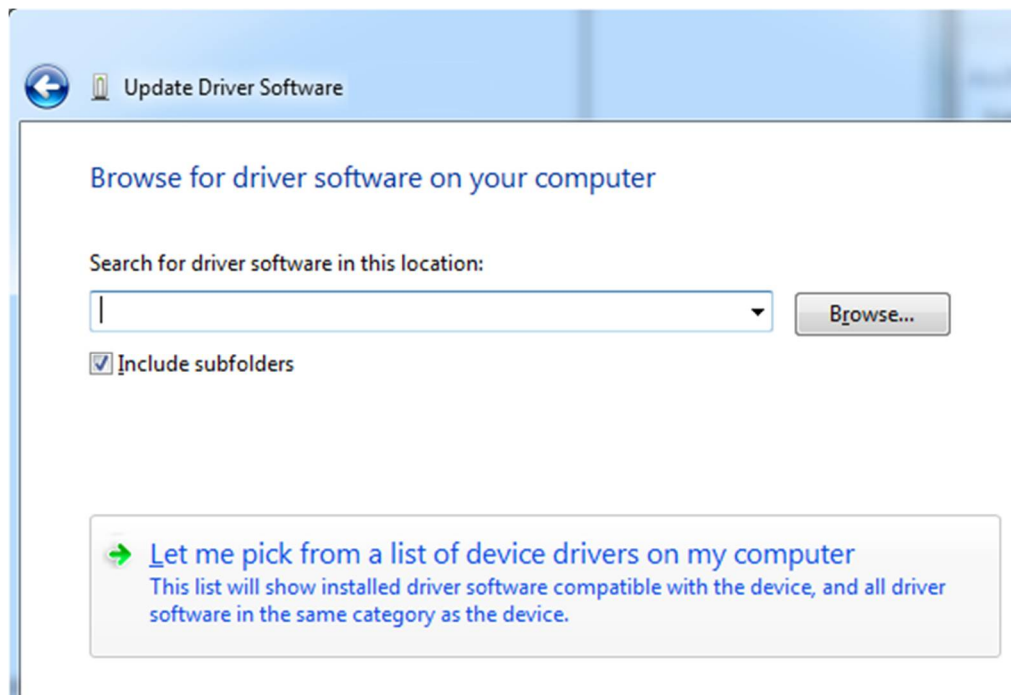
Step6: Now Select USB Serial Bus Controllers and click next.
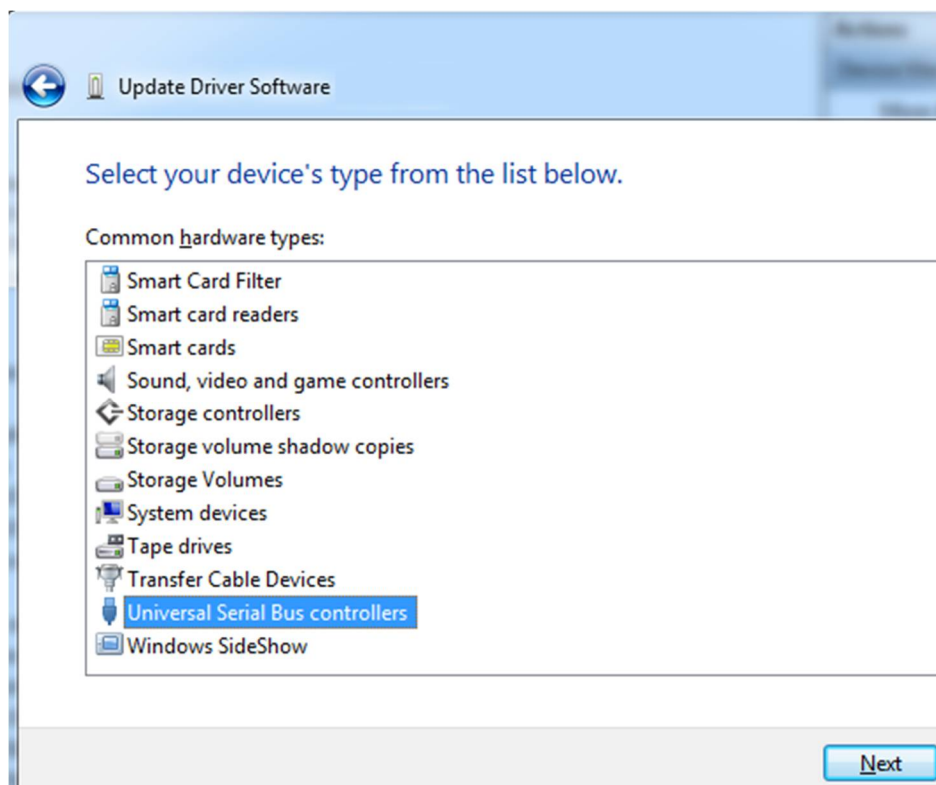
Step7: Select FTDI under manufacturer and select USB Serial converter A under model. (If multiple driver with Serial converter A present select latest version)
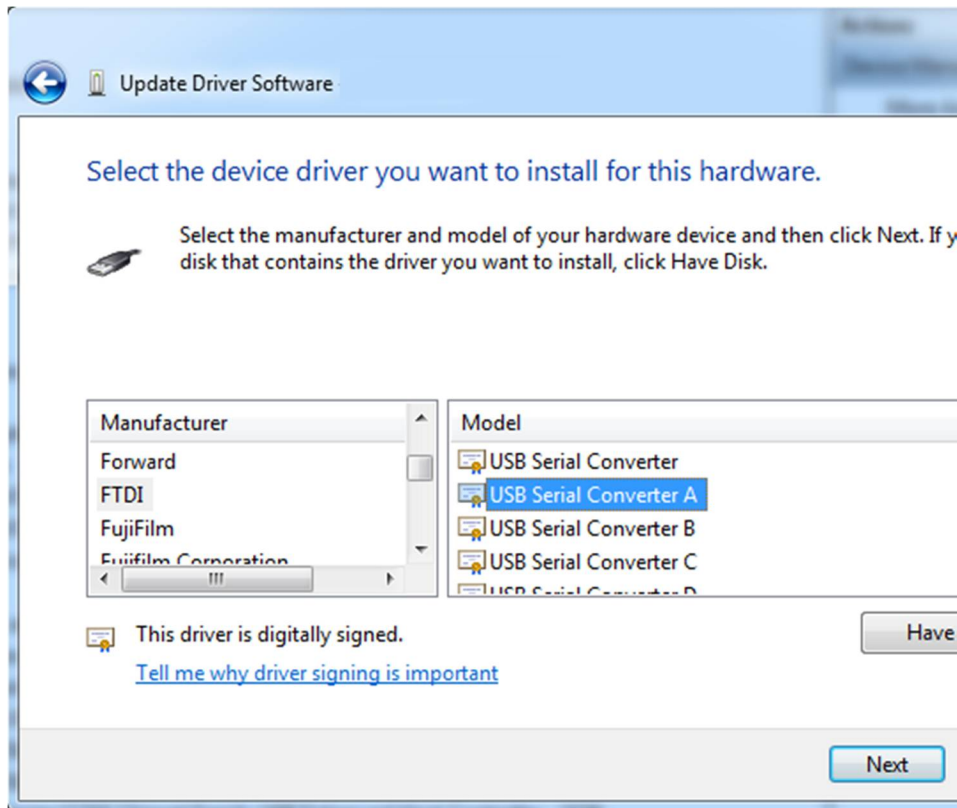
Step8: Repeat step 5 to step 7 for second unknown device. On step 7 select USB Serial Converter B instead A.
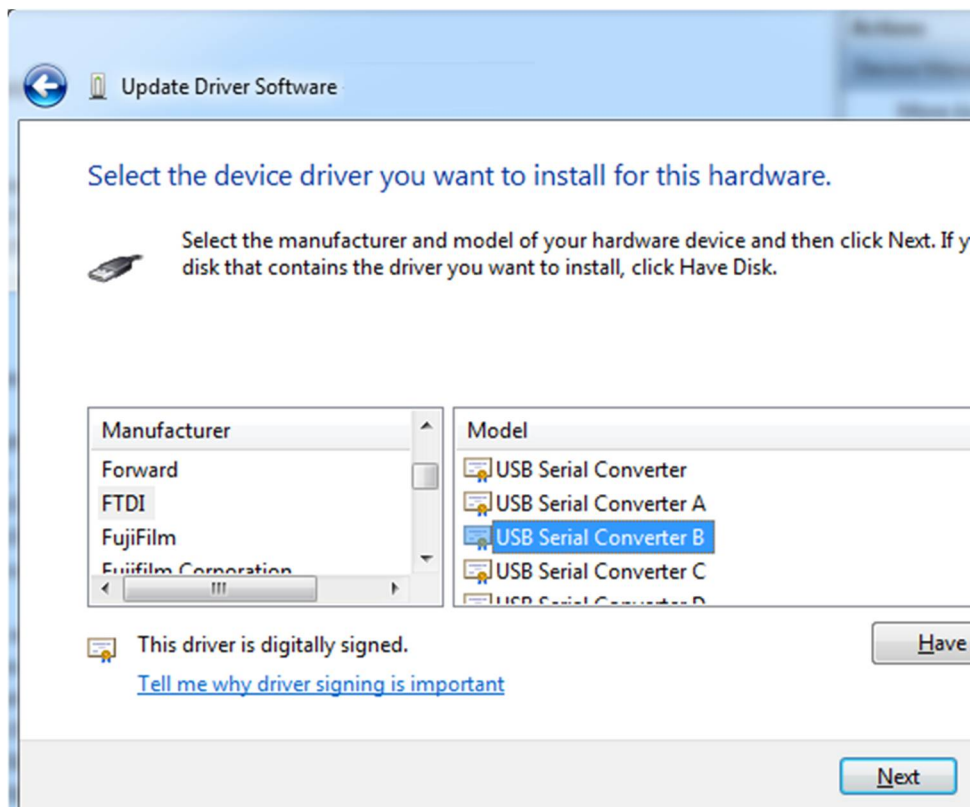
Step9: Now both USB Serial Convertor A and USB Serial Convertor B are detected under USB Controllers. But there another driver needs to be installed for USB Serial Port.
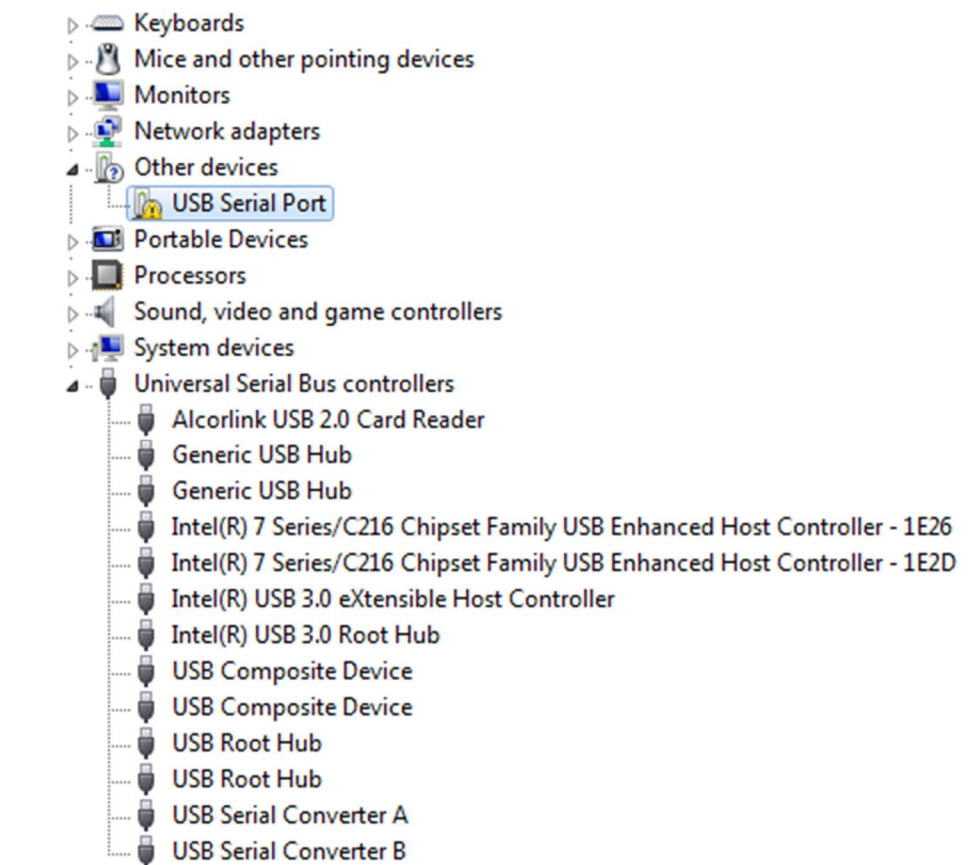
Step10: To install USB Serial Port, Right click and select update drive. Now select **Browse computer for driver software** and select let me pick from the list of device drivers from my computer as shown below.

Step11: Select Ports option and click next.
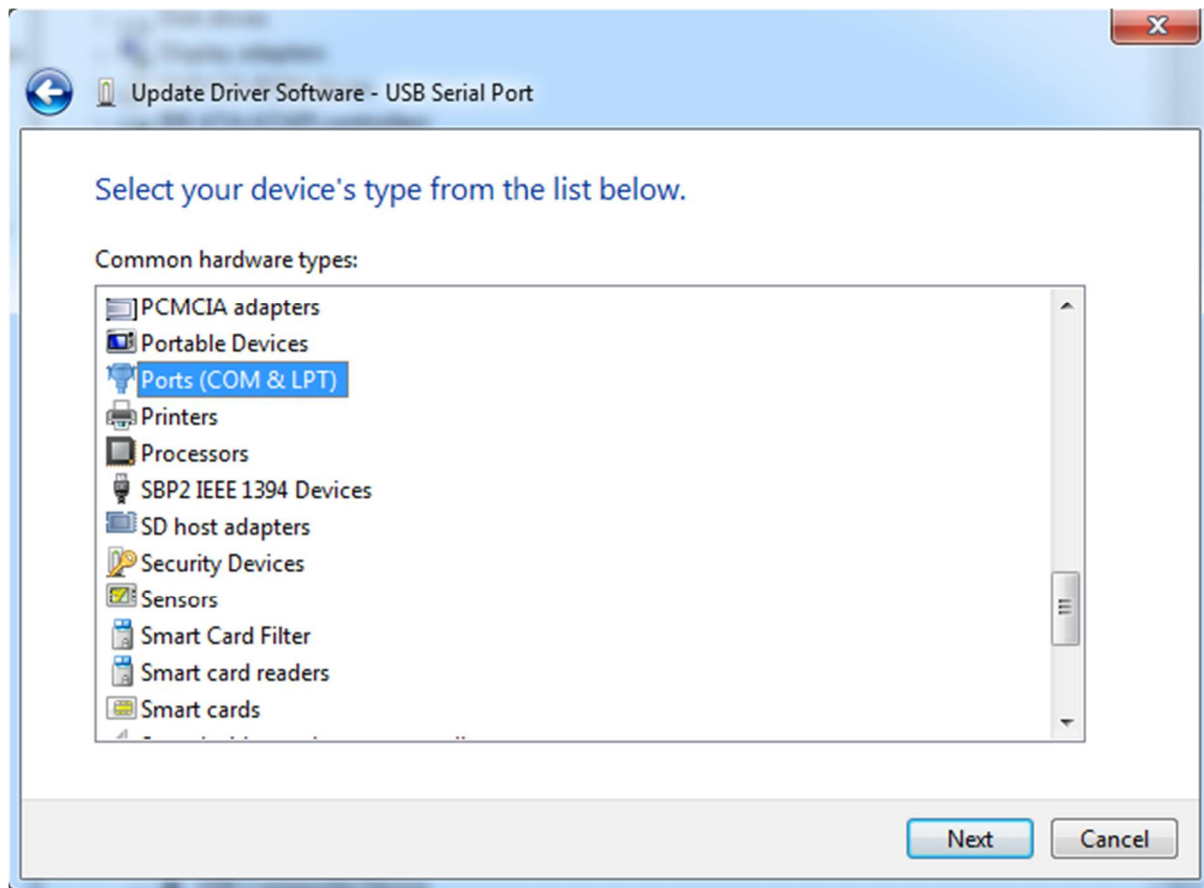
Step12: Select FTDI under manufacturer and Select USB Serial Port under Model.
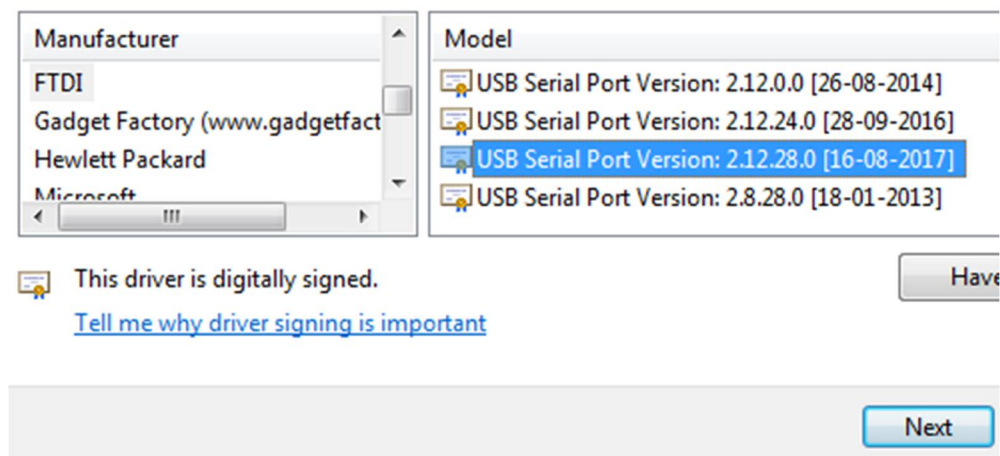
Step13: Now Drivers are installed and devices are detected under Ports and USB Controllers section.
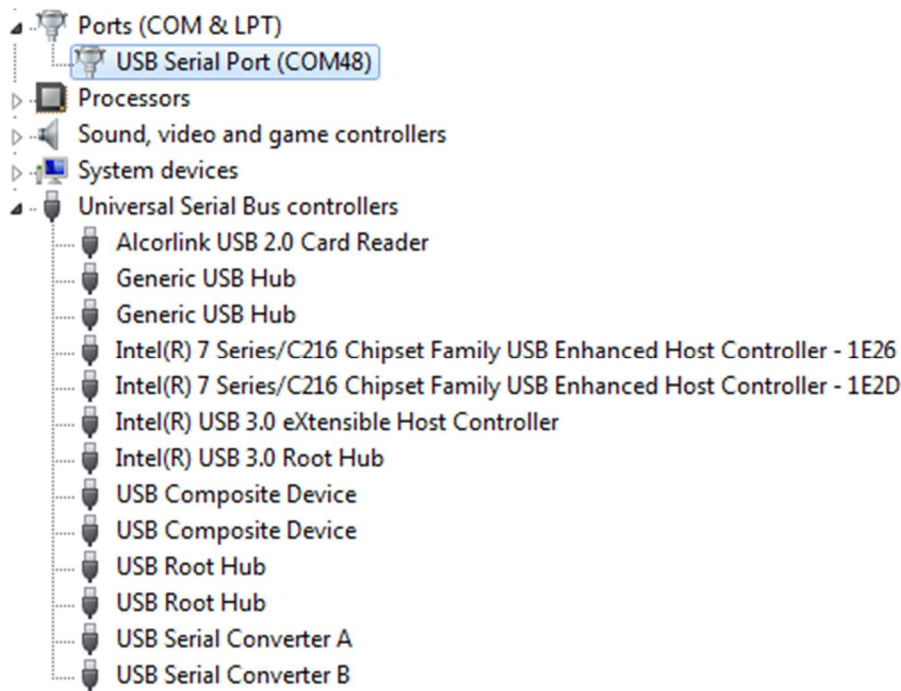
Programming EDGE Board Artix 7 FPGA using Vivado Design Suite

- Connect EDGE Artix 7 FPGA Kit to PC through USB cable and Turn On the kit.
- Open "Hardware Manager -> Open Target -> Auto Connect
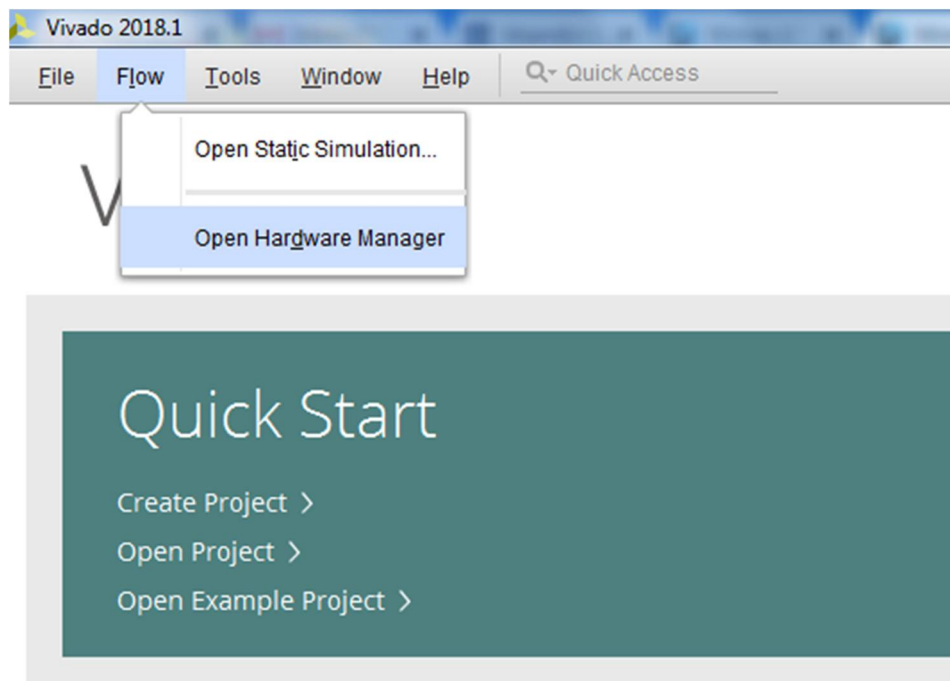
- If the device is detected successfully, then select "Program Device" by right click on the target device "xc7a35t_0" as shown below
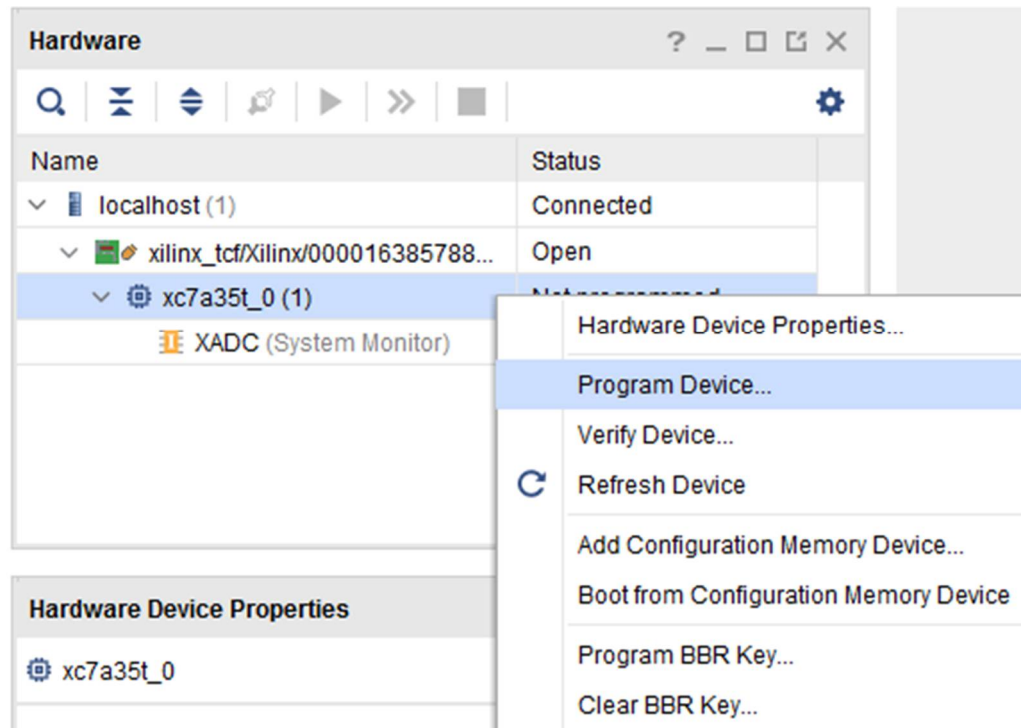
- Browse the Bit file need to be downloaded to the Artix 7 FPGA and click Program.
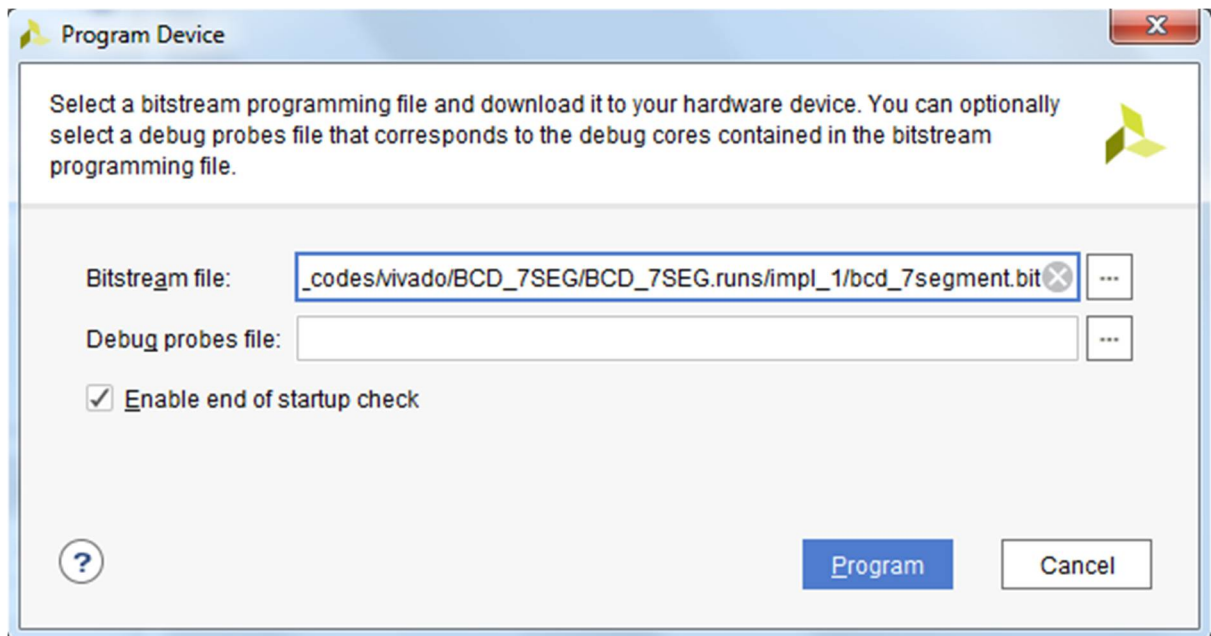
- Once the Program Succeeds, Done LED D1 light up on EDGE Artix 7 FPGA kit.

Programming Quad SPI FLASH Memory using Vivado Design Suite

- Open "Bitstream Settings", check "-bin_file*" checkbox and click OK.
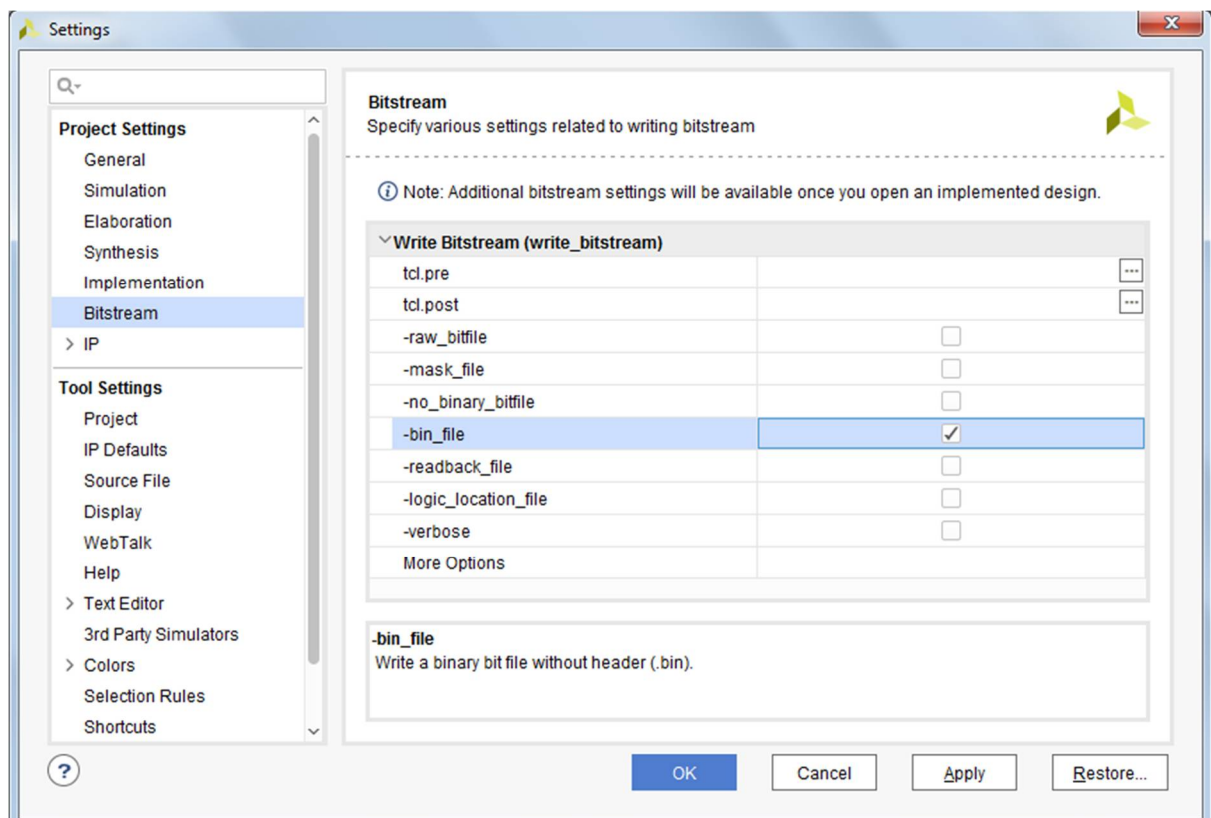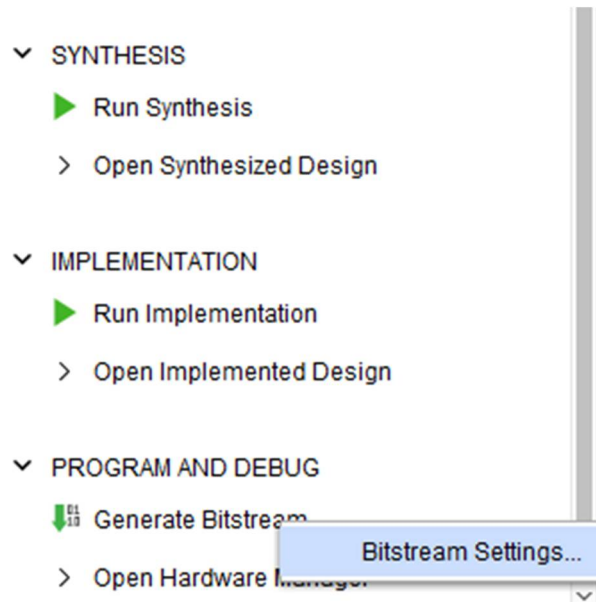
- Click on "Generate Bitstream" to generate your bit and bin file.
- Connect EDGE Artix 7 FPGA Kit to PC through USB cable and Turn On the kit.
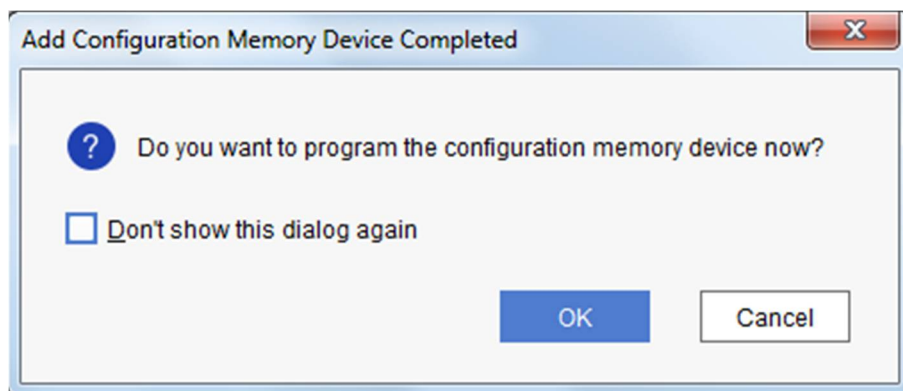- Open "Hardware Manager -> Open Target -> Auto Connect
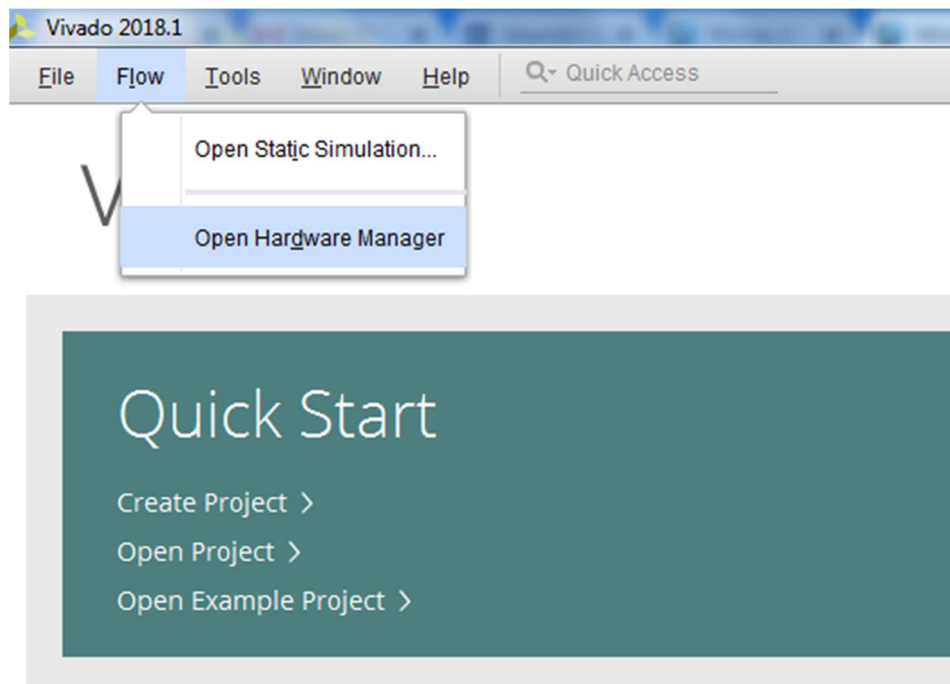
- If the device is detected successfully, then select "Add Configuration Memory Device" by right click on the target device "xc7a35t_0" as shown below.
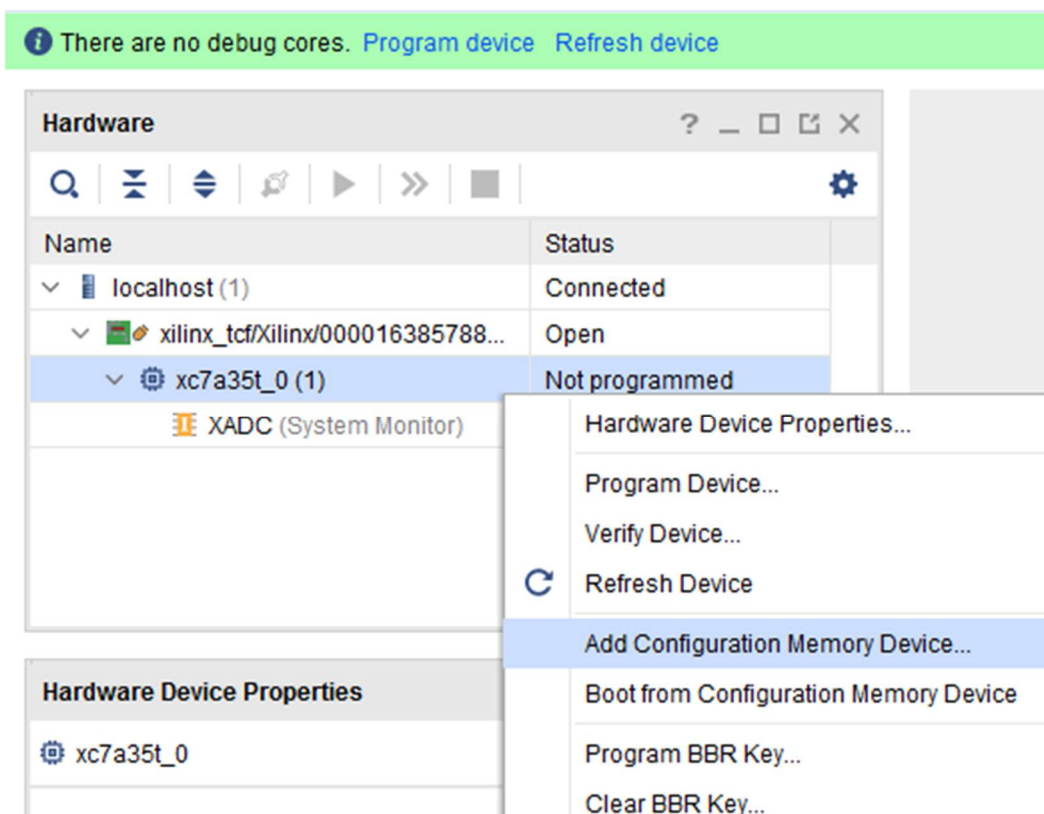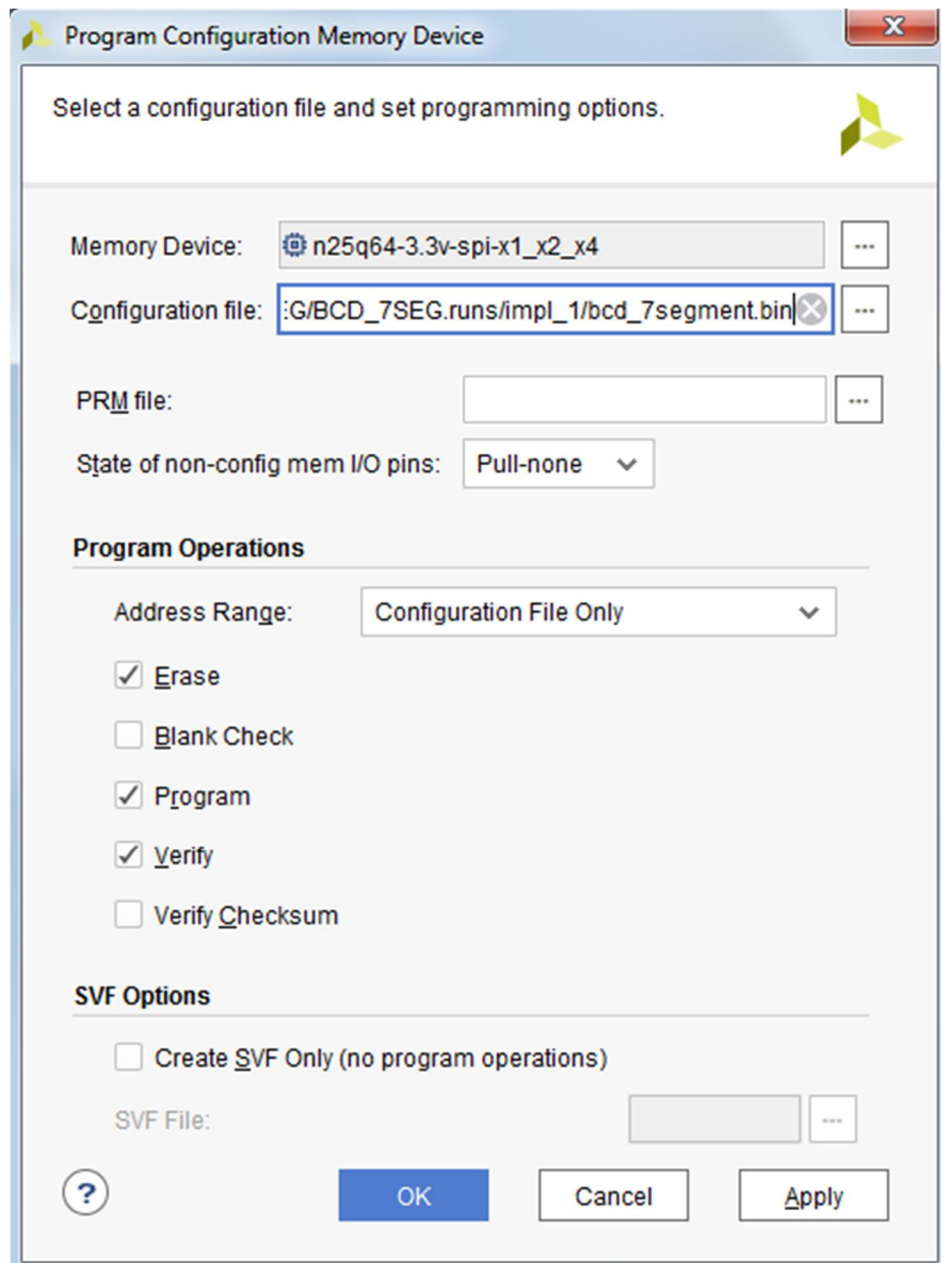
- Select the micron memory device "n25q64-3.3v-spi-x1_x2_x4", then click OK.
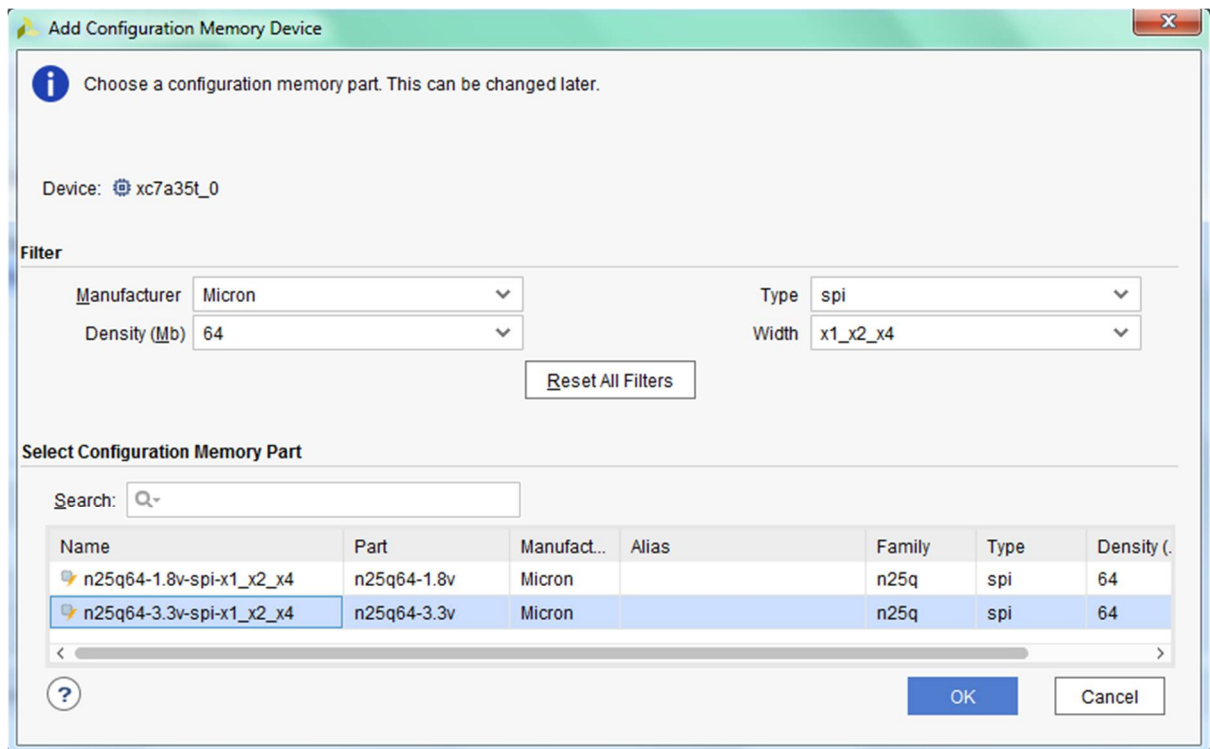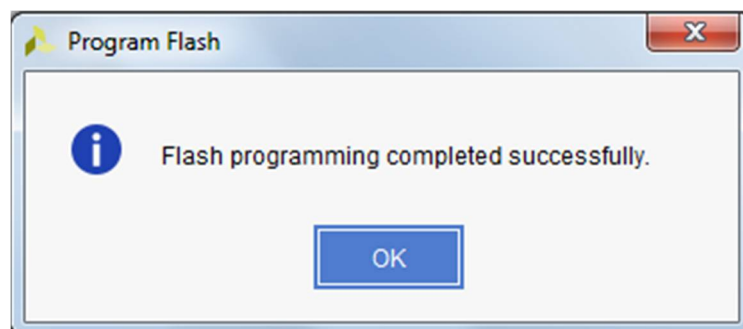

- Now Dialog box open and ask for configuration Memory. Click Ok.

- Browse the bin file to be programmed in the SPI FLASH Memory and click Program,

- Once the Program succeeds the following Dialog Box display the success message.

- To erase the PROM file, untick Program and verify option from Program Configuration Memory Window and click OK as shown in figure.