CHAPTER 1

INTRODUCTION

1.1 BACKGROUND

Frequency filter is a linear electric circuit that has been using in wide area of electronic. The high performance analog active filters have been receiving considerable attention from the last few decades because of its various application and advantages. It has been commonly used in several fields such as communication, measurement,instrumentation, control system and biomedical. Active filter mainly, multifunction or universal filter are more demanding because of its important property that it can be offered several responses by using the same circuit topology.

One of the most critical issues with integrated continuous time filters is the RC time constant variation problem. The RC time constant of the circuit varies due to various factors such as process tolerance, environmental effects of temperature drift, humidity and aging of components. This drawback can be overcome by the use of tunable filter, which have the property of tunability. Therefore, there is growing interest in designing of tunable electronic filters which could compensate the RC time constant variation.

The progress of analog technology has brought forth a large number of electronically tunable filters using different active elements such as operational transconductance amplifier (OTA), current conveyors, second generation current controlled conveyor (CCCII) ,current differencing transconductance amplifier (CDTA), current controlled conveyor differencing transconductance amplifier (CCCDTA), voltage differencing transconductance amplifier(VDTA), voltage differencing differential input buffered amplifier (VD-DIBA), voltage differencing input Buffered amplifier (VDIBA) and voltage differencing Buffered amplifier (VDBA) etc. They are versatile and very powerful building blocks for many signal processing applications due to their high frequency operation, wide dynamic range, current mode operation, high bandwidth and low power consumption.

Recently introduced new active building blocks (ABB) such as VDIBA is providing more flexibility in analog circuit designing. This block is equipped with the tunability feature thought theirtransconductance parameters and, the circuit based over this do not require passive resistor. Apart from this, the circuits based over these blocks occupy lesser area because of their low component count. Additionally, the current mode processing of this block results in simpler circuit structures. Moreover, these devices can be operated in both current and voltage mode thus provides flexibility in circuit designing and results in high performances circuits.

Now a day a several number of trends can be noticed in the area of analog filter design such as reducing the supply voltage of integrated circuit and transition to the current mode.On the other hand, voltage and current mode design still receive considerable attention of many researchers. Therefore, the circuit presented in thesis is realized mainly in voltage mode (VM) and current mode (CM).

Especially, Analog building block that is used in filters namely the universal or multi-function filter can provide several functions form a single topology. Single input, multiple output (SIMO) is most popular analog filter configuration in which various transfer functions can be realized simultaneously. This configuration used in several applications, for example in a phase-locked loop, touch-tone telephone tone decoder and also in the crossover network.

1.2 PROBLEM FORMULATION

Literature reports number of filter structures using various analog building blocks but they lack one or more of the following important features:

(a) Independent control of filter parameters.
(b) Use of less number of active and/or passive elements.
(c) Employs only grounded passive components which are attractive for integration.
(d) Cascadability.
(e) Incompetent of realizing all the five standard filtering functions.
(f) Lesser parasitic effect.
(g) Lesser sensitivity figure.

It is a beneficial to design the active filter such that it uses less number of active and passive components so that area and power consumption could be reduced.

1.3 OBJECTIVE

The main aim of the dissertation is derived from the problem formulation itself. The objective of the dissertation is to realize signal processing circuit which could offer all the aforementioned features in the signal circuit topology using high performance analog building blocks.

As a consequence, the following goals have been formulated for this work:

(a) To design universal filter which implement all filter functions.
(b) Reduction of the active and passive components as far as possible.
(c) To reduce the power and area requirement.
(d) To introduce tunability in all the filter parameters.
(e) To minimize parasitic effects to enhance the Bandwidth.
(f) To ensure cascadabilty.

1.4 REPORT ORGANIZATION

The report is organized as follows:

Chapter 1 includes introduction, problem formulation and objective of the work.

Chapter 2 includes a literature survey which explains the work that has already been done by various authors in the context of filter designing goals such as the number of filter functions number of active and passive components, tunability.

Chapter 3 deals with the explanation of newly introduced active element VDIBA with the design consideration needed to make an analog filter.

Chapter 4 includes the various simulation results of different filter at 180nm technology.

Chapter 5 about analysis of mixed mode biquad filter.

Chapter 6 presents the overall conclusion of the work and future aspects related to it. The conclusion provides the summarized view of the complete thesis and the future scope provides the pathway for later scholars to research in the same field.

CHAPTER 2

LITERATURE REVIEW

2.1 LITERATURE SURVEY

This phase will include study of basics of the topics and papers already published in different journals.

K. L. Pushkar et.al, 2011 [1] presented independent tunable VM biquad filter. The circuit employs new active element VDIBA which consisting of two capacitors and a one resistor only. The configuration can realize all the filter functions with the same circuit topology with three inputs and one output. The circuit does not require matching condition and inverting input. But, the circuit uses floating passive components which are not suitable for integration.

Norbert Herencscar et.al, 2013 [2] presented a new resistorless tunable voltage mode universal filter which uses a single VDIBA. The angular frequency can be tuned through the transconductance of VDIBA. The active and passive components have low sensitivity and no constraint matching condition is required. However, the circuit does not provide independent electronic control. Also, the circuit employs floating capacitor, which as previously quoted is less attractive for integration.

Jetsdapornsatasup et.al, 2013 [3] presented a voltage mode universal filter that can be electronically tunable. The circuit is having a single input five output and employs two VDTA, two resistors and two capacitors only. It provides independent electronic control of natural angular frequency and quality factor, but uses a large number of passive and active components.

Abdullah Yesil et.al, 2011 [4] described RF filter using a VDTA. The circuit employs a single VDTA and only two capacitors to realize low pass, high pass, and band pass filter. However, it fails to provide orthogonal tuning between the pole frequency and quality factor.

Dinesh Prasad et.al, 2013 [5] presented a current mode biquad filter using a VDTA. The configuration realizes entire filter functions. However, the circuit is not able to provide

orthogonal tuning. Also, the circuit requires inverting voltage input to realize all pass and band stop filtering function.

JetsdapornSatansup et.al, 2014 [6] presented a compact CM universal filter. It has three inputs and a single output. The circuit employs one VDTA and two grounded capacitor. It can realize all the filter functions with electronic control of the natural angular frequency and quality factor.

WilasNinsraku et.al, 2014 [7] presented a VM biquadratic filter using VD-DIBA. The filter configuration employs two VD-DIBA and two grounded capacitors only. All the functions such as LP, HP, BP, notch and AP has been realized by the same configuration and do not requires any external passive resistor. It does not require any inverting input to realize any filter functions. In addition to, the circuit enables simple cascading in voltage-mode due to having of proper high and low impedances at their respective input and output ports. But, it fails to provide the orthogonal tunability between pole frequency and quality factor.

Norbert Herencscar et.al, 2009 [8] realized a novel second order multifunction biquadratic filter. The circuit is versatile bcause it can be operated in CM as well as in VM. The circuit uses single current conveyor transconductance amplifier (CCTA), two capacitors, and two resistors. By using the adjoint transformation method, the VM filter can be transformed into a CM filter. The circuit can realize LP, BP, HP, BS and AP filter functions by using the same configuration and also provide independent control of the quality factor Q. No matching condition is required and exhibit low sensitivity. However, the circuit does not provide orthogonal tuning and also uses floating capacitor which is not beneficial for monolithic integration.

Suwat Maneewan et.al, 2014 [9] presented a novel voltage-mode first order all pass (AP) filter consists of single VDTA and a single capacitor. There are many advantages of the circuit such that it uses very less component, the phase shift of the circuit can be altered by the bias current, does not require any matching constraint conditions and the THD of the output signal is very low. The drawback of the circuit is that it fails to provide independent tuning as well as uses floating capacitor which are not appropriate for monolithic integration. Also, the circuit has higher sensitivities. At 1.25V power supplies, the maximum power consumption of the circuit found to be 400µW.

Norbert Herencscar et.al, 2013 [10] has designed a resistorless dual output VM AP filter. The filter circuit uses a single VDIBA and one capacitor onlythe filter enjoys orthogonally between the natural frequency and quality factor. However, the circuit does not need component matching conditions and having low sensitivity. The disadvantage of the circuit is that it uses floating capacitor which is not appropriate for integration. Also, the circuit does not provide orthogonal tuning.

Jaroslavkoton et.al, 2014 [11] focused on the application possibilities of the newly presented active building block named as voltage differencing differential difference amplifier (VDDDA). A multifunction frequency filter is designed by using this active element, which provides the possibility of mutually independent control of the quality factor

and a characteristic frequency. The structure of the filter is designed by using theidea of the Akerberg-Mossberg (AM) filter. AM filter suggests that the integrators are always realized only by two active elements which result in better phase compensation for the filter. The proposed structure features high-impedance inputs, low impedance output, and all basic frequency responses.

Yan-Hui Xi et.al, 2008 [12] designed a two new circuits by using the intrinsic properties of a novel trans linear CMOS CCCII. First one is CM second-order universal filter and second one is new active simulated inductance. Both circuits offer the advantageous features such that they do not require an external resistor which is suitable for IC technologies and also provide electronical tunability. Moreover, they use less number of active and passive elements.

Chang and Lee et.al, 1999 [13] designed VM filter with a single input and three outputs and it consists of two current conveyors, two capacitors which are grounded, and three external resistors. The circuit offers the following advantageous features such as realization of VM LP, BP, and HP filter responses without changing the configuration, does not require the constraint matching conditions, uses grounded capacitors that are beneficial for integration technologies and having low sensitivity figures But, the circuit fails to provide orthogonal tuning.

Jinn Wei Horng et.al, 2011 [14] realized CM and VM multifunction filters using current feedback amplifiers (CFAs). The VM circuit can realize simultaneously LP and BP filters only. The CM circuit exhibit simultaneously low pass, band pass and high pass filters. The circuit offers following features such as low sensitivity characteristics, employment of only grounded capacitors, no requirement of matching conditions and also has the ability to realize all the filter function from the same circuit configuration.

Nissar Ahmad shah et.al, 2006 [15] presented a mixed-mode multifunction filter. The configuration is employing three FTFNs and only five passive components. The circuit has a single input and three different outputs. The configuration can be driven by a voltage as well as by a current source while as outputs are always in voltages and currents form, thus the circuit can realize filtering functions in mixed-mode as well as normal-mode. Besides having small active and passive sensitivities, the parameters like resonance frequency (ω_o) and bandwidth (ω_o/Q) enjoy orthogonal tuning.

Manish Kumar et.al, 2010 [16] presented multifunction filter which realizes low-pass, high-pass, band-pass and notch filter. The configuration employing two current conveyors have a balanced output, four resistors and two capacitors. The circuit implements a number of filter function at the single output terminal using two current conveyors. In addition of this proposed circuit does not require any matching constraint/cancellation condition. The circuit employs grounded capacitor that is suitable for IC fabrication. The circuit enjoys the orthogonality between the cutoff frequency and the bandwidth. It has a low sensitivities figure for both active and passive components.

Nissar Ahmad shah et.al, 2007 [17] described a new transadmittance mode (TM) universal filter. The circuit employs only two CDTAs, two capacitors in which one is grounded while another one is floating and as many resistors with three inputs and a single output. All the filter function such as LP, HP, BP, notch and AP functions can realize simultaneously without changing the configuration. The circuit enjoys an independent electronic control of angular frequency (ω_o) and bandwidth (ω_o/Q). The circuits possess low sensitivity for both active and passive components.

Nissar Ahmad shah et.al, 2005 [18] presented a new filter topology employs a single operational amplifier (OA), one capacitor, and two resistors. The circuit can simultaneously realize LP and BP transadmittance function. The input impedance of the proposed filter is very high that is essential for cascading with no use of buffers. The filter uses a pole - model of OA, thus provide suitability to extend frequency operation. The circuit provides orthogonal tuning for pole frequency (ω_o) and quality factor (Q). The configuration uses less number of components and possesses low sensitivity.

C.M. Chang et.al, 2004 [19] discussed a new biquad filter model based on nullators, narrators, current mirrors and passive C (capacitor) and R (resistor) elements. Two implementations of biquad filter model have been proposed by using CCCIIs and OTA. These two biquad implementations realize all the important filter functions simultaneously, including universal filtering, less component count and independent control of pole frequency (ω_o) and bandwidth (ω_o/Q).

Alain Fabre et.al, 1996 [20] introduced two configurations for 2nd order current mode. These circuits exhibit low values for their active and passive sensitivities. Due to having zero input impedance they are easily cascadable. Two voltage-mode implementations are then deducted from them. Depending on the passive components used, the circuit will be either a 2nd order or a 3rd order filter. The VM, as well as the CM implementations are characterized by easily modifiable transfer functions, without affecting ω_o and Q.

Nikhil Raj et.al, 2010 [21] introduced OTA which operates in sub threshold (weak inversion) region thus able to provide a versatile solution for the realization of low power VLSI building blocks. This paper demonstrates a modified OTA which is developed by using a high swing improved-Wilson current mirror. The circuit can provide high linearity and better performance, thus suitable for low power and low-frequency applications. The achieved linearity and unity gain bandwidth (UGB) is ±1.9V and342.30KHz respectively. The OTA is operated at the power supply of 0.9V and consumes very less power in the range of few Nano watts.

FıratKacar et.al, 2012 [22] presented a new biquad filter circuit using an active element, namely VDBA. This block has low impedance output terminal and high impedance input terminals which provided advantages to VM circuits. Due to having of transconductance gain in VDBA, the proposed circuits can be designed without using any external resistors. Two new VM biquad filter configurations have been presented in this paper. Two active elements and two or three passive components have been used by both filters. They can realize voltage mode LP, BP, HP, BS and AP filter functions. The biquad

filters have low output impedances that are necessary for cascadability for voltage mode circuits and do not require any critical component matching conditions. For the second biquad, the quality factor can be adjusted by a resistor independently to provide tuning.

Jinn Wei Horn et.al, 2004 [23] presented a four-inputs and two-outputs VM multifunction biquad filter employing only two OTA and two capacitors. The new circuit offers several advantages, such as employs a minimum number of active and passive components i.e. two OTAs and two capacitors only, realization of HP, BP, LP, notch and AP responses from the same configuration, high input impedance and also employs only grounded capacitors for band pass and low pass filter realizations. There is an availability of one or more simultaneously output filter response and exhibit low sensitivity.

Milad Razzaghpour et.al, 2008 [24] presented a 0.5V ultra-low-power, improved OTA using the transistors which operate in weak inversion. This circuit is basically based on a bulk-driven input differential pair and uses again-stage in the Miller capacitor feedback path so that "pole-splitting"effect improves. The result shows the enhancement in unity-gain bandwidth and also DC gain with the power consumption of only 1.02μW.

Chunhua Wang et.al, 2008 [25] introduced a new CM single-input multiple- output type universal filter using non-inverting and inverting CCCII which is controlled by current. The circuit employs four CCCII and two grounded capacitors, and it can simultaneously realize LP, BP, HP, BR and AP functions. The circuit provides the mutually independent control of the quality factor and a pole frequency by means of setting the bias current of the CCCII. The parameter sensitivities are very low. Moreover, a high Q-value filter can be easily achieved by adjusting the ratio of two bias currents.

Nattapong Tongan et.al, 2009 [26] introduced circuit that can work as either a quadrature oscillator or a universal biquad filter with the same circuit topology. When the circuit works as quadrature oscillator, both the oscillation frequency and oscillation condition can be adjusted separately by the input bias currents. On the other hand, when the circuit works as a universal biquad filter, the pole frequency and quality factor can be tuned orthogonally by the input bias currents. The circuit description is very simple, employing of four CCCIIs and two grounded capacitors. The circuit does not use external resistors and employs only grounded elements, and thereby makes it attractive for IC architecture.

Muhammed A. Ibrahim et.al, 2008 [27] realized a universal filter based on dual output operational transconductance amplifiers (DOOTAs) working in mixed-mode, i.e., all the four modes such as voltage-mode(VM), current-mode(CM), transimpedance-mode (TIM) and transadmittance-mode(TAM). In these modes, the filter realizes all the basic filter functions simultaneously. The simulation results of the circuit have been confirmed by a P-SPICE simulation program using real device parameters.

LiZhijun et.al, 2009 [28] presented a novel mixed mode biquad filter based on MCCCIIs (multiple output current controlled conveyors). The filter structure using MCCCIIs(5), capacitors (2 that are grounded) and can realize LP,HP,BP filter functions

simultaneously from the same topology. The circuit can be operated either by the voltage or by the current and its output can be taken out as voltage or current. The pole frequency and quality factor can be tuned independently by changing the bias currents of MCCCIIs. To confirm the functionality of the proposed circuit, it is simulated using real device parameter.

Nadhmia Bouaziz ElFeki et.al, 2009 [29] introduced a high bandwidth and high performance analog building block i.e. second generation (CCII±) and third generation (CCIII±) current conveyors having dual output. Both the circuit provides large range of voltage and current bandwidths. At port X, Y and Z of the circuit have controllable intrinsic resistances. For optimal sizing to improve static and dynamic performance the optimization program has developed by using heuristic methodology. The current and voltage bandwidths are calculated as 1.5806GHz and 6.506GHz respectively, and input port resistance(R)for the bias current of 100μA is obtained as 454.11ohms. It is a very useful building block widely used in an analog circuit for designing of filter based circuits, specifically when the application requires dual output. The Voltage supply is required by the circuitis ±2.5V with very low power consumption. The paper also presented a filter configuration having multi-input multi-output. In the current-mode, only the LP and BP filter responses can realize from the same configuration. The cut of frequency of the LP filter obtained as 1.64GHz and the frequency of the bandpass filter has been obtained as 1.13GHz. The functionality of the circuit has been verified by the PSPICE simulations at CMOS 0.35μm technology.

Jiunwei Horng, 2004 [30] presented a VM universal filter having four-inputs and two-output. The configuration employs only two OTAs and two capacitor that can offer several advantages, such as using less number of spread (two OTAs and two capacitors), able to realize all the function i.e. HP, BP, LP, notch and AP from the same configuration, and for BP and LP filter realization uses grounded capacitor. The filter is able to realize one or more output filter response simultaneously and also the sensitivity of the component is less.

Sajai Vir Singh et.al, 2011 [31] presented an electronically tunable CM and VM universal biquad filter using active element i.e. CCCCTAs stands for current controlled current conveyor transconductance amplifiers. The circuit realizes only LP, BP and HP responses simultaneously while the realizations of BR and AP responses are also feasible from this configuration. The circuit configuration is versatile because it can work in mixed mode as well as in normal mode. The filter can provide the independent control of pole frequency by varying the bias current. In addition, the gain of BP and LP can be tuned individually by the bias current without affecting the parameters of filter. The sensitivities of the circuit are less than unity. The functioning of proposed filter is confirmed with the P-SPICE simulations. The total power consumption is calculated as 0.641mW at1.85mW power supply voltages.

Hua Pin Chen et. al, 2009 [32] presented a new universal biquad filter which works in mixed mode. The circuit is having four single output, one dual output OTAs and two grounded capacitors. The proposed circuit has the ability to realize all the four modes i.e. VM, CM, transconductance mode, and trans-resistance mode, and provides various advantages such as (i) realization of various filter responses like LP, BP, HP, notch, and AP filter, (ii) uses only grounded capacitors which is suitable for integration circuit, (iii) provides independent electronic tenability between ωo and Q, and (iv) sensitivity of components is less than 1. The analog filter chip has designed with TSMC 0.35μm 2P4M CMOS

technology and tested practically. This chip operates at 1MHz and power consumption of the circuit is about 30.95mW.

Sajai Vir Singh et. al, 2010 [33] presented a universal current-controlled CM biquad filter using CCCCTA. The circuit can realize all filter responses from the same configuration and it uses three MOCCCCTAs and two grounded capacitors which is beneficial for integration. Moreover, the filter circuit can be tuned independently (i.e. the pole frequency and quality factor) by changing bias currents of active block. The sensitivities of the circuit are less than 1.

Muhammad Taher Abuelmaatti et. al, 2013 [34] presented a novel mixed-mode biquad filter circuit. It can realize various filter responses from the same configuration such as LP, HP, BP, notch, AP, HP-notch and LP-notch and it uses six single outputs and one dual output OTAs, two grounded capacitors.The circuit provides independent electronic tunability for two parameters i.e. pole frequency and bandwidth.

Chetan Chauhan et.al, 2013 [35] presented a current controlled CM single input three output (SITO) biquad filter using CCTA. The circuit employing two CCTAs and all five passive components i.e. three resistors and two capacitors are grounded. The filter configuration simultaneously realizes LP, BP and BR in current-mode. It can also realize HP and AP filtering with the interconnection of relevant output currents. Moreover, the filter parameter i.e. quality factor and bandwidth can be controlled separately through bias current. It is having low sensitivity for both active and passive components. The workability of the filter circuit is verified through P-SPICE simulations.

Neeta Pandey et.al, 2010 [36] introduced two TM universal filters using one voltage input and several current outputs. The filter employs three multiple output CCCII and two grounded capacitors. It can realize LP, HP, BP, notch and AP responses. As desired, the input voltage signal is given at a high impedance input terminal and the output currents are obtained at high impedance output terminal which cascadability. The circuit can tune the filter parameters by its bias current independently and enjoys low sensitivity. Moreover, the configuration uses less number of components. The functionality has been checked by SPICE simulation.

Supachai Klungtong et.al, 2017 [37] introduced three-input single-output voltage-mode multifunction filter with electronic controllability based on single commercially available IC. In this contribution, the three-input single-output voltage mode filter is presented. The proposed filter uses only single commercially available IC, LT1228 as active element. The natural frequency and quality factor can be tuned electronically by changing the bias current of LT1228. The selection of output filter response can be done without requirement of the matching condition of passive and active component. Also, the selection of all-pass filter response can be done without the requirement of double gain amplifier. Using only single commercially available IC, the proposed filter is suitable for off-the-shelf implementation. The workability of the proposed filter is demonstrated by experimental results.

N. Afzal et.al, 2014 [38] introduced reconfigurable mixed mode universal filter. This paper presents a novel mixed mode universal filter configuration capable of working in voltage and transimpedance mode. The proposed single filter configuration can be reconfigured digitally to realize all the five second order filter functions (types) at single output port. Other salient features of proposed configuration include independently programmable filter parameters, full cascadability, and low sensitivity figure. However, all these features are provided at the cost of quite large number of active elements. It needs three digitally programmable current feedback amplifiers and three digitally programmable current conveyors. Use of six active elements is justified by introducing three additional reduced hardware mixed mode universal filter configurations and its comparison with repoted filter.

J.W. Horng et.al, 2014 [39] introduced three-input-one output current-mode universal biquadratic filter using one differential difference current conveyor, A current-mode universal biquadratic filter is presented. The architecture has three input terminals, one output terminal using one differential difference current conveyor (DDCC), two grounded capacitors and two resistors. It can realize all standard second-order filter functions, which are, high-pass, band-pass, low-pass, notch and all-pass responses without changing the circuit topology. The proposed circuit employs only one DDCC that simplifies the circuit configuration.

N. A. Shahet.al, 2005 [40] introduced a novel voltage-mode universal filter using a single CFA.A novel voltage-mode universal filter using absolute minimum number of active and passive components is presented. The filter uses only one inverting current feedback amplifier (CFA), two resistors and two capacitors, which is bare minimum requirement for this class of filter. The filter besides being devoid of component matching conditions is capable of implementing low-pass (LP), band-pass (BP), high-pass (HP) and notch responses from the same topology. However, implementation of all-pass (AP) signal needs a unity gain inverter. The active and passive sensitivity figures are inferior to unity. PSPICE simulation results confirming the theoretical results are included.

J. K. Pathaket.al, 2013 [41] introduced new voltage mode universal filters using only two CDBAs. Two new configurations for voltage mode filter using only two current differencing buffered amplifiers (CDBAs) are proposed. Both are new configuration can realize all the five standard types of the filters, namely, low pass (LP), high pass (HP), band pass (BP), band stop(BS), and all pass (AP), from the same topology. In contrast to previously known CDBA-based VMUFs, the new configuration do not need an additional active device for voltage inversion to realize all pass function. The proposed configurations offer the tenability of the natural angular frequency (ω_0) quality factor (Q), or the bandwidth (BW) through separate virtually grounded resistors.

C.-M. Chang et.al, 2006 [42] introduced universal voltage-mode filter using only plus-type DDCCs. Despite the extensive literature on current conveyor-based voltage-mode universal biquads with single input and multiple outputs, no filter circuit has been reported to simultaneously achieve all of the advantageous features: (i) employment of only two differential difference current conveyor (DDCC), (ii) employment only two grounded

capacitors, (iii) employment only three resistors, (iv) simultaneously realize voltage-mode low-pass, band-pass, high-pass, notch and all-pass filter signals from the five output terminals, respectively, (v) orthogonal control of ω_0 and Q, (vi) low input impedance and can be cascadable (vii) no need to employ inverting type input signals, and (viii) no need to impose component choice except realizing the all-pass filter signal.

W.Y. Chiu et.al, 2011 [43] introduced high-input and low-output impedance voltage-mode universal biquadratic filter using DDCCs. A new high input impedance voltage-mode universal biquadratic filter with three input terminals and six output terminals is presented. The proposed circuit uses three plus-type differential difference current conveyors (DDCCs), three resistors, and two grounded capacitors. The proposed circuit can realize all the standard filter functions, namely, lowpass, bandpass, highpass, notch, and all-pass, simultaneously, without component matching conditions. The proposed circuit still offers the features of high input impedance, using only grounded capacitors, and orthogonal controllability of resonance angular frequency and quality factor.

Kanhaiya Lal Pushkar et.al, 2012 [44] introduced voltage-mode universal biquad filter employing single voltage differencing differential input buffered amplifier". A new multi-function voltage-mode universal biquadratic filter using single Voltage Differencing Differential Input Buffered Amplifier (VD-DIBA), two capacitors and one resistor is proposed. The proposed configuration has four inputs and one output and can realize all the five standard filters from the same circuit configuration. The presented biquad filter offers low active and passive sensitivities. The validity of proposed universal biquadratic filter has been verified by SPICE simulation using 0.35µm MIETEC technology.

Khachen Khawngam et.al, 2017 [45] introduced mixed-mode third-order quadrature oscillator based on single MCCFTA This paper presents a new mixed-mode third order quadrature oscillator based on new modified current-controlled current follower transconductance amplifier (MCCFTA). The proposed circuit employs one MCCFTA as active element and three grounded capacitors as passive components which is highly suitable for integrated circuit implementation. The condition and frequency of oscillations can be controlled orthogonally and electronically by adjusting the bias currents of the active device. The circuit provides four quadrature current outputs and two quadrature voltage outputs into one single topology, which can be classified as mixed-mode oscillator. In addition, four quadrature current output terminals possess high-impedance level which can be directly connected to the next stage without additional buffer circuits. The performance of the proposed structure has been verified through P-SPICE simulators using 0.25µm CMOS process from TSMC and experimental results are also investigated.

.

Surasak Sangyaem et.al, 2016 [46] introduced five-input single-output voltage mode universal filter with high input and low output impedance using VDDDAs. The design of analog filter using active building block has been gained significant attention and has become an interesting research topic. A five-input single −output voltage-mode universal biquadratic filter using active building block, namely voltage differencing differential difference amplifier (VDDDA) is presented in this paper. The proposed filter consists of two VDDDAs and two grounded capacitors. The presented circuit has high impedance for all input voltage nodes and low impedance for output voltage node which is ideal for cascade in voltage-mode

circuit without the use of buffer circuits. It can provide five output voltage functions which are band-pass (BP), low-pass (LP), band-reject (BR), high-pass (HP) and all-pass (AP) responses. For high-pass and band-pass functions, the inverting and non-inverting response can be achieved. The matching condition, the inverting and double gain amplifier are not required which is easy to select the output response by digital method. The natural frequency and quality factor can be electronically tuned that is attractive for microcomputer or microcontroller controllability. To verify the validity of proposed filter, the P-SPICE simulation and experimental results using VDDDA constructed from commercially available IC are included. The measured results agree well with theoretical expect.

Norbert Herencsar, et.al, 2013 [47] introduced New resistor less tunable voltage-mode universal filter using single VDIBA. To increase the universality of the recently introduced voltage differencing inverting buffered amplifier (VDIBA), this letter presents a new voltage-mode (VM) multi-input–single-output (MISO) universal filter. The proposed filter contains only single VDIBA, two capacitors, and one nMOS transistor, operated in triode region, and is used for resonance angular frequency tuning. Since in the structure no resistors are needed the filter can be classified as resistorless. The VM MISO filter compared with other active building block-based counterparts is very simple; it contains only few transistors, and has the smallest size area. Moreover, no component matching is required and it shows low sensitivity performance.

JiunweiHornget.al, 2013 [48] introduced a grounded capacitor differentiator using current feedback amplifier. A new non-inverting RC active differentiator network base on a current feedback amplifier and using a grounded capacitor is described. Small time constant can be achieved by adjusting a single grounded resistor. Because the output impedance of the CFA is very low, the output terminal of the proposed circuit can be directly connected to the next stage. Experimental results that confirm theoretical analysis are presented.

Tangsrirat W & Channumsin et.al, 2011 [49] introduced high-input impedance voltage-mode multifunction filter using a single DDCCTA and grounded passive elements In this paper, a novel single-input three-output (SITO) second-order multifunction active voltage filter with high-input impedance is proposed. The proposed circuit is based on using the recently reported active building block, namely differential difference current conveyor transconductance amplifier (DDCCTA).It employs one DDCCTA as active element together with one grounded resistor and two grounded capacitors as passive elements. The circuit still maintains the following advantageous features : (i) the simultaneous realization of lowpass, bandpass and highpass responses from the same topology, (ii) no requirements for component matching conditions, (iii) electronic controllability of important filter parameters, (iv) simpler structure due to contains only one DDCCTA and three passive elements, and (v) low sensitivity performance. The non-ideal gain effects of the developed filter are examined and PSPICE simulation results are included using 0.5 μm MIETEC CMOS technology parameters.

Pipat Prommee et.al, 2017 [50] introduced electronically tunable MOS-only current-mode high-order band-pass filters. This paper presents new CMOS current-mode ladder Chebyshev and elliptic band-pass filters (BPFs). The signal flow graph and the network transformation methods are used to synthesize the proposed BPFs by using Chebyshev and

elliptic RLC low-pass prototypes. CMOS-based loss and lossless integrators with grounded capacitors are used to synthesize the proposed BPFs. The proposed filters can be electronically tuned between 10kHz and 100MHz by adjusting the bias current from 0.02µA to 200µA. Both filters use a 1.5V DC power supply, which leads to low dynamic power consumption. Both filters enjoy total harmonic distortion of less than 1.5% along the range of the tuning bias currents. Simulation results are included to illustrate the functionality of the proposed filters.

Hua-Pin Chen et.al, 2014 [51] introduced voltage-mode multifunction biquadratic filter with one input and six outputs using two IC CIIs.A novel voltage-mode multifunction biquadratic filter with one input and six outputs is presented. The proposed circuit can realize inverting and non-inverting low-pass, band-pass, and high-pass filters, simultaneously, by using two inverting second-generation current conveyors (ICCIIs), two grounded capacitors, and four resistors. Moreover, the proposed circuit offers the following attractive advantages: no requirements for component matching conditions, the use of only grounded capacitors, and low active and passive sensitivities. HSPICE and MATLAB simulations results are provided to demonstrate the theoretical analysis.

Jitendra Mohan et.al, 2014 [52] introduced single active element based voltage-mode multifunction filter. The paper presents a new voltage-mode multifunction filter. The proposed filter employs single modified fully differential second generation current conveyor (FDCCII), two grounded capacitors, and three resistors. The proposed circuit enjoys the employment of two grounded capacitors (attractive for absorbing shunt parasitic capacitance and ideal for IC implementation).The proposed circuit provides all five generic filter responses (low pass (LP), high pass (HP), band pass (BP), notch (NH), and all pass (AP) filter responses) simultaneously with single input. The novel proposed filter has low active and passive sensitivities. A number of time domain and frequency domain simulation results depicted through PSPICE using 0.18μm TSMC process parameters are included to validate the theory. The proposed circuit is expected to enhance the existing knowledge on the subject.

Mohd.Usama Ismail et.al, 2014 [53] introduced single input multi output digitally reconfigurable biquadratic analog filter. In this paper, a digitally re-configurable Single input multi output voltage mode multifunctional biquadratic analog filter has been presented. The circuit realizes a Single input multi output filter with non-inverting High Pass, Band Pass and Low Pass outputs and employs four differential voltage current conveyor blocks and uses seven passive components which are two grounded capacitors and five grounded resistors. Digital controlling is incorporated using a current summing network. Tuning of cut-off frequency is carried out with the help of a 3–bit digital control word (k). PSPICE simulations using TSMC 0.25micron CMOS technology have been performed to validate the theoretically predicted results.

Roman Sotner et.al, 2010 [54] introduced universal tunable current–mode biquad employing distributed feedback structure with MO–CCCII.One possible application of the multiple-output electronically-tunable active building block as a universal filter with distributed feedback structure is presented. The suggested structure is less conventional than the well-known state-variable Kerwin-Huelsman-Newcomb but allows the same filter

configurations with the similar properties. The major current-mode design approach disadvantage, ie, the necessity of multiple current outputs, is demonstrated. To date even a rather big line of the commercially available devices do not solve this problem. Some features of the active block used for modelling and transistor-level simulation are briefly discussed. The obvious chance for electronic tuning of the proposed filter is verified.

CHAPTER 3

VARIOUS ANALOG BUILDING BLOCKS AND FILTER DESIGN OBJECTIVE

3.1.VARIOUS ANALOG CIRCUIT BUILDING BLOCKS

Undoubtedly, the IC op-amp has been the most popular building block for various analog circuit designs. However, because of the well-known limitations of op-amp-based circuits such as gain bandwidth trade off, employment of large number of passive components, requirement of component matching in several applications and frequency range limitations because of finite gain bandwidth product as well as finite slew rate, researchers have focused attention on alternative analog circuit building blocks with a view to yet overcome these difficulties when matching the versatility of op-amps to synthesize a wide variety of analog functions.

Thus, a number of alternative building blocks have emerged such as operational transconductance amplifiers (OTA), which was introduced by Wheatley and Wittlinger in 1969, current conveyors (CC) current feedback operational amplifiers (CFOA) operational transresistance amplifiers (OTRA) (commercially available as Norton amplifier), current differencing buffered amplifiers (CDBA) ,current differencing transconductance amplifiers (CDTA), four-terminal floating null or (FTFN), differential difference current conveyors (DDCC), dual output second generation current conveyors (DOCCII), multiple output second generation current conveyors (MOCCII), differential voltage current conveyors (DVCC), inverting second generation current conveyors (ICCII), fully differential second generation current conveyors (FDCCII), current follower transconductance amplifiers (CFTA), current backward transconductance amplifiers (CBTA) etc.

This thesis is mainly concerned with the employment of two new building blocks namely, voltage differencing transcoductance amplifier (VDTA) and voltage differencing current conveyor (VDCC) in “Some Investigations into Analog Signal Generation/Processing using New Generation Current Mode Active elements”. It now appears necessary to give the detailed account of the work done on the use of the quoted building blocks in the use of various applications, starting from the classical op-amp.

3.1.1. Operational Amplifier (OP-AMP)

Operational amplifiers (op-amps) are the most popular active building blocks for analog signal generation and processing. Op-amps find applications ranging from direct

current applications to high speed amplifiers and filters. Some basic application of General purpose op-amps are summers, buffers, differentiators, integrators, impedance convertors, comparators etc. The op-amp is a differential voltage controlled voltage source (DVCVS). The symbolic representation of the op-amp is shown in Fig.3.1.1.

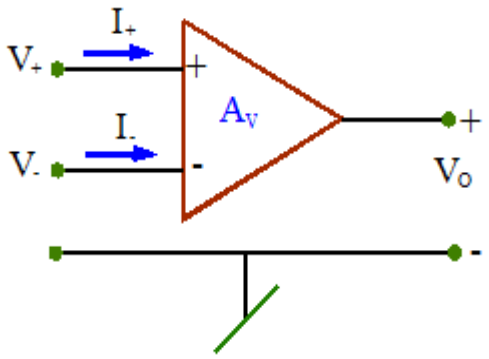


Fig.3.1 Symbolic representation of the op-amp

An ideal op-amp is characterized by $V_o = A_v (V_+ - V_-)$, where A_v = open-loop voltage gain and $I_+ = I_- = 0$.

A typical CMOS implementation of the op-amp is shown in Fig.3.1.2.

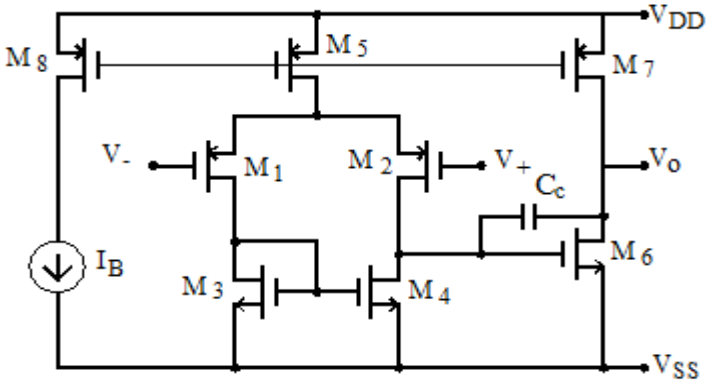


Fig.3.2 CMOS realization of an op-amp

3.1.2. Multi Output OperationalTransconductance Amplifier (MO-OTA)

The most widely used active ingredient for on chip implementation is undoubtedly the operational transconductance amplifier (OTA), introduced by Wheatley and Wittlinger in 1969. Bialko and Newcomb in 1971, demonstrated how all basic linear functions are performed using the integrated differential voltage-controlled-current-source (DVCCS). For an ideal OTA with transcoductance g_m the output current I_o is given by $I_o = g_m(V_+ - V_-)$. The transconductance (g_m) can be varied by changing the bias current I_{bias}. The transconductance

(g_m) of bipolar OTA is $I_{bias}/2V_T$ and of CMOS OTA is equal to $(\beta I_{bias}/4)^{1/2}$ (where $\beta = \mu_s C_{ox}(W/L)$) respectively. A CMOS low voltage OTA was introduced by Elwan, Gao, Sadkowski and Ismail in 2000. The generalized version of Bipolar OTA (BOTA), was MO-OTA and its applications were demonstrated in the design of economical biquadratic filters in. The symbolic notation of MO-OTA is shown in Fig.3.1.3.

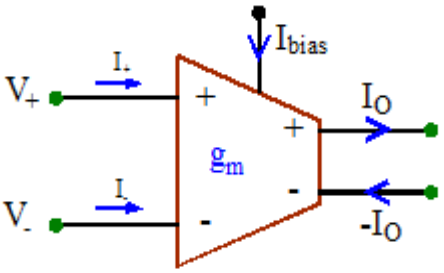


Fig.3.3 Symbolic notation of MO-OTA.

A CMOS realization of the MO-OTA is shown in Fig.3.1.4.

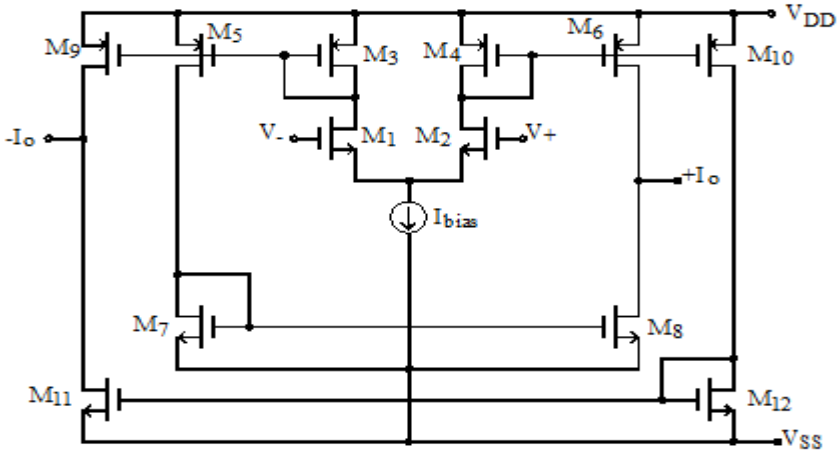


Fig.3.4 CMOS realization of the MO-OTA

3.1.3. Second Generation Current Conveyor (CCII)

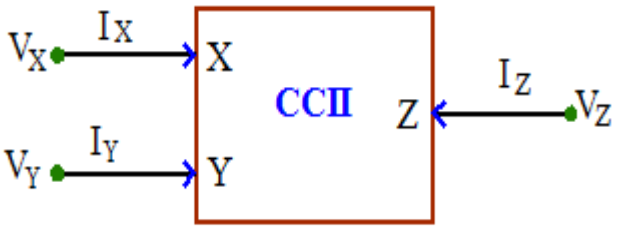


Fig.3.5 Symbolic notation of CCII

For an ideal second generation current conveyor (CCII) [3], the port characteristics can be described by the hybrid matrix:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \qquad 3.1)$$

Depending on the current direction in the Z terminal, CCII is characterized in a positive and negative version. Fig. 3.1.6 shows the specific CMOS implementation of CCII.

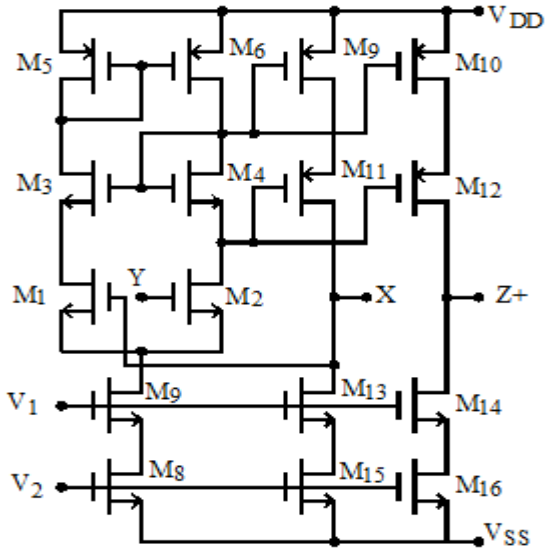


Fig.3.6 A typical CMOS implementation of CCII

3.1.4 Current Feedback Operational Amplifier (CFOA)

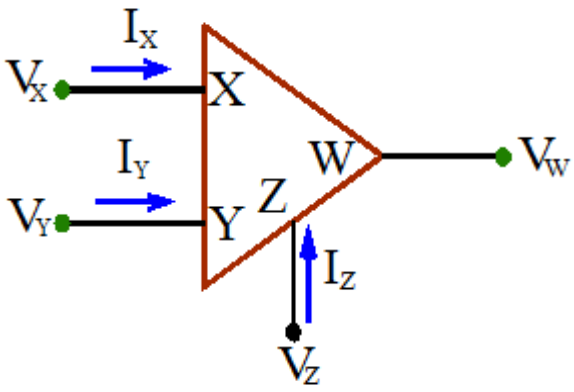
Another building block closely related to both op-amp and CCII+, which has received significant attention during the past more than one decade, has been known as transimpedance operational amplifier or more popularly known as CFOA. It offers several advantageous features over the traditional voltage-mode op-amp (VOA).

The conventional transimpedance operational amplifier (TOA) can be design by combining the CCII and the voltage buffered amplifier. CFOA and TOA have an identical internal structure. The absence of electronic control of the voltage gain or any other parameter in the conventional op-amp enforced designing the current controlled CFA (CC-CFA).

Differential voltage CFA (DVCFA) is an interesting form of CFOA and another generalized form, namely, the Differential Differential Supplemental Current Feedback Amplifier (DDCFFA)

introduced by Gupta and Senani which has been shown to be able to detect a large number of prevalent buildings. Obstruction.

Fig.3.7 Symbolic notation of the CFOA.



The port relationship of the ideal CFOA is described by the following hybrid matrix:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \\ V_W \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \\ I_W \end{bmatrix} \quad (3.2)$$

3.1.5 Current Differencing Transconductance Amplifier (CDTA)

CDTA was proposed by Biolek in 2003 for the first time. External resistors may not be required in CDTA applications as they are substituted by internal transconductors. It is a current mode active component as its input as well as output signals are currents. The symbolic notation of CDTA is shown in the Fig.3.8.

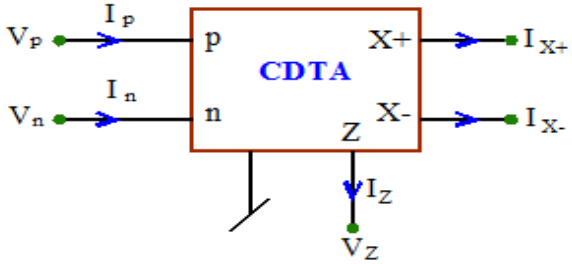
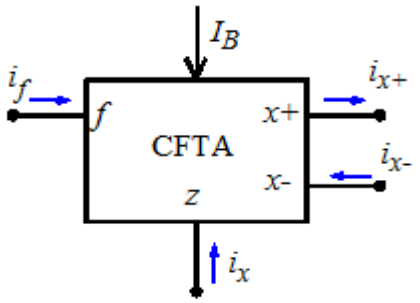


Fig.3.8 Symbolic notation of CDTA

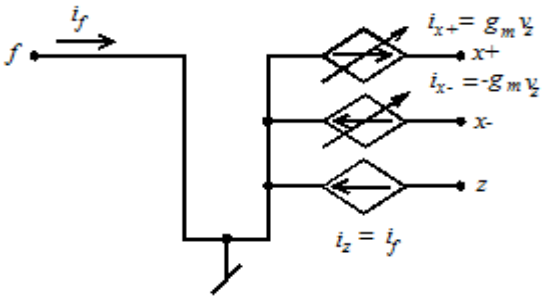
3.1.6. Current Follower Transconductance Amplifier (CFTA)

The CFTA, whose symbolic representation and behavioral model are shown in Fig.3.1.9 and Fig.3.1.10, consists of an input current follower stage along with an output transconductance amplifier stage. The input current follower transfers the input current to the Z-terminal while the output transconductance amplifier translates the voltage at the Z-terminal into output currents.



(a)

Fig. 3.9 Schematic symbol of CFTA



(b)

Fig.3.10Behavioral model of CFTA

The ideal terminal relationships between the terminals of CFTA can be described by equation set (3.3)

$$\begin{bmatrix} v_f \\ i_z \\ i_{x+} \\ i_{x-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & +g_m & 0 & 0 \\ 0 & -g_m & 0 & 0 \end{bmatrix} \begin{bmatrix} i_f \\ v_z \\ v_{x+} \\ v_{x-} \end{bmatrix} \qquad (3.3)$$

3.1.7. Voltage Differencing Differential Input Buffered Amplifier (VD-DIBA)

The VD-DIBA is a five terminal ABB introduced by Biolek and Biolkova in 2010 is shown in Fig. 3.1.11.The input stage of VD-DIBA can be implemented easily by a differential input single-output OTA, which converts the differential input voltage to output current that flows out at the Z-terminal. The output stage can be formed by unity-gain differential voltage buffer. From the model it can be seen that the VD-DIBA has two high-impedance voltage input terminals V+ and V-, one high-impedance current output node Z, and one low-impedance voltage output terminal W.

The schematic symbol and behavioral model of VD-DIBAare shown in Fig.3.1.11. (a) and (b) respectively.

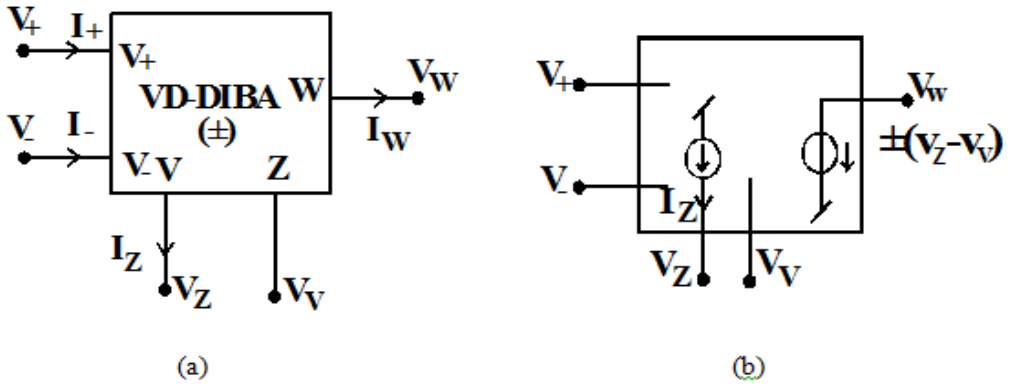


Fig.3.11 (a) Schematic symbol, (b) behavioral model of VD-DIBA

VD-DIBA can be described by the following hybrid matrix.

$$\begin{pmatrix} I_+ \\ I_- \\ I_z \\ I_v \\ V_w \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \pm 1 & \mp 1 & 0 \end{pmatrix} \begin{pmatrix} V_+ \\ V_- \\ V_z \\ V_v \\ I_w \end{pmatrix} \qquad (3.4)$$

3.2 OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

The OTA was commercially available for the first time in1969 by RCA**(**Radio CorporationofAmerica).Theschematicsymbolandsimplebipolarimplementationof OTA are shown in Fig.3.1 and Fig.3.2.

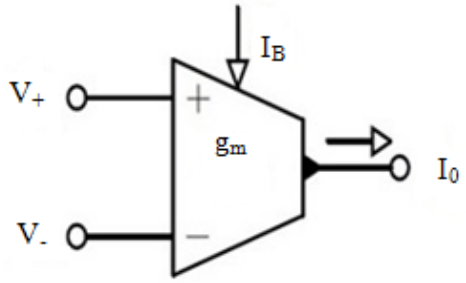


Fig.3.12Schematic symbol of OTA

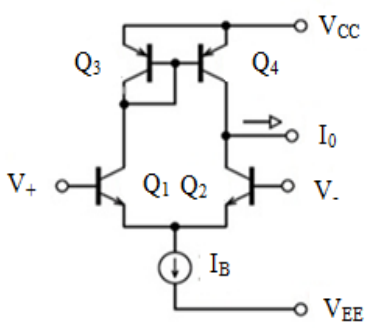


Fig.3.13 Bipolar implementation of OTA

In Fig.3.13, transistors Q_1 and Q_2 operate as a differential amplifier to convert an input voltage to an output current and simple current mirror formed by the transistors Q_3 and Q_4 where I_B is an input bias current. The ideal OTA exhibit the properties of voltage- controlled current source (VCCS) and characterized by its transconductance g_m. The output current of the OTA is given by the Eqn.(3.1)

$$I_0 = g_m(V_+ \quad - V_-) \qquad (3.5)$$

Where V_+ represents the voltage present at the non-inverting terminal of OTA while V_-represents the voltage present at inverting terminal of OTA. Ideally, the OTA amplifier has finite transconductance g_m that must be frequency-independent on the other hand its input and output impedances are infinite theoretically. The bipolar OTA shown in Fig.3.2 the transconductance can be expressed by the Eqn. (3.2) as follows:

$$g_m = \frac{I_B}{2V_T} \qquad (3.6$$

Where V_T stands for the thermal voltage (approximately 26mV at 27°C) and I_B stands

for the bias current (control current) by which the transconductance g_m of the OTA can be varied. Currently, the OTA elements are distributed in the market by many manufacturers. There are some commercially available OTA element such as the circuit LT1228 (Linear Technology) or MAX435 (MAXIM-Dallas Semiconductor). These are the high-speed wideband transconductance amplifier (WTA) having high-impedance inputs and output. It is suitable for a wide variety of applications such as high-speed RFfilters, high-speed instrumentation amplifiers, and high-speed differential line driver and receiver applications due to its special performance features.

3.3 DESCRIPTION OF VDIBA

The VDIBA is recently introduced four terminal active elements and associated with the feature of electronic tuning the circuit symbol and behavioral model are shown in Fig.3.3 and Fig.3.4 respectively. VDIBA consist with a pair of voltage differencing inputs V_+ and V- having high impedance, high impedance current output i.e. z terminal, and voltage output noted as w- exhibit low impedance.

The VDIBA composed of OTA and inverting voltage buffer (IVB). Firstly, the differential input single output OTA configuration has been used as shown in Fig.3.4 so that the OTA easily converts the input voltage into the output current that flows out from the z terminal followed by a unity gain IVB. This active block is found to be a very attractive for designing resistorless and electronically controllable application.

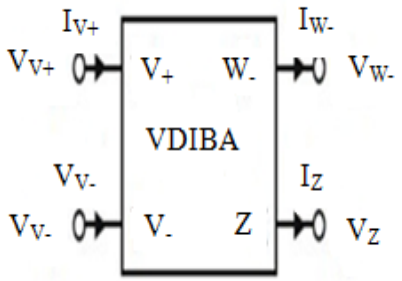


Fig.3.14 Circuit Symbol of VDIBA.

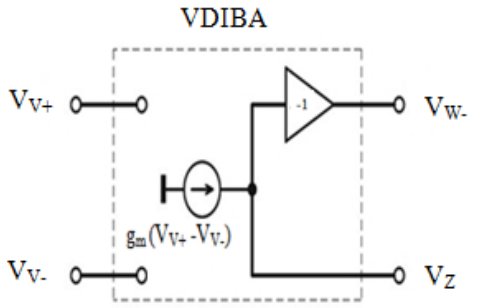


Fig.3.15 Behavioral model of VDIBA

Using ideal notation, the relationship between port currents and voltages of a VDIBA are given by Eqn. (3.7).

$$[I_{v+}\ I_{v-}\ I_z\ V_{w-}\ ] = [0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ g_m\ -g_m\ 0\ 0\ 0\ 0\ -\beta\ 0\ ][V_{v+}\ V_{v-}\ V_z\ I_{w-}\ ] \quad (3.7)$$

In the above matrix, g_m and β have transconductance and non-ideal voltage gain, respectively. For an ideal VDIBA,The value of β for an ideal VDIBA is equal to unity.

The CMOS implementation of the VDIBA in Fig.3.5. The circuit is composed of a cascade of active load differential pairs (transistors M1 and M4) with a unity gain inverting voltage buffer (match transistors M5 and M6).

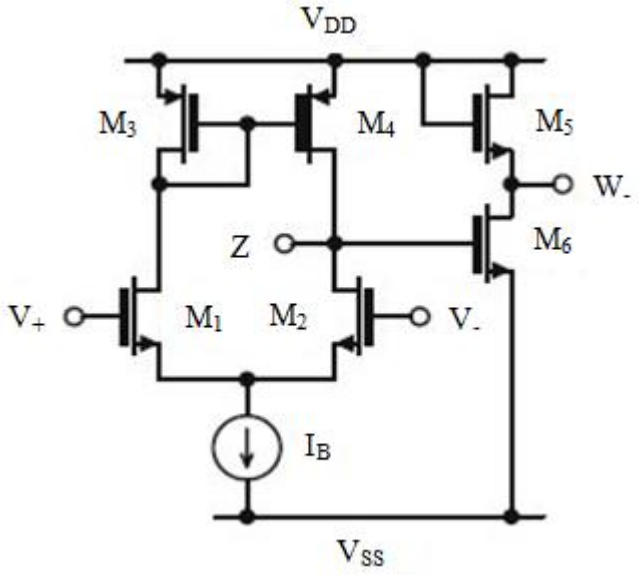


Fig.3.16 CMOS implementation of VDIBA

The input/output terminal resistances of the CMOS VDIBA can be calculated as:

$$R_{ow-} = \frac{1}{g_{mb}} \| r_{o6} \quad (3.8)$$

$$R_{oz} \cong r_{o4} \| r_{o2} \tag{3.9}$$

$$R_{v+} = R_{v-} \cong \infty \tag{3.10}$$

The g_{mb} and r_{ow} represent the transconductance and output resistance of the i^{th} transistor, respectively. From Eqn. (3.4) to (3.6) it can be seen that while the output terminal (w-) can exhibit low resistance by selecting large transistor M_5 (and M_6 due to the matching condition requirement), the input terminals (V_+ and V_-) as well as the z terminal, have high resistances.

When any analog filter circuit has been realized using a high-performance building block like VDIBA, the first-order AP filter become a first choice mainly for the communication and instrumentation systems. Due to of its high accuracy, wide bandwidth, low voltage and low power implementations make block an ideal choice for analog signal processing applications.

3.4. FILTER THEORY

Filters are used as ABBs namely the UF or multifunctional filter, which can provides several functions from one topology, SIMO is the most popular analog filter configuration in which several transfer functions can be realized simultaneously.

Filters can be considered as an arrangement of signal determination. It has been broadly utilized as a part of numerous territories, for example, radar, correspondence, aviation, medicine, programmed control and image processing control, and so forth.

The building block of the filter is shown in Fig.3.6 which illustrates the basic working of a filter.

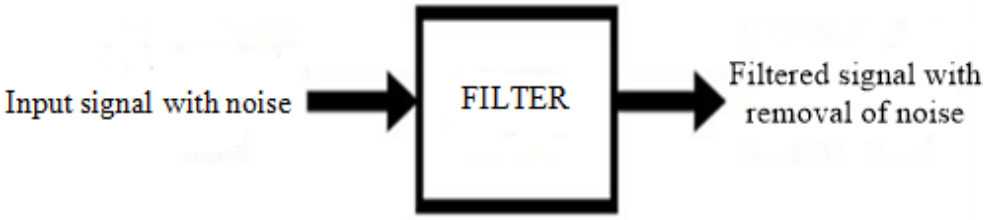


Fig.3.17 Building block of filter

(a) The capacity of a filter is to expel undesirable parts of the signal (e.g., noise) or to extort valuable parts of the signal.
(b) To limit a signal into particular frequency band as a ratio, TV channels selector and anti-aliasing filter.
(c) For dispensation sub-band signal split a signal into two or more sub-band signals, for ex., in coding of music.
(d) To regulate the frequency spectrum of a signal, for ex., in a microwave spectrum analyzer.
(e) To imitate the input-output association of a system, for ex., in a mobile communication channel, voice production, musical instruments and room acoustics.

Filters are the basic ABB widely used in communication system for realizing radio frequency (RF), intermediate frequency (IF) filters.

(a) In modems and voice processing applications mostly low frequency BP filters are used for the audio frequency range is between 0kHz to 20kHz.
(b) In the telephone fundamental organization, high frequency BP filter of numerous hundred MHz have been used to select the channel.
(c) Anti-aliasing LP filters and noise filters used in data acquisition systems.
(d) The BR filter is used to suppress the line frequency Hz 60 (50) and high frequency transients in the power supply system.

The filter is essentially called as a framework in circuit hypothesis that can adjust the amplitude and phase attributes of a signal as for recurrence. In a perfect world, the filter will neither add new frequency to the input signal, nor it changes the component frequencies of that signal. It basically changes the amplitude and phase relationship of the different frequency component.

It electronic framework, filters are utilized essentially to acknowledge the specific scope of the signal, here and there used to tune a single frequency furthermore to reject signals in other frequency ranges. The gain relies on upon signal frequency for this sort of filter. Active channel contains basically one active components whose output is associated with its contribution through typically inactive segments C and R This criticism from output

to include permits us to assemble filters with nonexistent poles utilizing C and R alone. The fundamental target of active filter is to wipe out inductors (L) and lessening the estimation of the filter capacitance.

3.4 1. TYPES OF FILTERS

There are basically two types filters which are classified as:

(a) Analog filter
(b) Digital filter

3.4.1.1.Analog filter

Analog filter are typically made with electronic network using three basic components: the R, L and C. By the adjustment of these elements in a various configuration, it is likely to change the filter performance for particular use as given:

(a) The OTA are typically used to increase the performance of such filters.
(b) It is vital to make a note that these filters are normally utilized in signal conditioning process than any digitization process is carried out. This can help to eliminate unnecessary noise or decline of BW to make it simpler and easier signal processing. The mainly prominent purpose of this type is for anti-aliasing function in LP filtering.
(c) The efficiency of analog filters is dependent upon the value of the element used in circuit fabrication. Various parameters, for example: tolerance factor components, power dissipation , design methods and often the dimension of all elements play a vital role in creating realistic constraints of analog filters.

Analog filters can be classified as:

3.4.1.1.1. Passive Filter

The filters utilized for the above example were produced by using passive elements, such as R, C and L, so that filters are known as passive filters. A passive filter is basically one that utilizes no recative elements such as transistors, OTAs etc. in this context, it is the easiest to implement a TF on given in terms of the amount of essential elements. Passive filters have a little more profit, thus:

(a) Passive filters need no power source for biasing as they have no active components.
(b) Not being limited by the BW limitations of OPAMPs, which are able to do the job well in vary large frequencies.
(c) Can be used in functions related to the high current and voltage levels that cannot be handled by the active devices.
(d) Passive filters as well as produce slight noise when circuit made by active component. The noise generated is simply the thermal noise that comes from the resistive elements, and a prudent design, the magnitude of this noise can be much reduced.

Passive filters have a number of significant drawbacks in some functions given as:

(a) Because no use active components, which cannot provide a signal gain.
(b) The input impedances may be less than advantageous, and output impedances can be optimized many functions, so buffer amplifiers may be needed. The L is essential to carry out the generally functional passive filter features.
(c) These can be very expensive if high correctness (1% or 2%) in the material size, large values is required.
(d) The principal values of the L elements are not spaced very strictly and that is difficult to locate an off-the-shelf part within 10% of any random value, so modifiable L elements are used. These are changed to the required values is time consuming and expansive, when the filter is generated greatly.
(e) In addition, passive filters made with more than seconds order can be complicated and time consuming to synthesize.

3.4.1.1.2. Active filter

Active filters utilized amplifying components, particular OPAMPs together with the R and C in its feedback circuit loop to design filter characteristics required. These filters have benefits as follows:

(a) Active filters have input impedance while small output impedance and almost random gain.
(b) They are thus typically simply synthesis compared to passive filters.
(c) Probably the main significant feature is that they lack passive element, inductor, thereby reducing the problem associated with these elements.
(d) However, the difficulty of value spacing and correctness also influence C, although less.
(e) Efficiency at higher frequency is limited by the gain BW product of the amplifying

components, but within operating frequency range the OPAMPs based active filters are able to achieve very fine correction, that offer small tolerance R and C are used.

A number of the drawback of the filters is given below:

(a) Active filters produce noise due to amplification networks, but this causes minimizing the use of small noise amplifiers and synthesis of good circuit.

Tunable active filters are extensively used in instrumentation and communication where variable frequency operation is required. In these types of filters, frequency of the filter can be controlled by bias voltage or bias current. Also, by using tunable filters, RC variation could be compensated. Therefore, the tunable active filter has gained improved popularity in recent time. Tuning approach can be used to set the desired value of filter parameters namely pole frequency, quality factor and BW. During these days, multifunctional filters and UFs have received considerable attention because of its versatility in different applications KHN (Kerwin-Huelsman-Newcomb) biquard is well known example of multifunction filter which provides independent control of the angular frequency ω_0 and Q.

3.4.1.2. Digital filter

In signal processing framework, a digital filter is a framework that performs numerical operations on an inspected signal, discrete-time signal to enhance or diminish certain parts of that signal. This is conversely with the other primary sort electronic filter, simple channel, which is an electronic circuit which works in consistent time analog signals.

A digital filter framework comprises of a analog to digital converter for inspecting the input signal, trailed by a microprocessor and a few peripherals, for example, memory for putting away information and filter coefficients and so on. At last, a digital to analog converter is expected to incorporate the output stage. Program directions running on the microchip to actualize the digital filter by playing out the scientific operations on the numbers got from the ADC.

In some elite applications, an application specific integrated circuit (ASIC) or field programmable gate array (FPGA) is utilized rather than a broadly useful chip or a digital signal processor (DSP) devoted to a particular design in parallel to accelerate operations, for example, filtering. Digital filters can be more costly than an equal simple filter because of its more prominent unpredictability, however numerous useful plans that are outlandish or unreasonable as simple filter. At the point when pre-claimed with regards to real time analog

systems, digital filters are now and then have latency issue due to the related analog to digital and digital to analog convertor anti-aliasing filters, or because of different delays in its usage.

3.4.2 Tunable Multifunction Filter

Active filters widely used in signal processing and instrumentation area where frequency of the filter can be controlled by the current or voltage. Also by using the tunable filters, RC time constant variation problem can compensate. Thus, tunable active filter is getting more attention in designing of the analog filter. These are bandwidth adjustable. If we are tuning a tunable band pass or band reject filters provide the best solution for pre-tuning the desired signals while rejecting the interfering signals. Depending on the specific application, the tuning range can varied. During these days, second order filter structures that can realize basic three filter responses such as LP, HP, BP or all standard i.e. BS and AP with the same configuration receives huge attention. Such types of topologies are called universal or multi function filters, respectively. Mainly, the best known multifunction filtering structure is based on the KHN (Kerwin–Huelsman–Newcomb) that provides mutually separate control between the natural angular frequency ω and quality factor Q.

3.4.3 Design Consideration

The design consideration needed for the designing of tunable active filters can be summarized as follows:

(a) Lowering the number of active components.

In order to carry out economical designing, less numbers of active elements should be used as they occupy less area on the chip.

(b) Use of grounded resistors:

If tunability feature is required to be used in the circuit then less number of component count is required.

(c) Use of grounded capacitors:

With the use of grounded capacitors one can achieve economically tunable circuit realization.

(d) **Independently controlled w_0 and Q:**

Both the parameters are set independent of each other so that they can functional

individually without affecting one another.

(e) Use of commercially available CCIIs:

Commercially available CCs are used so that the filter could be implemented with ease from the available integrated circuits.

3.4.4 Filter Applications

Filter is basic building blocks used widely in Communication Systems for realizing RF, IF filters.

(a) In modems and speech processing applications mostly low Frequency band-pass filters are used for the audio frequency range lies between 0KHz to 20KHz.
(b) Intelephonecentraloffices,high-frequencyband-passfiltersofseveral100MHz have been used for selecting the channel.
(c) Anti-aliasing low-pass filters as well as noise filters used in Data acquisition systems.
(d) Band-rejection filters are used to suppress the 60 (or 50)Hz line frequency and high frequency transients in system power supplies.

CHAPTER 4

REALIZATION AND VERIFICATION OF PROPOSED SIGNAL PROCESSING CIRCUITS

4.1. TOOL USED

To simulate the OTA circuit,tanner EDA tool version 13.0 is utilized. Tanner tool is a computer analyse program for analog ICs. Tanner tool package contain followong simulation software

(a) S Edit(Schematic Edit)
(b) T Edit (Simulation Edit)
(c) W Edit(Waveform Edit)
(d) L Edit (Layout Edit)

Using these software , program gives provision to the user to invent and simulate innovative ideas in analog ICsprior to departing to the valuable time spending and precious action of chip production.

4.1.1 S-Edit

S Edit is series of commands of file, modules and pages. Itcontribute symbols and schematic models. S-Edit gives the provision of:

(a) Commencement of modelling.
(b) Design connectivity.
(c) Viewing, drawing and editing of objects.
(d) Instance and browser schematic and symbol mode.
(e) Properties, net lists and simulations.

In S-Edit, the provides elements form the library can be chosen to put together the schematic design of the necessary circuit. It provides the information process for implementing development in detail in terms of file module processand module. Efficient

schematic circuit modelling needs a working understanding of the S-Edit design information files consist of modules. A module is a operational component of design model such as a mosfet,a gate and an amplifier. Modules consists of two parts:

(a) Primitives – Geometrical objects designed utilising drawing software tols.
(b) Instances – Orientation to other sectional module in file.The instance part of module is the unique.

Two viewing modes of the S-Edit are:

(a) Schematic mode – This approach assists in designing or viewing a schematic.
(b) Symbol mode – It shows symbol of a bigger working part such as operational amplifier.

4.1.2 T-Edit

The main part of T-Spice function is the output file also referred as the network description, the connection etc. It is the simple test file document that consists of device modeling report and commands that comes from the SPICE language utilizing of which T-Spice design a model of the network which is to be run. Input files of the design be able to be generate an customized using any test editing tool. T spice is a software tool for simulation of the designed models. It gives the provision of:

(a) Simulation of design models.
(b) Commands for simulation.
(c) Statements of device.
(d) External models defined by user.
(e) Small signal and noise models.

T-spice utilize KCL to solve network difficulties. In T-Spice tool the whole design model circuit combination of devices circuits connected to the nodes. Various power supply voltage source present at all nodes source the design modelling state. T-spice software tool solve for a set of node voltage that fullfill the KCL condition. To estimate whether a set of nodes voltges is a way out or not, T-spice computers and edition of all the current passing out of each device into node link to it. The association between the voltages at device terminal and currents through the terminal is calculated by the Eqn.(4.1) of device model for a register passive component having resistance (R).

$$\dot{I} = \frac{V}{R} \qquad (4.1)$$

where V represents the voltage difference between two terminal of the device.

4.1.3W-Edit

The capability to think about the compound mathematical data resultant from VLSI circuit simulation is significant to testing, understanding and getting improved such design. W-Edit is a software for waveform viewing that offers simplicity of utilisation, power supply and swiftness in familiar environment designed for graphical data.The advantages of W-Edit include.

(a) Tense integration among T-Spice design simulator. Also W-edit can plot a waveform utilizing data offer by T-Spice software directly devoid of adjustment of the output text files of device data. This data can also be plotted dynamically as it is created during the running of software.
(b) Chart can repeatidily organise for the kind of data being obtained.
(c) A data is handled by W-Edit as a part known as trace. Traces from various output files can be view concurrently in a particular or several windows, traces can be mock and move between chart and window. Trace arithmetic of the design can be done on trace to generate new traces.
(d) Chart view can be enlarge and minimise including categories the accurate X and Y coordinate range.
(e) Various properties such as axis, traces charts test and colours can be modified. Various numarical data at the input to W-edit in the form of plane or digital type test files.
(f) Moreover header, comments provided by T-spice tool is automatic plot configuration. Runtime of output is prepared by connecting W-edit to a running simulation in T-spice tool. W-edit data alongwith chart, trace axis and environment setting in data file having W-edit database (WDB).

4.1.4 L-Edit

It is a software tool that show the mask that are utilized to model integrated circuit (ICs) devices. It describes the layout design model in term of data files, cells and mask primitives modules components. On the other side at the layout level the elements parameters are totally diverse from systematic design of device, thus it offers the feature to the client to understand the output of device circuit prior to forward it to the time killing and expensive procedure of manufacturing the design. Various rules for masking layout circuit diagram of a schematic circuit utilising of which user can figure out the difference between output response with the expected one.

In L-Edit tools layers are linked with masks utilized in manufacturing procedure. Various layers can be suitably represented by various patterns, colours. It also explains a layout in terms of data files, cells modules, instances and mask primitives components. We can load a large number of files as needed into memory. The file might be have numerous sets. Such cells might be arranged hierarchically in a classic design or they might be free in a library file. All cells might consists large number or
mixture of mask primitives modules and instances of different cells.

Cell is the fundamental building block of the ICs design in L-Edit. Design layout take

place within cells. Thus a cell is able to:

(a) Contain small part or the entire design.
(b) Be mention in other cells as a sub cell and also as instance.
(c) Be implemented up completely of instances of different cells modules.
(d) Contains unique draw primitives.
(e) Be implemented completely by primitives modules, a large number of combination of primitives module and instances of different cells.

4.2 SIMULATION ANALYSIS

For the circuit simulation, various types of Simulation analysis have been done such as DC analysis, AC analysis and Transient analysis etc. The AC small-signal analysis mainly linearizes the circuit with its DC operating point and evaluates the response for a given small sinusoidal source. Specter can perform the analysis while sweeping a parameter. The parameter can be a design variable, frequency, temperature and a component model parameter. The DC analysis is used to calculate the DC operating point and to examine different DC transfer curves of the circuit. In this analysis, we must have to specify a parameter and a sweep range to generate transfer curves. The parameter can be a temperature, a device instance parameter like voltage.

4.3 ANALYSIS OF VDIBA

DC analysis and AC analysis have been performed to check the functionality of VDIBA. The schematic of VDIBA has been created by using virtuoso schematic composer as shown in Fig.4.1. For the simulations, DC power supply voltages have been taken as $+V_{DD} = -V_{SS} = 0.9V$. The bias current is set at 100μA. The aspect ratios taken for the OTA and IVB are listed in Table 4.1.

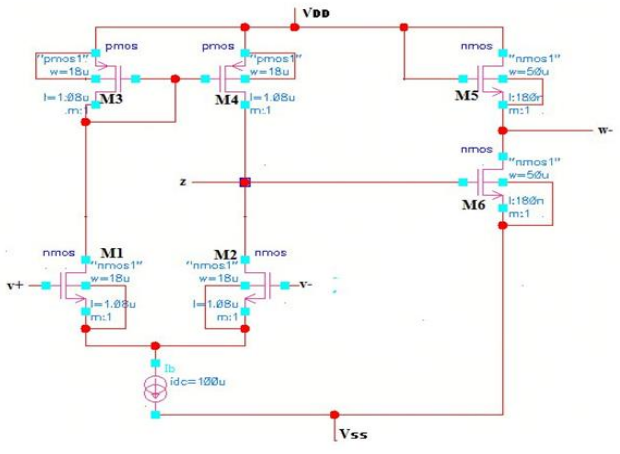


Fig.4.1 Schematic of VDIBA

Table 4.1 Aspect ratios for CMOS VDIBA

Transistor	W/L(μm)
M_1	18/1.08
M_2	18/1.08
M_3	18/1.08
M_4	18/1.08
M_5	54/0.18
M_6	54/0.18

Note that the W/L ratio of the transistors M_5 and M_6 should be selected high to decrease the loading effect.

4.4 ANALYSIS OF BIQUAD FILTER

The voltage mode MISO type universal biquad filter is shown in Fig4.2. The VM second-order filtering structure employs single VDIBA and has three passive components. The circuit is multifunctional and it is capable of realizing LP, HP, BP, BR and AP responses without changing the circuit topology. Component matching condition and the inverting inputs are not required.

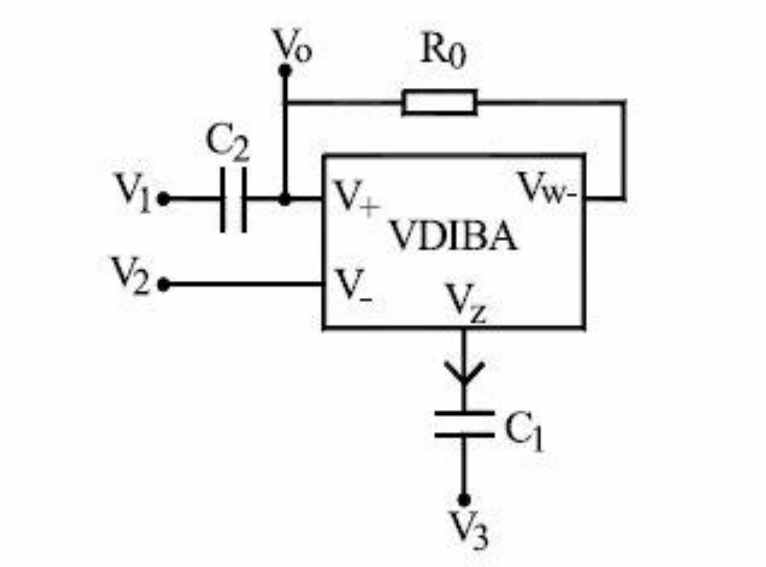


Fig.4.2.Voltage Mode Universal Biquad Filter

The ideal output voltage$V_0$of the circuit is given by the relation as follows:

$$V_O = \frac{V_1 S^2 - V_3 s\left(\frac{1}{R_O C_2}\right) + V_2 \frac{g_m}{R_O C_1 C_2}}{S^2 + s\left(\frac{1}{R_O C_2}\right) + \frac{g_m}{R_O C_1 C_2}} \quad (4.2)$$

From Eqn. (4.2) the various filter responses can be realized:

(a) If $V_2 = V_{in}$ and $V_1 = V_3 = 0$ (grounded), thenLPfilter can be realized.
(b) If $V_1 = V_{in}$ and $V_2 = V_3 = 0$, then HP filter can be realized.
(c) If $V_3 = V_{in}$ and $V_1 = V_2 = 0$, then BP filter can be realized.
(d) If $V_1 = V_2 = V_{in}$, and $V_3 = 0$, then BR filter can be realized
(e) If $V_1 = V_2 = V_3 = V_{in}$ then AP filter can be realized.

The expressions for natural frequency (ω_0) and bandwidth (BW) are given:

$$\omega_O = \sqrt{\frac{g_m}{R_O C_1 C_2}} \quad (4.3)$$

$$B\dot{W} = \frac{1}{R_O C_2} \quad (4.4)$$

It can be seen from Eqn.(4.3) and Eqn. (4.4) that by fixing the value of BW, $\dot{\omega}$ can be independently and electronically varied by the transconductance of VDIBAi.e g_m. Moreover, non inverting input and matching condition needed to realize all the five filter functions. But, floating passive elements have been used which is not attractive for integration.

4.4.1 Performance Results

To check the functionality of biquad filter, (as shown in Fig 4.2) the circuit is simulated at tanner. For this, the value of passive elements has been taken as C_1=0.1nF C_2=0.05nF and R_o=1.67KΩ. The transconductance of VDIBA taken as 656.0094μA/V and is controlled by the bias current I_b.

The resonance frequency and BW of the proposed filter for the selected passive element are 1.34 and 11.95MHz, respectively. The total power consumption of the proposed biquad has been found to be 10.5mW. The frequency responses of LP, BP, HP, BS and AP filter are calculated in voltage mode as shown in Fig.4.3, Fig.4.4, Fig.4.5, Fig.4.6, and Fig.4.7 respectively.

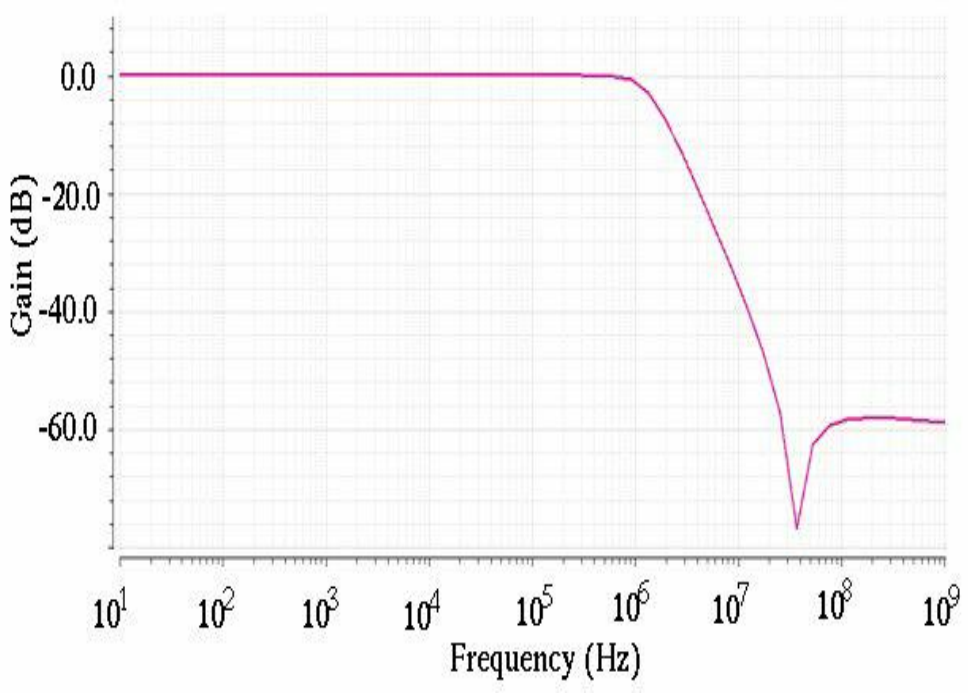


Fig.4.3: Frequency response of LP filter

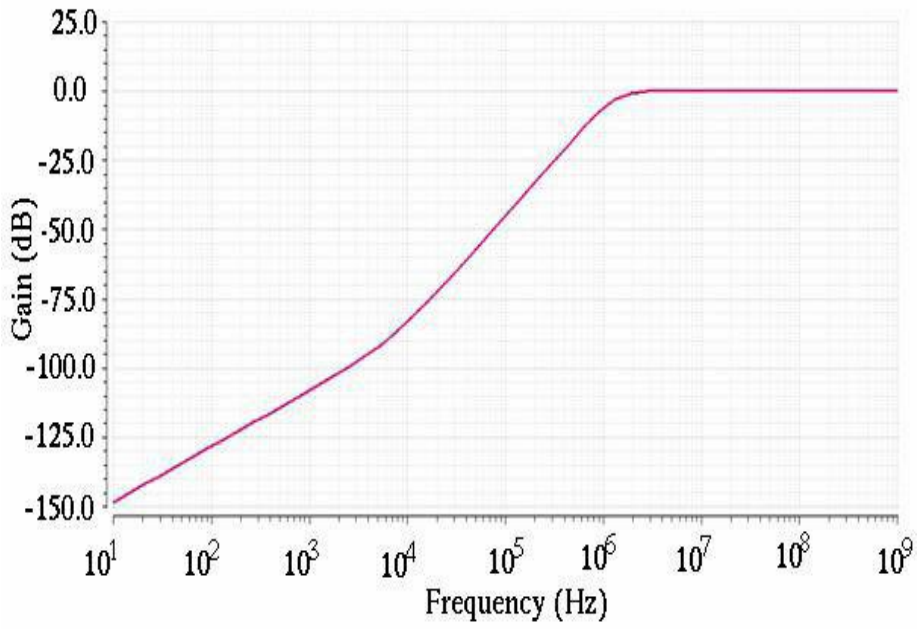


Fig.4.4: Frequency response of HPfilter.

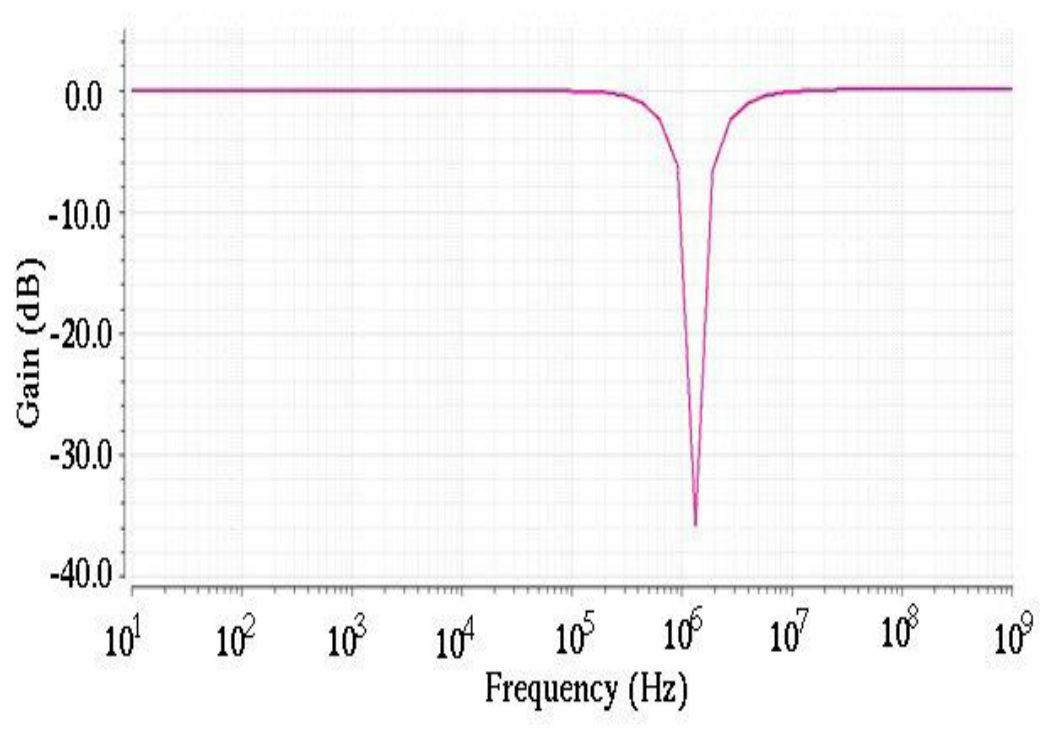


Fig.4.5: Frequency response of BRfilter.

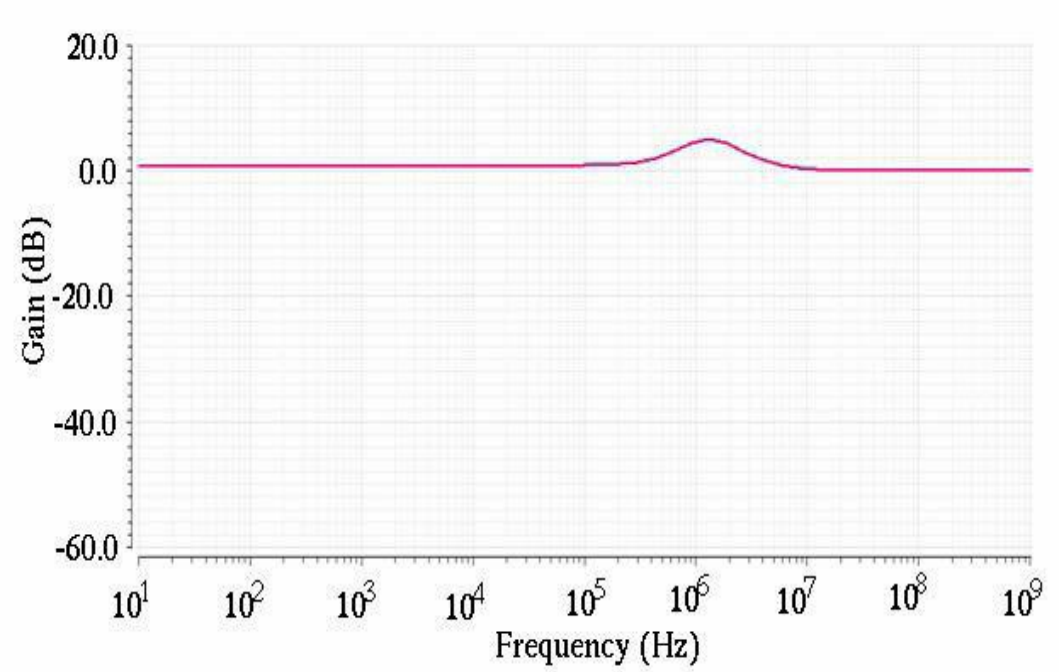


Fig.4.6: Frequency response of APfilter

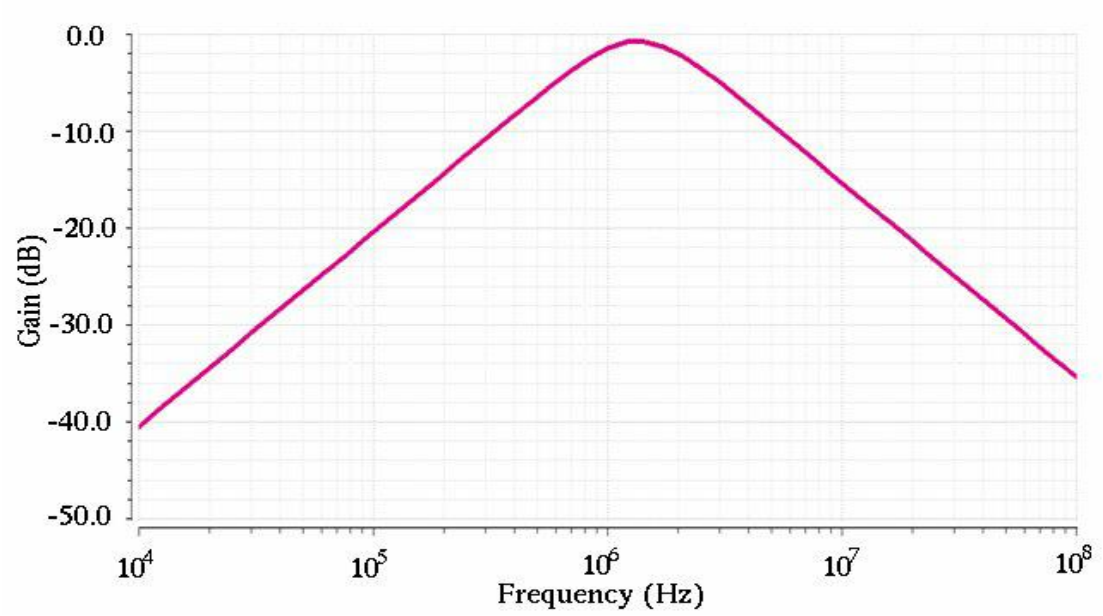


Fig.4.7: Frequency response of BPfilter

The pole frequency and BW of the proposed filter for the selected passive components are 1.34MHz and11.95MHz respectively. Thus, the experimental results confirm the validity of the biquad filter configuration.

CHAPTER 5

ANALYSIS OF MIXED MODE BIQUAD FILTER

5.1 ANALYSIS OF VOLTAGE MODE FILTER

The proposed voltage mode filter configuration is shown in Fig.5.1. The filter structure consists of two VDIBA, two capacitors only. It has five inputs (two for current and three for voltage) and two output ports (voltage). The filter configuration works in voltage mode.

The circuit has the capability to realize all the filter functions in inverting and non-inverting forms and also possess low impedance at output which is essential for cascadability in voltage mode circuits. In addition, the circuit parameters such as natural frequency and BW can be independently controlled electronically. The circuit works in Voltage mode and can realize simultaneously all filter functions, i.e .LP, HP, BP, BR and AP without changing the circuit configuration.

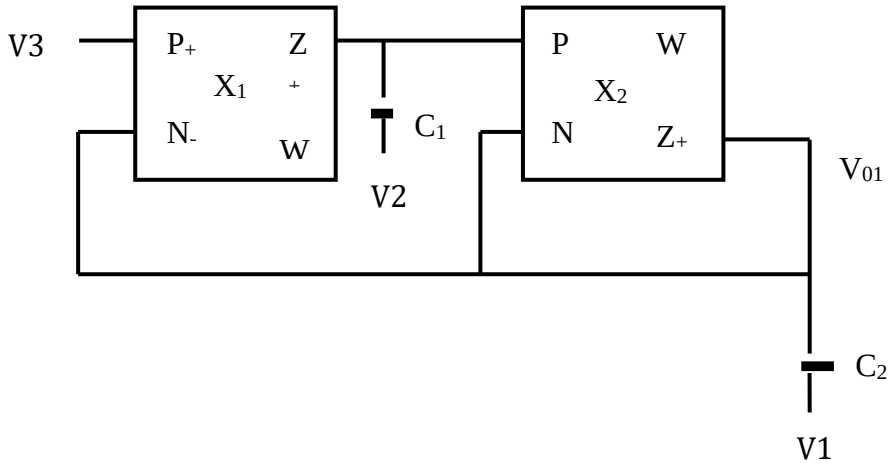


Fig 5.1: Proposed VM biquad filter

$$V_O = \frac{s^2 V_1 + s\frac{g_{m_2} V_2}{C_2} + \frac{g_{m_1} g_{m_2} V_3}{C_1 C_2}}{s^2 + s\frac{g_{m_2}}{C_2} + \frac{g_{m_1} g_{m_2}}{C_1 C_2}} \quad (5.1$$

From Eqn. (5.1) the second order mixed mode universal filter transfer functions are obtained according to input voltage or current conditions. For all filter responses the bandwidth, resonance angular frequency (ω_o) and quality factor (Q) can be expressed from the denominator are given by

$$w_O = \sqrt{\frac{g_{m_1} g_{m_2}}{C_1 C_2}} \quad (5.2)$$

$$BW = \frac{g_{m_2}}{C_2} \quad (5.3)$$

$$Q = \sqrt{\frac{g_{m_1} C_2}{g_{m_2} C_1}} \quad (5.4)$$

It can be seen from Eqn.(5.1) that the proposed filter realizes all the filter functions from the same topology. Table5.1 shows realization condition of all the filter functions for various combinations of input variables.

Table 5.1: Input set for different filter functions

S.NO.	INPUT	FILTER FUNCTION
1	$V_1=V_2=0$, $V_3=V_{in}$	LP
2	$V_2=V_3=0$, $V_1=V_{in}$	HP
3	$V_1=V_3=0$, $V_2=V_{in}$	BP
4	$V_2=0$, $V_1=V_3=V_{in}$	BR
5	$V_1=V_2=V_3=V_{in}$	AP

5.1.1 Performance Results

The functionality of proposed configuration has been checked by using tanner at 180nm technology. The DC power supply voltage used for CMOS VDIBA is 0.9V. The transistor dimensions of the OTA for M1-M4 and the IVB for M5 and M6 has been taken as $W/L_{(M1-M4)}=18\mu m/1.08\mu m$ and $W/L_{(M5,M6)}=54\mu m/0.18\mu m$ respectively. The bias current have been selected as $I_b=100\mu A$. The capacitance values C_1 and C_2 are taken as 10pf and 5pf respectively.

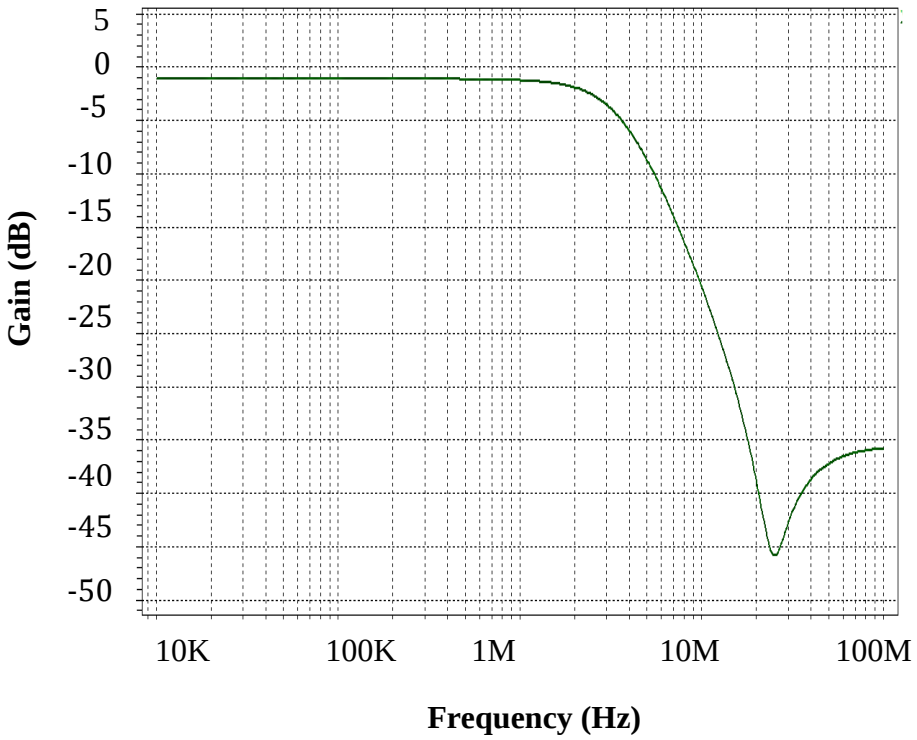


Fig.5.2: Frequency response of LP filter

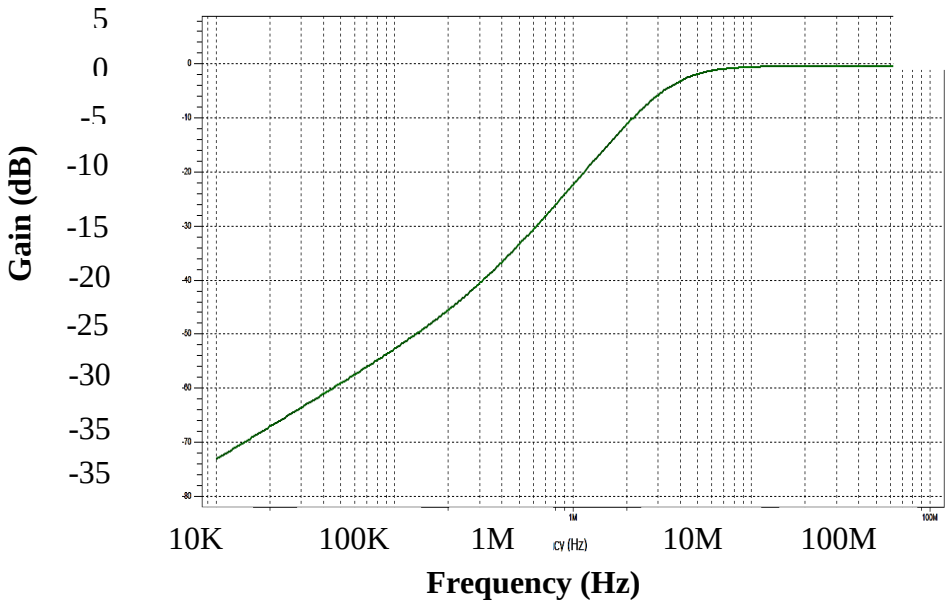


Fig.5.3: Frequency response of HP filter

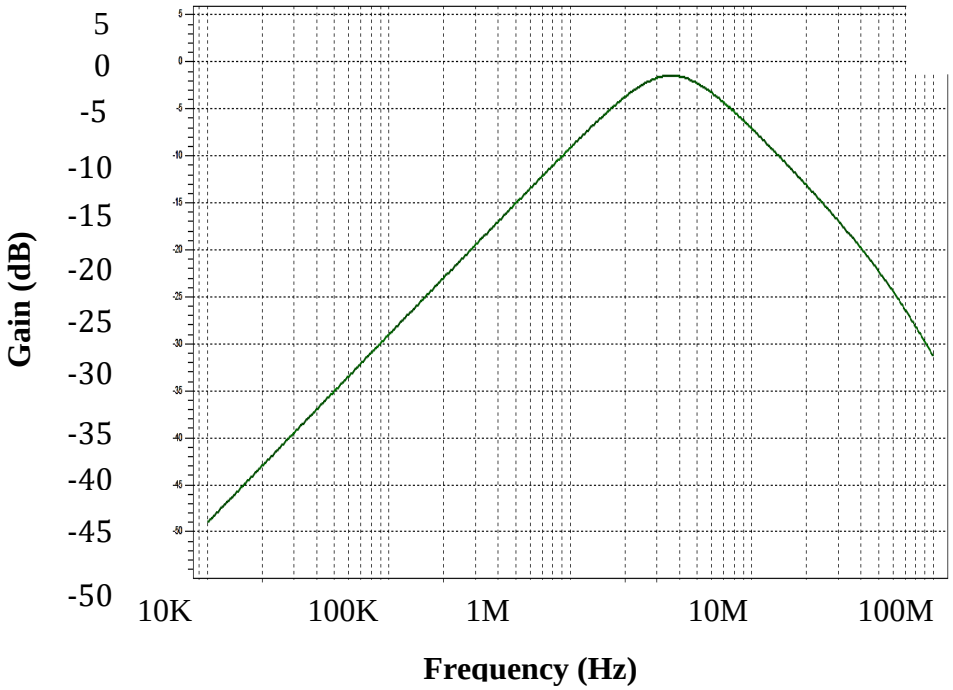


Fig.5.4: Frequency response of BP filter

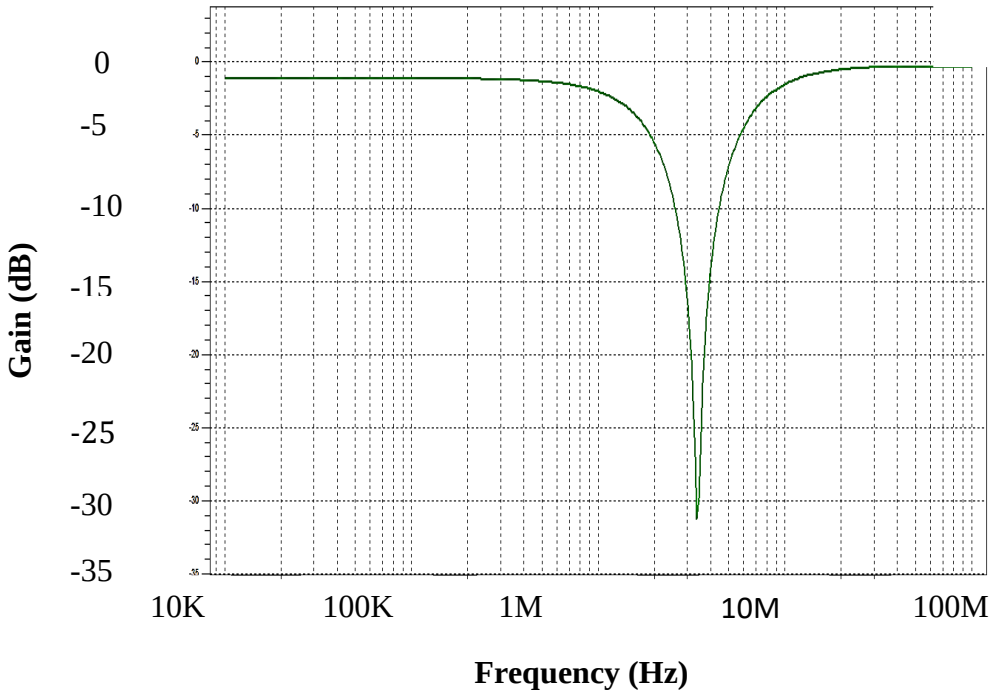


Fig.5.5: Frequency response of BR filter

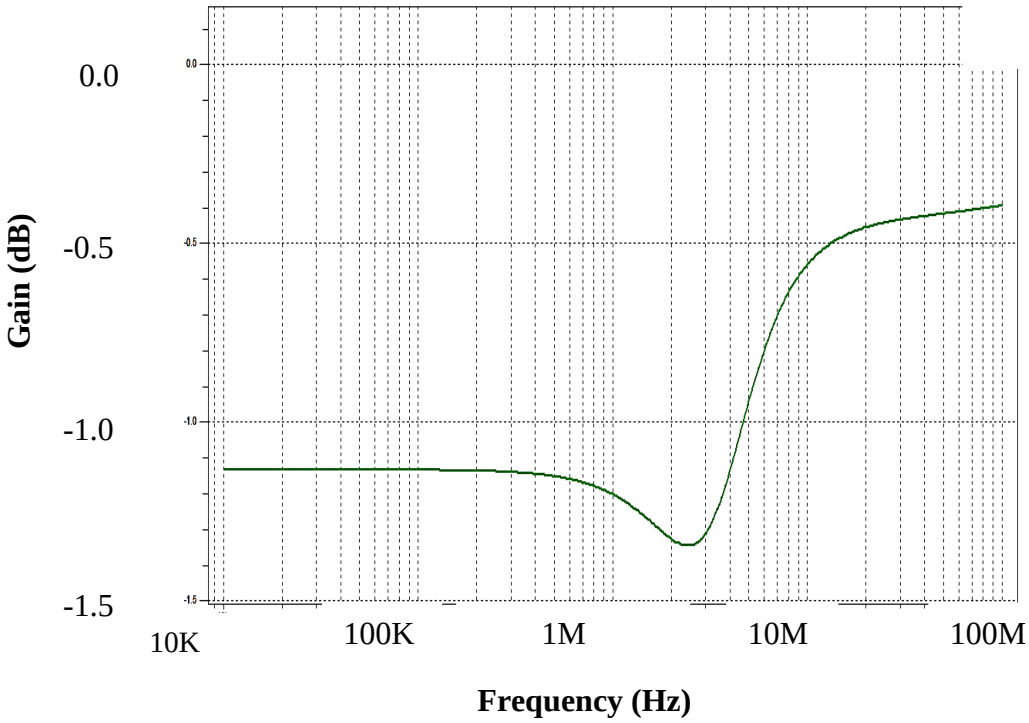


Fig.5.6: Frequency response of AP filter

Fig.5.2, 5.3, 5.4, 5.5, and 5.6 shows the frequency response of LP, HP, BP, BR and AP of proposed VM universal filter.

5.2 FREQUENCY VARITION WITH BIAS CURRENT (I_b)

The functionality of proposed configuration has been checked by using tanner at 180nm technology. The DC power supply voltage used for CMOS VDIBA is 0.9V. The bias currents have been selected as $I_b = 1\mu A$. The value of passive components C_1 and C_2 are taken as 10pf and 5pf respectively. The VM are controlled by the bias current of the VDIBA Fig. 4.13 shows the filter responses of LP, HP, BP, BR and AP. of proposed VM universal filter values. The choice of component results in f_o = 546.09KHz.

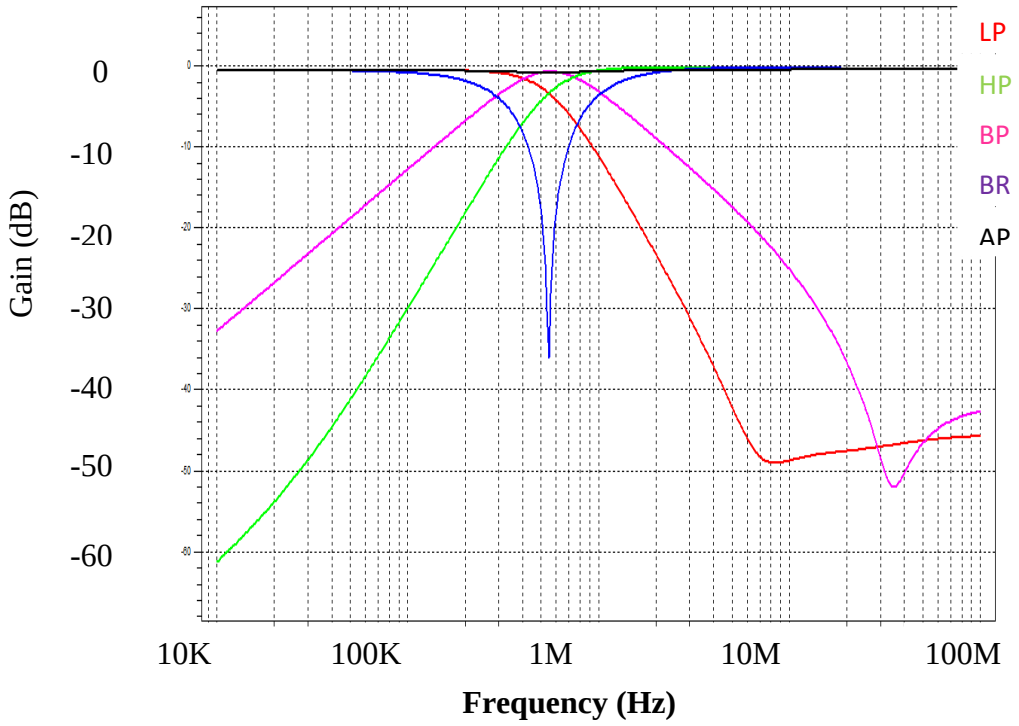


Fig.5.7: Frequency response of filter atI_b=1μA

At I_b=50μA the frequency is 3.19MHz.

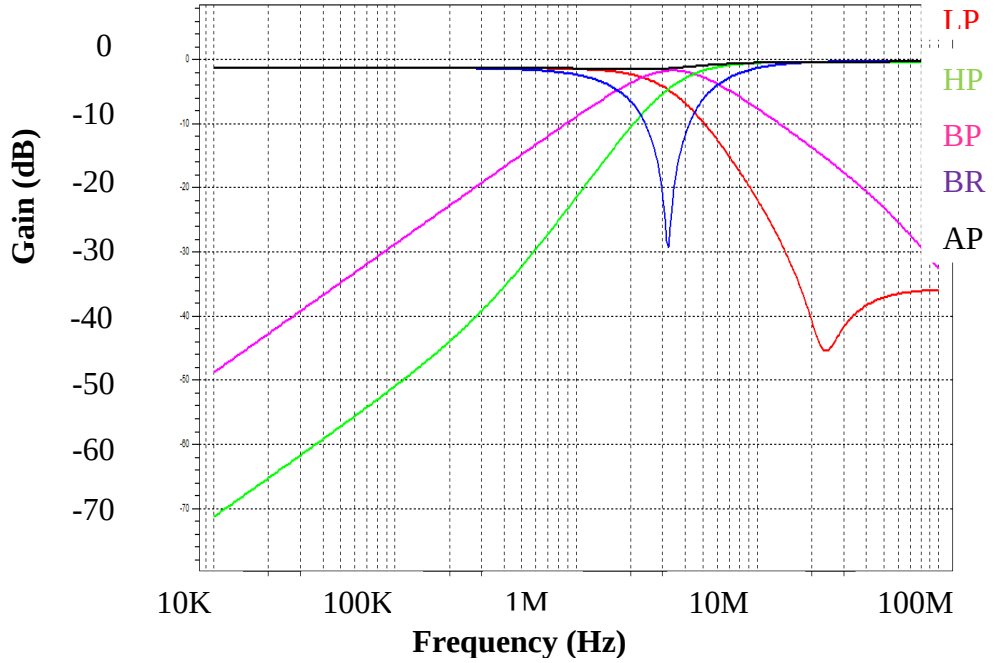


Fig.5.8: Frequency response of filterat I_b=50μA

At I_b=100μA the frequency is 3.41MHz.

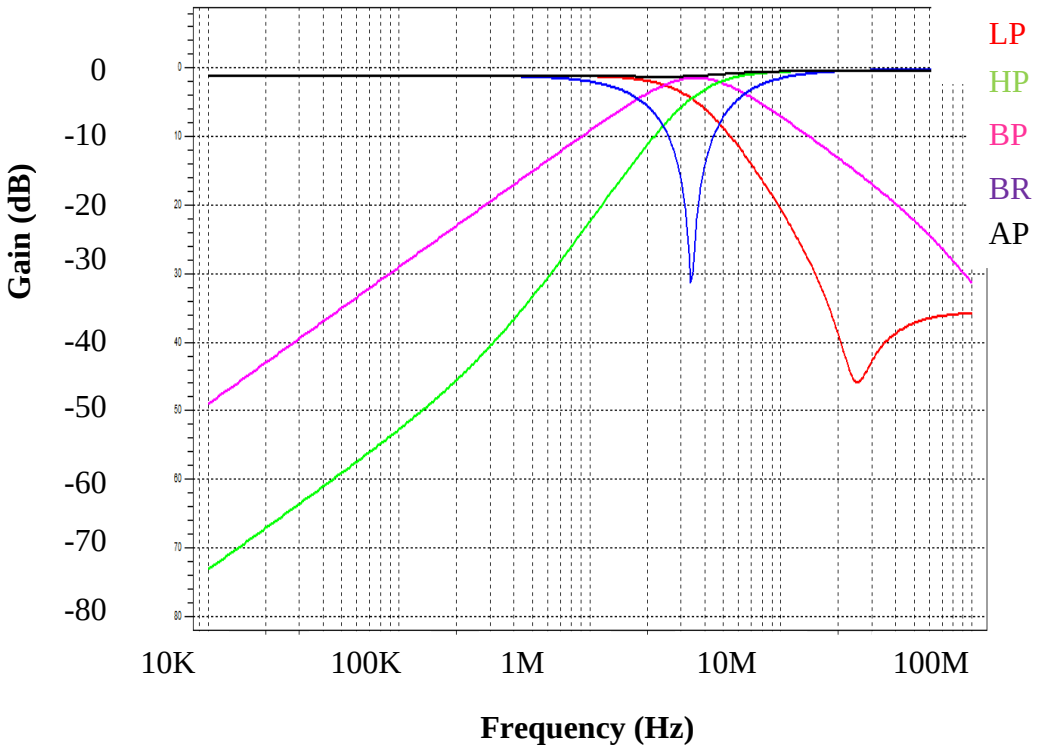


Fig. 5.9: Frequency response of filter atI_b=100μA

At I_b=150μA the frequency is 3.53MHz.

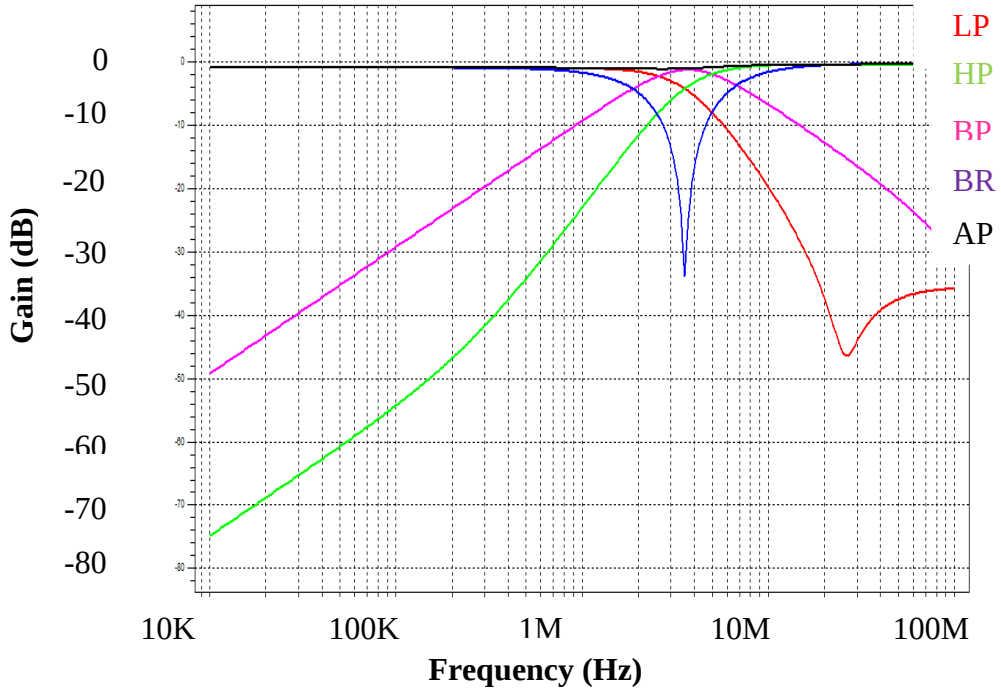


Fig.5.10: Frequency response of filter atI_b =150μ

At I_b =200μA the frequency is 3.71MHz

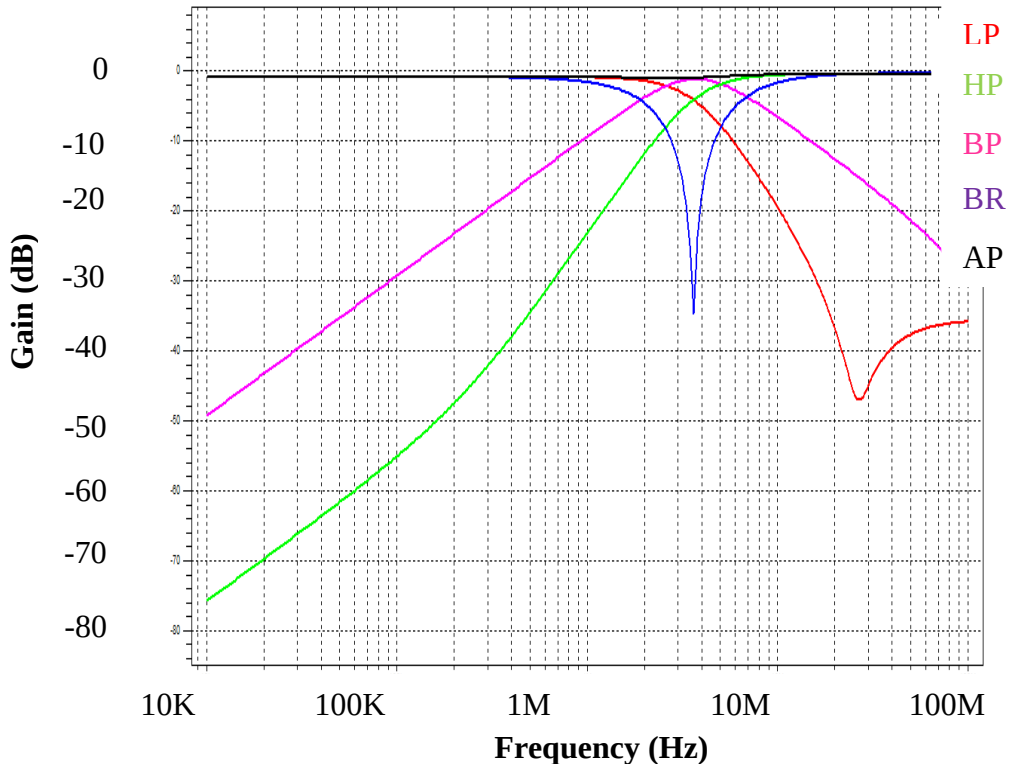


Fig.5.11: Frequency response of filter atI_b =200μA

5.3. POWER DISSIPATION IN CMOS CIRCUITS

5.3.1. Objectives

The following goals have been formulated for this work:

(a) Motivation
(b) Effect of Power Dissipation
(c) How to Reduce Temperature
(d) Components of Power Dissipation
(e) Static Power Dissipation
(f) Dynamic Power Dissipation
(g) Methods to Reduce Power Dissipation
(h) Short-Circuit Power Dissipation

5.3.1.1. Motivation

Why is power dissipation so important? Power dissipation considerations have become important not only from reliability point of view, but they have assumed greater

importance by the advent of portable battery driven devices like laptops, cell phones, PDAs etc.

5.3.1.2. Effects of Power Dissipation

When power is dissipated, it invariably leads to rise in temperature of the chip. This rise in temperature affects the device both when the device is off as well as when the device is on.

When the device is off, it leads to increase in the number of intrinsic carriers, by the following relation:

$$n_i \propto e^{\frac{-\dot{E}g}{KT}} \qquad (5.5)$$

From this relation it can be seen that as temperature increases, it leads to increase in the number of intrinsic carriers in the semiconductor. The majority carriers, contributed by the impurity atoms, are less affected by increase in temperature. Hence the device becomes more intrinsic.

As temperature increases, leakage current, which directly depends on minority carrier concentration, increases which leads to further increase in temperature. Ultimately, the device might break down, if the increase in temperature is not taken care of by time to time removal of the dissipated heat.

An ON device won't be affected much by minority carrier increase, but will be affected by V_T and μ which decrease with increase in temperature and lead to change in I_D. Hence the device performance might not meet the required specifications. Also, power dissipation is more critical in battery powered applications as the greater power dissipated, the battery life will be.

5.3.1.3. How to Reduce Temperature

The heat generated due to power dissipation can be taken away by the use of heat sinks. A heat sink has lower thermal resistance than the package and hence draws heat from it. For the heat to be effectively removed, the rate of heat transfer from the area of heat generation to the ambient should be greater than the rate of heat generation. This rate of heat transfer depends on the thermal resistance.

The thermal resistance, θ is given by the following relation:

$$\theta = \frac{\dot{l}}{\sigma_c A} \tag{5.6}$$

Where,
l = length,
A = Area and
σ_c= thermal conductivity of the heat sink

$$\theta = \frac{\dot{\delta T}}{\delta P} \tag{5.7}$$

Using this relation, we can see that for a given power dissipation, P_D

$$\theta \leq \frac{(\dot{T_J} - T_a)}{P_D} \tag{5.8}$$

Where,
Tj= junction temperature, and
Ta= ambient temperature.
Heat sink materials are generally coated black to radiate more energy

5.3.1.4. Components of Power Dissipation

Unlike bipolar technologies, here a majority of power dissipation is static, the bulk of power dissipation in properly designed CMOS circuits is the dynamic charging and discharging of capacitances. Thus, a majority of the low power design methodology is dedicated to reducing this predominant factor of power dissipation.

There are three main sources of power dissipation:

(a) Static power dissipation (PS)
(b) Dynamic power dissipation (DS)
(c) Short circuit power dissipation (PSC)

Thus the total power dissipation, P_D, is

$$P_D = P_S + P_D + P_{SC} \tag{5.9}$$

5.3.1.5. Static Power Dissipation

Consider the complementary CMOS gate, shown in Figure 5.12

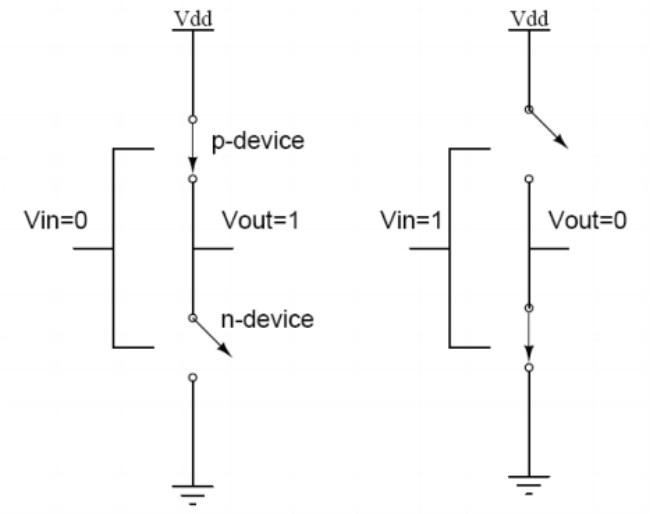


Fig 5.12: CMOS inverter model for static power dissipation evaluation

When input = '0', the associated n-device is off and the p-device is on. The output voltage is V_{DD} or logic '**1**'. When the input ='**1**', the associated n-device is on and the p-device turns off. The output voltage is '0' volts or V_{SS}. It can be seen that one of the transistors is always off when the gate is in either of these logic states. Since no current flows into the gate terminal, and there is no DC current path from V_{DD} to V_{SS}, the resultant quiescent (steady-state) current, and hence power P_S, is zero.

However, there is some small static dissipation due to reverse bias leakage between diffusion regions and the substrate. In addition, sub threshold conduction can contribute to the static dissipation. A simple model that describes the parasitic diodes for a CMOS inverter should be looked at in order to have an understanding of the leakage involved in the device. The source-drain diffusions and the n-well diffusion form parasitic diodes. In the model, a parasitic diode exists between n-well and the substrate. Since parasitic diodes are reverse biased, only their leakage current contributes to static power dissipation. The leakage current is described by the diode equation:

$$\dot{i_0} = \dot{i_s}(e^{\frac{\dot{qv}}{KT}} - 1) \qquad (5.10)$$

Where,
i_s= reverse saturation current
V = diode voltage
q = electronic charge
k = Boltzmann's constant
T = temperature

static power dissipation is the product of the device leakage current and supply voltage:

$$P_S = i_{leakage} * V_{DD} \quad (5.11)$$

5.3.1.6. Dynamic Power Dissipation

During switching, either form '0' to '1' or, alternatively, form '1' to '0', both N-type and P-type transistors are on for a short period of time. This result in a short current pulse from V_{DD} to V_{SS}. Current is also required to charge and discharge the output capacitive load. This latter half is usually the dominant position. The current pulse from V_{DD} toV_{SS} results in a 'short-circuit' loss depending on the input rise/fall time, load capacitance and gate design.

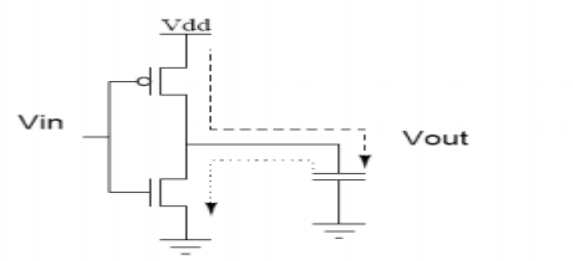


Fig 5.13: Power dissipation due to charging/discharging of capacitor

dynamic dissipation can be performed by assuming that the rise and fall time of the step input is less than the repetition period. The average dynamic power, P_D, dissipated during switching for a square-wave input, Vin, having a repetition frequency $f_p=1/t_p$, is given by:

$$\dot{P_D} = \frac{1}{t_p}\int_0^{\frac{t_p}{2}} i_n(t)\dot{V_{out}}dt + \frac{1}{t_p}\int_{\frac{t_v}{2}}^{t_v} i_p(t)(v_{dd} - \dot{v_{out}})dt \quad (5.12$$

Where
In=n-device transient current
Ip=p-device transient current

$$\dot{i_n}(t) = C_L\frac{d\dot{V_{out}}}{dt} \quad (5.13)$$

For a step input and with

$$\dot{P_D} = \frac{\dot{C_L}}{t_p}\int_0^{V\infty} V_{out}d\dot{V_{out}} + \frac{\dot{C_L}}{t_p}\int_{V\infty}^{0} (V_{DD} - V_{out})\dot{d}(\dot{V_{DD}} - \dot{V_{out}}) \quad (5.14$$

(5.15)

$$P_D = \frac{C_L V_{DD}^2}{t_p}$$

With

$$f_p = \frac{1}{t_p} \qquad (5.16$$

Resulting in

$$P_D = C_L V_{DD}^2 f_P \qquad (5.17)$$

Similarly for a repetitive step input, the average power that is dissipated is proportional to the energy required to charge and discharge the circuit capacitance. The important factor to be noted here is that eq 5.17 shows power to be proportional to switching frequency but independent of device parameters. The power dissipation also depends on the switching activity (α) .

The equation can be written as

$$P_D = C_L V_{DD}^2 f_P \qquad (5.18$$

5.3.1.7. Methods to Reduce Dynamic Power Dissipation:

As can be seen from Eq (5.18), the power dissipated can be reduced by reducing either the clock frequency, f_p, or the load capacitance, C_L, or the rail voltage, V_{DD}, or the switching activity parameter, α. Reducing the clock frequency is the simplest thing to do, but it seriously affects the performance of the chip. Applications where power is supreme, this approach can be used satisfactorily. Another method to reduce the dissipated power is to lower the load capacitance, C_L. But this method is more difficult than the previous approach because it involves dutiful system design, so that there are fewer wires, smaller pins, smaller fan-out, smaller devices and so on .

Power dissipation can also be reduced by reducing the rail voltage, V_{DD} . But this can only be done by device technology. Also rail voltage is agreed standard in most cases by the semiconductor industry, so we do not have much control over this parameter. Also rail voltage is strongly dependent on the threshold voltage and the noise margin.

Some special techniques are also used to reduce power dissipation. The first one involves the use of pipelining to operate the internal logic at a lower clock than the i/o frequency. The other technique is to reduce switching activity, α, by optimizing algorithms, architecture, logic topology and using special encoding techniques.

5.3.1.8. Short-Circuit Power Dissipation:

The short-circuit power dissipation is given by

$$P_D^{\cdot} = I_{mean}^{\cdot} * V_{DD}^{\cdot} \quad (5.19$$

5.4. IMPLEMENTATION AND ANALYSIS

In this phase simulation of the VDIBA will be carried out in Tanner tool. The results obtained from the simulations will be analyzed and different parameters will be calculated:

Table.5.2 Comparison Table of Base Paper and Proposed Work

Parameter	Base paper[1]	Proposed Work	Achieved Results
No. of filter function	All filter function	Universal filter	All filter function
No. of capacitance	2	2	2
No. of resistance	1	1	0
Frequency	1.34MHz	1.34-2.40MHz	547.09KHz-3.65MHz
Bandwidth	11.95MHz	11.95-15.00MHz	15MHz
Total power dissipation	10.5Mw	10.0-10.5mW	.489mW-
Power supply	0.9V	0.9-0.8V	0.9V

CHAPTER6

CONCLUSION AND FUTURE SCOPE

6.1 CONCLUSION

From the last decade, a huge number of active building blocks have been introduced in the field of analog signal processing. The newly introduced VDIBA block has been realized. This block is equipped with tenability feature through their transconductance parameters and also, the circuit based over it doesnot require a passive resistor. The circuits based over these blocks occupy the lesser area because of their low component count. Moreover, the current mode processing of these blocks results in simpler circuit structures. Thus, the use of these blocks results in optimized and high performance circuits. The functionality of VDIBA block has been confirmed byDC and AC analysis.

Several filter circuits based on VDIBA have been analyzed and simulated by using the Tanner tool at CMOS 180nm process parameters. The proposed filter configuration offers the following features.

(a) Availability of universal filtering function simultaneously from the same configuration.
(b) Orthogonaladjustmentofthenaturalangularfrequencyandthequalityfactorbyelectronic means.
(c) Does not require critical component matching constraints in the design.
(d) Employs only grounded capacitors which are ideal for integration.
(e) Provide high bandwidth.
(f) Ensure cascadability.

6.2 FUTURE SCOPE

A number of novel circuit functions such as amplifier, integrator, summer, differentiator, etc. and topologies have been explored on a front of analog signal processing circuits. This work can be further extended by minimizing the parasitic effects so that the bandwidth of the respective filter can be increased.

REFERENCES

[1] K.L.Pushkar, D.R.Bhaskar, Dinesh Prasad, 2013, "Voltage mode new universal biquad filter configuration using a single VDIBA", *Circuits Syst Signal Process–springer,* Vol. 33, pp. 275–285.

[2] Norbert Herencsar, Oguzhan Cicekoglu, Roman Sotner, Jaroslav Koton, Kamil Vrba, 2013, "New resistorless tunable voltage-mode universal filter using single VDIBA", *Analog Integr Circ Sig Process–springer,*Vol. 76 pp.251–260.

[3] Jetsdaporn Satansup, Tattaya Pukkalanum,Worapong Tangsrirat, 2013, "Electronically tunable single-inputfive-output voltage mode universal filter using VDTA and grounded passive elements", *Circuits Syst Signal Process –springer,* Vol. 27, pp .673–682.

[4] Abdullah Yesil, Firat Kacar, Hakan Kuntman, 2011, "New simple CMOS realization of voltage differencing transconductance amplifier and its RF filter application" , *Radioengineering,*Vol.20, pp. 632-637.

[5] Dinesh Prasad, Data Ram Bhaskar, Mayank Srivastava, 2013, "Universal current-mode biquad filter using a VDTA", *Circuits and Systems,* Vol. 4, pp.29-33.

[6] Jetsdaporn Satansup, Worapong Tangsrirat, 2014, "Compact VDTA based current mode electronically tunable universal filters using grounded capacitors", *Miecro electronics journal-elsevier,*Vol. 45, pp.613-618.

[7] Wilas Ninsraku, Dalibor Biolekb, Winai Jaiklad, Surapong Siripongdee, Peerawut Suwanjan, 2014, "Electronically controlled high input and low output impedance voltage mode multi function filter with grounded capacitors" , *Int.J.Electron.Commun.–Elsevier,*Vol.68,pp. 1239-1246.

[8] Norbert Herencsar, Jaroslav Koton, and Kamil Vrba, 2009, "Single CCTA–based universal biquadratic filters employing minimum components", *International Journal of Computer and Electrical Engineering,* Vol. 1,pp. 307-310.

[9] Suwat Maneewan, Nawee Udorn, Danupat Duangmalai, Phamorn Silapan, Winai Jaikala, 2014, "A voltage-mode first order all pass filter based on VDTA", *Theoretical And Applied Electrical Engineering,*Vol. 12, pp.40-46.

[10] Norbert Herencsar, Jaroslav Koton, Shahram Minaei, Erkan Yuce, and Kamil Vrba, 2013, "Novel resistorless and electronically tunable realization of dual-output VM All-Pass Filter using VDIBA", *Analog Integr Circ Sig Process–springer,* Vol.74 , pp.141–154.

[11] Jaroslav Koton, Norbert Herencsar, Kamil Vrba, Bilgin Metin, 2014, "Voltage-mode multi function filter with mutually independent Q and ω control feature using VDDDAs", *Analog Integr Circ Sig Process– springer* ,Vol. 81, pp.53–60.

[12] Yan-hui Xi1LiLiu, 2008, "A Novel CMOS Current Controlled Conveyor II and Its Applications", *International Conference on Intelligent Computation Technology and*

Automation, Vol. 23, pp. 7-10.

[13] Chang,Chun-Ming, Chang Yuan, Chung-Li, Ming-Jye Lee, 1999, "Voltage-mode multi function filter with single input and three outputs using two compound current conveyors", *IEEE Transactionson Fundamental Theory and Applications, Circuits and Systems I* ,Vol.46, pp. 1364-1365.

[14] Jiun-Wei Horng, Chun-LiHou, Wei-Shyang Huang, Dun-YihYang, 2011."Voltage/Current-Mode Multifunction Filters Using One Current Feedback Amplifier and Grounded Capacitors", *Circuits and Systems- Sceintific research*, 2011, Vol.2, pp. 60-64.

[15] Nissar Ahmad Shah, Mohmad Amin Malik, 2006 "Multi function mixed-mode filter using FTFNs, *Analog Integrated Circuits and Signal Processing*",Vol. 47, Issue 3, pp.339-343.

[16] Manish kumar, M.C. srivastava, Umesh Kumar,2010, "Current Conveyor Based Multifunction Filter", *International Journal of Computer Science and Information Security, (IJCSIS)*, Vol.7, pp.105-107.

[17] Nisar A. Shah, Munazah Quadri, Syed Z. Iqbal, 2007, "CDTA based universal transadmittance filter", *Analog Integr Circ Sig Process–springer*, Vol.52, pp.65-69.

[18] Nisar Ahmad Shah, Syed Zaffer Iqbal, Basharat Parveen, 2005, "Low pass and band pass transadmittance filter using operational amplifier pole", *Int. J. Electron. Commun.–Elsevier,*Vol. 59, pp. 410-412.

[19] C.M.Chang, B.M.Al-Hashimi, J.N.Ross, 2004, "Unified active filter biquad structures", *IEEEProc. - Circuits, Devices and Systems,*Vol. 151,pp. 273 –277.

[20] Alain Fabre, Naamane Mimeche, 1996, "Insensitive voltage-mode and current-mode filters with easily modifiable transfer functions", *Analog Integrated Circuit and Signal Procesings–springer,*Vol.11, pp.253–264.

[21] Nikhil Raj, Ranitesh Gupta, Vikram Chopra, 2010, "A Low Voltage High Performance OTA in 0.18 Micron with High Linearity" ,*Analog Integrated Circuit and Signal Processings–springer,*Vol.90, pp.712–721.

[22] Fırat Kacar, Abdullah Yesilland Abbas Noori, 2012, "New CMOS Realization of Voltage Differencing Buffered Amplifier and Its Biquad Filter Applications", *Radio engineering*, Vol.21, pp.333-339.

[23] Jiun-Wei Horng, 2004, "Voltage-Mode Universal Biquadratic Filter Using Two OTAs", *Active And Passive Elec. Comp.,*Vol. 27, pp. 85–89.

[24] Milad Razzaghpour , Abbas Golmakani, 2008,"An Ultra-Low-Voltage Ultra-Low-Power OTA with improved gain-bandwidth product", *International Conference on Micro electronics*, Vol.3, pp.1-4.

[25] Chunhua Wang, Haiguang Liu, YanZhao, 2008, "A New Current-ModeCurrent-Controlled Universal Filter Based on CCCII(±), *Circuits System Signal Processing* ,Vol.27,pp.673–682.

[26] Nattapong Thongjan, Chaiya Tanaphatsiri, Montree Siripruchyanun, 2009, "CCCII-based High Input-impedanceCurrent-Mode Universal Filter and Quadrature Oscillator", *The Seventh PSU Engineering Conference,* Vol. 23,pp. 250-253.

[27] Muhammed A. Ibrahim, 2008, "Design and Analysis of a Mixed-Mode Universal Filter Using Dual-Output Operational Transconductance Amplifiers (DO-OTAs)", *Proceedings of the International Conference on Computer and Communication Engineering,* Vol. 9,pp. 915-918.

[28] Li Zhijun, 2009, "Mixed-mode universal filter using MCCCII**",** *International Journal of Electronics Communication (science direct),* Vol.63,pp. 1072-1075.

[29] Nadhmia Bouaziz ElFeki, Dorra Sellami Masmoudi, 2009, "High Performance Dual-Output Second and Third Generation Current Conveyors and Current-Mode Multi function Filter Application", *International Multi-Conference on Systems, Signals and Devices,*Vol.33,pp. 201-206.

[30] Jiun-Wei Horng, 2004, "Voltage-Mode Universal Biquadratic Filter Using Two OTAs", *Active And Passive Elec. Comp.,*Vol. 27, pp. 85–89.

[31] Sajai Vir Singh, Sudhanshu Maheshwari, Durg Singh Chauhan, 2011, "Single MO-CCCCTA-Based Electronically Tunable Current/Trans-Impedance-Mode Biquad Universal Filter", *Circuits and Systems,* Vol.2, pp. 1-6.

[32] Hua-Pin Chen, Yi-Zhen Liao, Wen-Ta Lee, 2009, "Tunable mixed-mode OTA-C universal filter", *Analog Integr Circ Sig Process –springer,* Vol. 58, pp. 135-141

[33] Sajai Vir Singh, Sudhanshu Maheshwari, Durg Singh Chauhan, 2010,"Universal Current-Controlled Current-Mode Biquad Filter Employing MO-CCCCTAs and Grounded Capacitors", *Circuits and Systems,* Vol. 01, pp.35-40.

[34] Muhammad Taher Abuelma'atti & Abdulwahab Bentrcia, 2013, "A novel mixed-mode OTA-C universal Filter", *International Journal of Electronics,* Vol. 92, pp. 375-383.

[35] Chetan Chauhan, Ravindra Tomar, S.V.Singh, D.S. Chauhan, 2013, "Current Controlled Current-Mode SITO Biquad Universal Filter Using CCTAs", *Conference on Advancesing Communication and Control Systems,* Vol.5,pp. 297-301.

[36] Neeta Pandey, Sajal K. Paul, 2010, "SIMO Transadmittance Mode Active-C Universal Filter", *Circuits and Systems,* Vol. 1, pp. 54-58.

[37] Supachai Klungtong, Dusit Thanapatay, and Winai Jaikla, 2017, "Three-Input Single-Output Voltage-Mode Multi function Filter with Electronic Controllability Based on Single Commercially Available IC", *Active and Passive Electronic Components,* Vol. 2017,pp. 1-10.

[38] Neelofer Afzal and Devesh Singh, 2014, "Reconfigurable Mixed Mode Universal Filter", *Active and Passive Electronic Components,* Vol. 14, pp. 1-14.

[39] Jiun-Wei Horng, Chang-Ming Wu & Norbert Herencsar, 2014, "Three-input-one-output current-mode universal biquadratic filter using one differential difference current conveyor", *Indian Journal of Pure & Applied Physics,* Vol. 52, pp. 556-562.

[40] Ninar Ahmad Shah and Mohamed Amin Malik, 2004, "Voltage/Current-Mode Universal Filter Using FTFN and CFA", *Analog Integrated Circuits and Signal Processing,* Vol. 45, pp. 197-203.

[41] J. K. Pathak, A. K. Singh, and Raj Senani, 2013, "New Voltage Mode Universal Filters Using Only Two CDBAs", *Hindawi Publishing Corporation,* Vol. 2013, pp. 1-6.

[42] C. M. Chen, 2006, "Universal voltage-mode filter using only plus-type DDCCs", *Analog Integr Circuit Sig Process,* pp. 137-139.

[43] Wei-Yuan Chiu and Jiun-Wei Horng, 2011, "High input and low output impedance voltage mode universal biquired filter using DDCCs", *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS,* Vol. 54.

[44] Kanhaiya Lal Pushkar, Data Ram Bhaskar, Dinesh Prasad, 2013, "Voltage-Mode Universal Biquad Filter Employing Single Voltage Differencing Differential Input Buffered Amplifier", *Circuits and Systems,* Vol. 2013, pp44-48.

[45] Khachen Khawngam, Montree Kumngern, Fabian Khateb, 2017, "Mix Mode Third-Order Quadrature Oscillator Based on Single MCCFTA", *Radio engineering,* Vol. 26, PP. 522 533.

[46] Surasak Sangyaem, Surapong Siripongdee, Winai Jaikla, Fabian Khateb, 2017, "Five-inputs single-output voltage mode universal filter with high input and low output impedance using VDDDAs", *Elsevier Gmbh,* Vol. 2016, pp 14-25.

[47] Norbert Herencsar, Oguzhan Cicekoglu, 2013, "New resistorless tunable voltage- mode universal filter using single", *Analog Integr Circ Sig Process* Vol.(2013), pp. 251–260.

[48] Jiun-Wei Horng, Guang-Ting Huang, 2013, "A Grounded Capacitor Differentiator Using Current Feedback Amplifier", *Circuits and Systems,* Vol. 2013, pp. 233-236.

[49] Worapong Tangsrirat, Orapin Channumsin*, 2011, "*High-Input Impedance Voltage-Mode Multifunction Filter Using a Single DDCCTA and Grounded Passive Elements", *Radio engineering,* Vol. 20, pp. 905-910.

[50] Pipat Prommee, Aphinat Tiamsuphat, Muhammad Taher Abuelma , 2017, "Electronically tunable MOS-only current-mode high-order band-pass filters", *Turkish Journal of Electrical Engineering & Computer Sciences,* Vol. 25, pp. 1116-1136.

[51] Hua-Pin Chen, 2014, "Voltage-Mode Multifunction Biquadratic Filter with One Input and Six Outputs Using Two ICCIIs", *Hindawi Publishing Corporation,* Vol.2014, pp. 1-7.

[52] Jitendra Mohan, Bhartendu Chaturvedi, and Sudhanshu Maheshwari, 2014, Single Active Element Based Voltage-Mode Multifunction Filter", *Hindawi Publishing Corporation,* Vol.2014, pp.1-7.

[53] Mohd. Usama Ismail and Bilal Arif, 2014, "Single Input Multi Output Digitally Reconfigurable Biquadratic Analog Filter", *IEEE,* pp.201-206.

[54] Roman Sotner, Josef Slezak, Josef Slezak and Jirı Petrzela, 2010, "universal tunable current–mode biquad employing distributed feedback structure with MO–CCCII", *Journal of Electrical engineering,* VOL. 61, pp.52–56.

APPENDIX 1

1.1 Analysis of LPF programming.

T-Spice - Tanner SPICE
Version 13.00
Standalone hardware lock
Product Release ID: T-Spice Win32 13.00.20080321.01:01:33


```
*
V1 5 0 AC 0
V2 4 0 AC 0
V3 2 0 AC 0.1
C1 3 4 10P
C2 1 5 5P
X1 2 1 3 10 VDIBA
X2 3 1 1 11 VDIBA


.SUBCKT VDIBA  5   6  7  8
 *           VP VN IZ VW
*V3 11 0 AC 0.1
*V1 12 0 AC 0
*V2 6 0 AC 0
*VP=5, VN=6, IZ=7, VW=8
*V2 7 0 DC 0
*vp 5 0 ac .1
*vn 6 0 ac -.1
IB 4 2 DC 100U
M1 3 5 4 4 NMOS W=18U L=1.08U
M2 7 6 4 4 NMOS W=18U L=1.08U
M3 3 3 1 1 PMOS W=18U L=1.08U
M4 7 3 1 1 PMOS W=18U L=1.08U
M5 1 1 8 8 NMOS W=54U L=0.18U
M6 8 7 2 2 NMOS W=54U L=0.18U
*C1 7 11 25P
*C2 5 12 10P
*R1 5 8 1.67K
```

```
.MODEL NMOS NMOS (                          LEVEL   = 7
+VERSION = 3.1          TNOM    = 27          TOX     = 4.1E-9
+XJ      = 1E-7         NCH     = 2.3549E17   VTH0    = 0.3725327
+K1      = 0.5933684    K2      = 2.050755E-3 K3      = 1E-3
+K3B     = 4.5116437    W0      = 1E-7        NLX     = 1.870758E-7
+DVT0W   = 0            DVT1W   = 0           DVT2W   = 0
+DVT0    = 1.3621338    DVT1    = 0.3845146   DVT2    = 0.0577255
+U0      = 259.5304169  UA      = -1.413292E-9 UB     = 2.229959E-18
+UC      = 4.525942E-11 VSAT    = 9.411671E4  A0      = 1.7572867
+AGS     = 0.3740333    B0      = -7.087476E-9 B1     = -1E-7
+KETA    = -4.331915E-3 A1      = 0           A2      = 1
+RDSW    = 111.886044   PRWG    = 0.5         PRWB    = -0.2
+WR      = 1            WINT    = 0           LINT    = 1.701524E-8
+XL      = 0            XW      = -1E-8       DWG     = -1.365589E-8
+DWB     = 1.045599E-8  VOFF    = -0.0927546  NFACTOR = 2.4494296
+CIT     = 0            CDSC    = 2.4E-4      CDSCD   = 0
+CDSCB   = 0            ETA0    = 3.175457E-3 ETAB    = 3.494694E-5
+DSUB    = 0.0175288    PCLM    = 0.7273497   PDIBLC1 = 0.1886574
+PDIBLC2 = 2.617136E-3  PDIBLCB = -0.1        DROUT   = 0.7779462
+PSCBE1  = 3.488238E10  PSCBE2  = 6.841553E-10 PVAG   = 0.0162206
+DELTA   = 0.01         RSH     = 6.5         MOBMOD  = 1
+PRT     = 0            UTE     = -1.5        KT1     = -0.11
+KT1L    = 0            KT2     = 0.022       UA1     = 4.31E-9
+UB1     = -7.61E-18    UC1     = -5.6E-11    AT      = 3.3E4
+WL      = 0            WLN     = 1           WW      = 0
+WWN     = 1            WWL     = 0           LL      = 0
+LLN     = 1            LW      = 0           LWN     = 1
+LWL     = 0            CAPMOD  = 2           XPART   = 0.5
+CGDO    = 8.53E-10     CGSO    = 8.53E-10    CGBO    = 1E-12
+CJ      = 9.513993E-4  PB      = 0.8         MJ      = 0.3773625
+CJSW    = 2.600853E-10 PBSW    = 0.8157101   MJSW    = 0.1004233
+CJSWG   = 3.3E-10      PBSWG   = 0.8157101   MJSWG   = 0.1004233
+CF      = 0            PVTH0   = -8.863347E-4 PRDSW  = -3.6877287
+PK2     = 3.730349E-4  WKETA   = 6.284186E-3 LKETA   = -0.0106193
+PU0     = 16.6114107   PUA     = 6.572846E-11 PUB     = 0
+PVSAT   = 1.112243E3   PETA0   = 1.002968E-4 PKETA   = -2.906037E-3   )


*
.MODEL PMOS PMOS (                          LEVEL   = 7
+VERSION = 3.1          TNOM    = 27          TOX     = 4.1E-9
+XJ      = 1E-7         NCH     = 4.1589E17   VTH0    = -0.3948389
+K1      = 0.5763529    K2      = 0.0289236   K3      = 0
+K3B     = 13.8420955   W0      = 1E-6        NLX     = 1.337719E-7
+DVT0W   = 0            DVT1W   = 0           DVT2W   = 0
+DVT0    = 0.5281977    DVT1    = 0.2185978   DVT2    = 0.1
+U0      = 109.9762536  UA      = 1.325075E-9 UB      = 1.577494E-21
+UC      = -1E-10       VSAT    = 1.910164E5  A0      = 1.7233027
+AGS     = 0.3631032    B0      = 2.336565E-7 B1      = 5.517259E-7
+KETA    = 0.0217218    A1      = 0.3935816   A2      = 0.401311
+RDSW    = 252.7123939  PRWG    = 0.5         PRWB    = 0.0158894
+WR      = 1            WINT    = 0           LINT    = 2.718137E-8
+XL      = 0            XW      = -1E-8       DWG     = -4.363993E-8
+DWB     = 8.876273E-10 VOFF    = -0.0942201  NFACTOR = 2
```

```
+CIT     = 0            CDSC    = 2.4E-4        CDSCD   = 0
+CDSCB   = 0            ETA0    = 0.2091053     ETAB    = -0.1097233
+DSUB    = 1.2513945    PCLM    = 2.1999615     PDIBLC1 = 1.238047E-3
+PDIBLC2 = 0.0402861    PDIBLCB = -1E-3         DROUT   = 0
+PSCBE1  = 1.034924E10  PSCBE2  = 2.991339E-9   PVAG    = 15
+DELTA   = 0.01         RSH     = 7.5           MOBMOD  = 1
+PRT     = 0            UTE     = -1.5          KT1     = -0.11
+KT1L    = 0            KT2     = 0.022         UA1     = 4.31E-9
+UB1     = -7.61E-18    UC1     = -5.6E-11      AT      = 3.3E4
+WL      = 0            WLN     = 1             WW      = 0
+WWN     = 1            WWL     = 0             LL      = 0
+LLN     = 1            LW      = 0             LWN     = 1
+LWL     = 0            CAPMOD  = 2             XPART   = 0.5
+CGDO    = 6.28E-10     CGSO    = 6.28E-10      CGBO    = 1E-12
+CJ      = 1.160855E-3  PB      = 0.8484374     MJ      = 0.4079216
+CJSW    = 2.306564E-10 PBSW    = 0.842712      MJSW    = 0.3673317
+CJSWG   = 4.22E-10     PBSWG   = 0.842712      MJSWG   = 0.3673317
+CF      = 0            PVTH0   = 2.619929E-3   PRDSW   = 1.0634509
+PK2     = 1.940657E-3  WKETA   = 0.0355444     LKETA   = -3.037019E-3
+PU0     = -1.0227548   PUA     = -4.36707E-11  PUB     = 1E-21
+PVSAT   = -50          PETA0   = 1E-4          PKETA   = -5.167295E-3   )


VDD 1 0 DC 0.9
VSS 2 0 DC -0.9
.ENDS


.AC DEC 100 10K 100MEG
*.PRINT AC I(V2)
.PRINT AC 'VDB(1)+20'
```

1.2 Analysis of HPF programming.

```
T-Spice - Tanner SPICE
Version 13.00
Standalone hardware lock
Product Release ID: T-Spice Win32 13.00.20080321.01:01:33
Copyright © 1993-2008 Tanner EDA


*
V1 5 0 AC 0.1
V2 4 0 AC 0
V3 2 0 AC 0
C1 3 4 10P
C2 1 5 5P
X1 2 1 3 10 VDIBA
X2 3 1 1 11 VDIBA


.SUBCKT VDIBA  5   6  7  8
 *          VP VN IZ VW
```

```
*V3 11 0 AC 0.1
*V1 12 0 AC 0
*V2 6 0 AC 0
*VP=5, VN=6, IZ=7, VW=8
*V2 7 0 DC 0
*vp 5 0 ac .1
*vn 6 0 ac -.1
IB 4 2 DC 100U
M1 3 5 4 4 NMOS W=18U L=1.08U
M2 7 6 4 4 NMOS W=18U L=1.08U
M3 3 3 1 1 PMOS W=18U L=1.08U
M4 7 3 1 1 PMOS W=18U L=1.08U
M5 1 1 8 8 NMOS W=54U L=0.18U
M6 8 7 2 2 NMOS W=54U L=0.18U
*C1 7 11 25P
*C2 5 12 10P
*R1 5 8 1.67K


.MODEL NMOS NMOS (                      LEVEL   = 7
+VERSION = 3.1          TNOM    = 27            TOX     = 4.1E-9
+XJ      = 1E-7         NCH     = 2.3549E17     VTH0    = 0.3725327
+K1      = 0.5933684    K2      = 2.050755E-3   K3      = 1E-3
+K3B     = 4.5116437    W0      = 1E-7          NLX     = 1.870758E-7
+DVT0W   = 0            DVT1W   = 0             DVT2W   = 0
+DVT0    = 1.3621338    DVT1    = 0.3845146     DVT2    = 0.0577255
+U0      = 259.5304169  UA      = -1.413292E-9  UB      = 2.229959E-18
+UC      = 4.525942E-11 VSAT    = 9.411671E4    A0      = 1.7572867
+AGS     = 0.3740333    B0      = -7.087476E-9  B1      = -1E-7
+KETA    = -4.331915E-3 A1      = 0             A2      = 1
+RDSW    = 111.886044   PRWG    = 0.5           PRWB    = -0.2
+WR      = 1            WINT    = 0             LINT    = 1.701524E-8
+XL      = 0            XW      = -1E-8         DWG     = -1.365589E-8
+DWB     = 1.045599E-8  VOFF    = -0.0927546    NFACTOR = 2.4494296
+CIT     = 0            CDSC    = 2.4E-4        CDSCD   = 0
+CDSCB   = 0            ETA0    = 3.175457E-3   ETAB    = 3.494694E-5
+DSUB    = 0.0175288    PCLM    = 0.7273497     PDIBLC1 = 0.1886574
+PDIBLC2 = 2.617136E-3  PDIBLCB = -0.1          DROUT   = 0.7779462
+PSCBE1  = 3.488238E10  PSCBE2  = 6.841553E-10  PVAG    = 0.0162206
+DELTA   = 0.01         RSH     = 6.5           MOBMOD  = 1
+PRT     = 0            UTE     = -1.5          KT1     = -0.11
+KT1L    = 0            KT2     = 0.022         UA1     = 4.31E-9
+UB1     = -7.61E-18    UC1     = -5.6E-11      AT      = 3.3E4
+WL      = 0            WLN     = 1             WW      = 0
+WWN     = 1            WWL     = 0             LL      = 0
+LLN     = 1            LW      = 0             LWN     = 1
+LWL     = 0            CAPMOD  = 2             XPART   = 0.5
+CGDO    = 8.53E-10     CGSO    = 8.53E-10      CGBO    = 1E-12
+CJ      = 9.513993E-4  PB      = 0.8           MJ      = 0.3773625
+CJSW    = 2.600853E-10 PBSW    = 0.8157101     MJSW    = 0.1004233
+CJSWG   = 3.3E-10      PBSWG   = 0.8157101     MJSWG   = 0.1004233
+CF      = 0            PVTH0   = -8.863347E-4  PRDSW   = -3.6877287
+PK2     = 3.730349E-4  WKETA   = 6.284186E-3   LKETA   = -0.0106193
+PU0     = 16.6114107   PUA     = 6.572846E-11  PUB     = 0
+PVSAT   = 1.112243E3   PETA0   = 1.002968E-4   PKETA   = -2.906037E-3   )
```

```
.MODEL PMOS PMOS (                      LEVEL   = 7
+VERSION = 3.1          TNOM    = 27          TOX     = 4.1E-9
+XJ      = 1E-7         NCH     = 4.1589E17   VTH0    = -0.3948389
+K1      = 0.5763529    K2      = 0.0289236   K3      = 0
+K3B     = 13.8420955   W0      = 1E-6        NLX     = 1.337719E-7
+DVT0W   = 0            DVT1W   = 0           DVT2W   = 0
+DVT0    = 0.5281977    DVT1    = 0.2185978   DVT2    = 0.1
+U0      = 109.9762536  UA      = 1.325075E-9 UB      = 1.577494E-21
+UC      = -1E-10       VSAT    = 1.910164E5  A0      = 1.7233027
+AGS     = 0.3631032    B0      = 2.336565E-7 B1      = 5.517259E-7
+KETA    = 0.0217218    A1      = 0.3935816   A2      = 0.401311
+RDSW    = 252.7123939  PRWG    = 0.5         PRWB    = 0.0158894
+WR      = 1            WINT    = 0           LINT    = 2.718137E-8
+XL      = 0            XW      = -1E-8       DWG     = -4.363993E-8
+DWB     = 8.876273E-10 VOFF    = -0.0942201  NFACTOR = 2
+CIT     = 0            CDSC    = 2.4E-4      CDSCD   = 0
+CDSCB   = 0            ETA0    = 0.2091053   ETAB    = -0.1097233
+DSUB    = 1.2513945    PCLM    = 2.1999615   PDIBLC1 = 1.238047E-3
+PDIBLC2 = 0.0402861    PDIBLCB = -1E-3       DROUT   = 0
+PSCBE1  = 1.034924E10  PSCBE2  = 2.991339E-9 PVAG    = 15
+DELTA   = 0.01         RSH     = 7.5         MOBMOD  = 1
+PRT     = 0            UTE     = -1.5        KT1     = -0.11
+KT1L    = 0            KT2     = 0.022       UA1     = 4.31E-9
+UB1     = -7.61E-18    UC1     = -5.6E-11    AT      = 3.3E4
+WL      = 0            WLN     = 1           WW      = 0
+WWN     = 1            WWL     = 0           LL      = 0
+LLN     = 1            LW      = 0           LWN     = 1
+LWL     = 0            CAPMOD  = 2           XPART   = 0.5
+CGDO    = 6.28E-10     CGSO    = 6.28E-10    CGBO    = 1E-12
+CJ      = 1.160855E-3  PB      = 0.8484374   MJ      = 0.4079216
+CJSW    = 2.306564E-10 PBSW    = 0.842712    MJSW    = 0.3673317
+CJSWG   = 4.22E-10     PBSWG   = 0.842712    MJSWG   = 0.3673317
+CF      = 0            PVTH0   = 2.619929E-3 PRDSW   = 1.0634509
+PK2     = 1.940657E-3  WKETA   = 0.0355444   LKETA   = -3.037019E-3
+PU0     = -1.0227548   PUA     = -4.36707E-11 PUB     = 1E-21
+PVSAT   = -50          PETA0   = 1E-4        PKETA   = -5.167295E-3  )


VDD 1 0 DC 0.9
VSS 2 0 DC -0.9
.ENDS
.AC DEC 100 10K 100MEG
*.PRINT AC I(V2)
.PRINT AC 'VDB(1)+20'
```

1.3 Analysis of BPF programming.

```
T-Spice - Tanner SPICE
Version 13.00
Standalone hardware lock
Product Release ID: T-Spice Win32 13.00.20080321.01:01:33
```

```
*
V1 5 0 AC 0
V2 4 0 AC 0.1
V3 2 0 AC 0
C1 3 4 10P
C2 1 5 5P
X1 2 1 3 10 VDIBA
X2 3 1 1 11 VDIBA


.SUBCKT VDIBA  5   6  7  8
 *           VP VN IZ VW
*V3 11 0 AC 0.1
*V1 12 0 AC 0
*V2 6 0 AC 0
*VP=5, VN=6, IZ=7, VW=8
*V2 7 0 DC 0
*vp 5 0 ac .1
*vn 6 0 ac -.1
IB 4 2 DC 100U
M1 3 5 4 4 NMOS W=18U L=1.08U
M2 7 6 4 4 NMOS W=18U L=1.08U
M3 3 3 1 1 PMOS W=18U L=1.08U
M4 7 3 1 1 PMOS W=18U L=1.08U
M5 1 1 8 8 NMOS W=54U L=0.18U
M6 8 7 2 2 NMOS W=54U L=0.18U
*C1 7 11 25P
*C2 5 12 10P
*R1 5 8 1.67K


.MODEL NMOS NMOS (                              LEVEL   = 7
+VERSION = 3.1          TNOM    = 27            TOX     = 4.1E-9
+XJ      = 1E-7         NCH     = 2.3549E17     VTH0    = 0.3725327
+K1      = 0.5933684    K2      = 2.050755E-3   K3      = 1E-3
+K3B     = 4.5116437    W0      = 1E-7          NLX     = 1.870758E-7
+DVT0W   = 0            DVT1W   = 0             DVT2W   = 0
+DVT0    = 1.3621338    DVT1    = 0.3845146     DVT2    = 0.0577255
+U0      = 259.5304169  UA      = -1.413292E-9  UB      = 2.229959E-18
+UC      = 4.525942E-11 VSAT    = 9.411671E4    A0      = 1.7572867
+AGS     = 0.3740333    B0      = -7.087476E-9  B1      = -1E-7
+KETA    = -4.331915E-3 A1      = 0             A2      = 1
+RDSW    = 111.886044   PRWG    = 0.5           PRWB    = -0.2
+WR      = 1            WINT    = 0             LINT    = 1.701524E-8
+XL      = 0            XW      = -1E-8         DWG     = -1.365589E-8
+DWB     = 1.045599E-8  VOFF    = -0.0927546    NFACTOR = 2.4494296
+CIT     = 0            CDSC    = 2.4E-4        CDSCD   = 0
+CDSCB   = 0            ETA0    = 3.175457E-3   ETAB    = 3.494694E-5
+DSUB    = 0.0175288    PCLM    = 0.7273497     PDIBLC1 = 0.1886574
+PDIBLC2 = 2.617136E-3  PDIBLCB = -0.1          DROUT   = 0.7779462
+PSCBE1  = 3.488238E10  PSCBE2  = 6.841553E-10  PVAG    = 0.0162206
+DELTA   = 0.01         RSH     = 6.5           MOBMOD  = 1
```

```
+PRT     = 0           UTE     = -1.5         KT1     = -0.11
+KT1L    = 0           KT2     = 0.022        UA1     = 4.31E-9
+UB1     = -7.61E-18   UC1     = -5.6E-11     AT      = 3.3E4
+WL      = 0           WLN     = 1            WW      = 0
+WWN     = 1           WWL     = 0            LL      = 0
+LLN     = 1           LW      = 0            LWN     = 1
+LWL     = 0           CAPMOD  = 2            XPART   = 0.5
+CGDO    = 8.53E-10    CGSO    = 8.53E-10     CGBO    = 1E-12
+CJ      = 9.513993E-4 PB      = 0.8          MJ      = 0.3773625
+CJSW    = 2.600853E-10 PBSW   = 0.8157101    MJSW    = 0.1004233
+CJSWG   = 3.3E-10     PBSWG   = 0.8157101    MJSWG   = 0.1004233
+CF      = 0           PVTH0   = -8.863347E-4 PRDSW   = -3.6877287
+PK2     = 3.730349E-4 WKETA   = 6.284186E-3  LKETA   = -0.0106193
+PU0     = 16.6114107  PUA     = 6.572846E-11 PUB     = 0
+PVSAT   = 1.112243E3  PETA0   = 1.002968E-4  PKETA   = -2.906037E-3  )


*
.MODEL PMOS PMOS (                      LEVEL   = 7
+VERSION = 3.1         TNOM    = 27           TOX     = 4.1E-9
+XJ      = 1E-7        NCH     = 4.1589E17    VTH0    = -0.3948389
+K1      = 0.5763529   K2      = 0.0289236    K3      = 0
+K3B     = 13.8420955  W0      = 1E-6         NLX     = 1.337719E-7
+DVT0W   = 0           DVT1W   = 0            DVT2W   = 0
+DVT0    = 0.5281977   DVT1    = 0.2185978    DVT2    = 0.1
+U0      = 109.9762536 UA      = 1.325075E-9  UB      = 1.577494E-21
+UC      = -1E-10      VSAT    = 1.910164E5   A0      = 1.7233027
+AGS     = 0.3631032   B0      = 2.336565E-7  B1      = 5.517259E-7
+KETA    = 0.0217218   A1      = 0.3935816    A2      = 0.401311
+RDSW    = 252.7123939 PRWG    = 0.5          PRWB    = 0.0158894
+WR      = 1           WINT    = 0            LINT    = 2.718137E-8
+XL      = 0           XW      = -1E-8        DWG     = -4.363993E-8
+DWB     = 8.876273E-10 VOFF   = -0.0942201   NFACTOR = 2
+CIT     = 0           CDSC    = 2.4E-4       CDSCD   = 0
+CDSCB   = 0           ETA0    = 0.2091053    ETAB    = -0.1097233
+DSUB    = 1.2513945   PCLM    = 2.1999615    PDIBLC1 = 1.238047E-3
+PDIBLC2 = 0.0402861   PDIBLCB = -1E-3        DROUT   = 0
+PSCBE1  = 1.034924E10 PSCBE2  = 2.991339E-9  PVAG    = 15
+DELTA   = 0.01        RSH     = 7.5          MOBMOD  = 1
+PRT     = 0           UTE     = -1.5         KT1     = -0.11
+KT1L    = 0           KT2     = 0.022        UA1     = 4.31E-9
+UB1     = -7.61E-18   UC1     = -5.6E-11     AT      = 3.3E4
+WL      = 0           WLN     = 1            WW      = 0
+WWN     = 1           WWL     = 0            LL      = 0
+LLN     = 1           LW      = 0            LWN     = 1
+LWL     = 0           CAPMOD  = 2            XPART   = 0.5
+CGDO    = 6.28E-10    CGSO    = 6.28E-10     CGBO    = 1E-12
+CJ      = 1.160855E-3 PB      = 0.8484374    MJ      = 0.4079216
+CJSW    = 2.306564E-10 PBSW   = 0.842712     MJSW    = 0.3673317
+CJSWG   = 4.22E-10    PBSWG   = 0.842712     MJSWG   = 0.3673317
+CF      = 0           PVTH0   = 2.619929E-3  PRDSW   = 1.0634509
+PK2     = 1.940657E-3 WKETA   = 0.0355444    LKETA   = -3.037019E-3
+PU0     = -1.0227548  PUA     = -4.36707E-11 PUB     = 1E-21
+PVSAT   = -50         PETA0   = 1E-4         PKETA   = -5.167295E-3  )
```

```
VDD 1 0 DC 0.9
VSS 2 0 DC -0.9
.ENDS


.AC DEC 100 10K 100MEG
*.PRINT AC I(V2)
.PRINT AC 'VDB(1)+20'
```

1.4 Analysis of BRF programming.

```
T-Spice - Tanner SPICE
Version 13.00
Standalone hardware lock
Product Release ID: T-Spice Win32 13.00.20080321.01:01:33
Copyright © 1993-2008 Tanner EDA


*
V1 5 0 AC 0.1
V2 4 0 AC 0
V3 2 0 AC 0.1
C1 3 4 10P
C2 1 5 5P
X1 2 1 3 10 VDIBA
X2 3 1 1 11 VDIBA


.SUBCKT VDIBA  5   6  7  8
 *           VP VN IZ VW
*V3 11 0 AC 0.1
*V1 12 0 AC 0
*V2 6 0 AC 0
*VP=5, VN=6, IZ=7, VW=8
*V2 7 0 DC 0
*vp 5 0 ac .1
*vn 6 0 ac -.1
IB 4 2 DC 100U
M1 3 5 4 4 NMOS W=18U L=1.08U
M2 7 6 4 4 NMOS W=18U L=1.08U
M3 3 3 1 1 PMOS W=18U L=1.08U
M4 7 3 1 1 PMOS W=18U L=1.08U
M5 1 1 8 8 NMOS W=54U L=0.18U
M6 8 7 2 2 NMOS W=54U L=0.18U
*C1 7 11 25P
*C2 5 12 10P
*R1 5 8 1.67K


.MODEL NMOS NMOS (                      LEVEL   = 7
+VERSION = 3.1          TNOM    = 27            TOX     = 4.1E-9
+XJ      = 1E-7         NCH     = 2.3549E17     VTH0    = 0.3725327
+K1      = 0.5933684    K2      = 2.050755E-3   K3      = 1E-3
+K3B     = 4.5116437    W0      = 1E-7          NLX     = 1.870758E-7
```

```
+DVT0W   = 0           DVT1W   = 0           DVT2W   = 0
+DVT0    = 1.3621338     DVT1    = 0.3845146     DVT2    = 0.0577255
+U0      = 259.5304169   UA      = -1.413292E-9  UB      = 2.229959E-18
+UC      = 4.525942E-11  VSAT    = 9.411671E4    A0      = 1.7572867
+AGS     = 0.3740333     B0      = -7.087476E-9  B1      = -1E-7
+KETA    = -4.331915E-3  A1      = 0           A2      = 1
+RDSW    = 111.886044    PRWG    = 0.5         PRWB    = -0.2
+WR      = 1           WINT    = 0           LINT    = 1.701524E-8
+XL      = 0           XW      = -1E-8       DWG     = -1.365589E-8
+DWB     = 1.045599E-8   VOFF    = -0.0927546    NFACTOR = 2.4494296
+CIT     = 0           CDSC    = 2.4E-4      CDSCD   = 0
+CDSCB   = 0           ETA0    = 3.175457E-3   ETAB    = 3.494694E-5
+DSUB    = 0.0175288     PCLM    = 0.7273497     PDIBLC1 = 0.1886574
+PDIBLC2 = 2.617136E-3   PDIBLCB = -0.1        DROUT   = 0.7779462
+PSCBE1  = 3.488238E10   PSCBE2  = 6.841553E-10  PVAG    = 0.0162206
+DELTA   = 0.01        RSH     = 6.5         MOBMOD  = 1
+PRT     = 0           UTE     = -1.5        KT1     = -0.11
+KT1L    = 0           KT2     = 0.022       UA1     = 4.31E-9
+UB1     = -7.61E-18     UC1     = -5.6E-11      AT      = 3.3E4
+WL      = 0           WLN     = 1           WW      = 0
+WWN     = 1           WWL     = 0           LL      = 0
+LLN     = 1           LW      = 0           LWN     = 1
+LWL     = 0           CAPMOD  = 2           XPART   = 0.5
+CGDO    = 8.53E-10      CGSO    = 8.53E-10      CGBO    = 1E-12
+CJ      = 9.513993E-4   PB      = 0.8         MJ      = 0.3773625
+CJSW    = 2.600853E-10  PBSW    = 0.8157101     MJSW    = 0.1004233
+CJSWG   = 3.3E-10       PBSWG   = 0.8157101     MJSWG   = 0.1004233
+CF      = 0           PVTH0   = -8.863347E-4  PRDSW   = -3.6877287
+PK2     = 3.730349E-4   WKETA   = 6.284186E-3   LKETA   = -0.0106193
+PU0     = 16.6114107    PUA     = 6.572846E-11  PUB     = 0
+PVSAT   = 1.112243E3    PETA0   = 1.002968E-4   PKETA   = -2.906037E-3    )


*
.MODEL PMOS PMOS (                            LEVEL   = 7
+VERSION = 3.1         TNOM    = 27          TOX     = 4.1E-9
+XJ      = 1E-7        NCH     = 4.1589E17     VTH0    = -0.3948389
+K1      = 0.5763529     K2      = 0.0289236     K3      = 0
+K3B     = 13.8420955    W0      = 1E-6        NLX     = 1.337719E-7
+DVT0W   = 0           DVT1W   = 0           DVT2W   = 0
+DVT0    = 0.5281977     DVT1    = 0.2185978     DVT2    = 0.1
+U0      = 109.9762536   UA      = 1.325075E-9   UB      = 1.577494E-21
+UC      = -1E-10        VSAT    = 1.910164E5    A0      = 1.7233027
+AGS     = 0.3631032     B0      = 2.336565E-7   B1      = 5.517259E-7
+KETA    = 0.0217218     A1      = 0.3935816     A2      = 0.401311
+RDSW    = 252.7123939   PRWG    = 0.5         PRWB    = 0.0158894
+WR      = 1           WINT    = 0           LINT    = 2.718137E-8
+XL      = 0           XW      = -1E-8       DWG     = -4.363993E-8
+DWB     = 8.876273E-10  VOFF    = -0.0942201    NFACTOR = 2
+CIT     = 0           CDSC    = 2.4E-4      CDSCD   = 0
+CDSCB   = 0           ETA0    = 0.2091053     ETAB    = -0.1097233
+DSUB    = 1.2513945     PCLM    = 2.1999615     PDIBLC1 = 1.238047E-3
+PDIBLC2 = 0.0402861     PDIBLCB = -1E-3       DROUT   = 0
+PSCBE1  = 1.034924E10   PSCBE2  = 2.991339E-9   PVAG    = 15
+DELTA   = 0.01        RSH     = 7.5         MOBMOD  = 1
```

```
+PRT     = 0            UTE     = -1.5          KT1     = -0.11
+KT1L    = 0            KT2     = 0.022         UA1     = 4.31E-9
+UB1     = -7.61E-18    UC1     = -5.6E-11      AT      = 3.3E4
+WL      = 0            WLN     = 1             WW      = 0
+WWN     = 1            WWL     = 0             LL      = 0
+LLN     = 1            LW      = 0             LWN     = 1
+LWL     = 0            CAPMOD  = 2             XPART   = 0.5
+CGDO    = 6.28E-10     CGSO    = 6.28E-10      CGBO    = 1E-12
+CJ      = 1.160855E-3  PB      = 0.8484374     MJ      = 0.4079216
+CJSW    = 2.306564E-10 PBSW    = 0.842712      MJSW    = 0.3673317
+CJSWG   = 4.22E-10     PBSWG   = 0.842712      MJSWG   = 0.3673317
+CF      = 0            PVTH0   = 2.619929E-3   PRDSW   = 1.0634509
+PK2     = 1.940657E-3  WKETA   = 0.0355444     LKETA   = -3.037019E-3
+PU0     = -1.0227548   PUA     = -4.36707E-11  PUB     = 1E-21
+PVSAT   = -50          PETA0   = 1E-4          PKETA   = -5.167295E-3  )


VDD 1 0 DC 0.9
VSS 2 0 DC -0.9
.ENDS


.AC DEC 100 10K 100MEG
*.PRINT AC I(V2)
.PRINT AC 'VDB(1)+20'
```

1.5 Analysis of APF programming.

```
T-Spice - Tanner SPICE
Version 13.00
Standalone hardware lock
Product Release ID: T-Spice Win32 13.00.20080321.01:01:33
Copyright © 1993-2008 Tanner EDA


*
V1 5 0 AC 0.1
V2 4 0 AC 0.1
V3 2 0 AC 0.1
C1 3 4 10P
C2 1 5 5P
X1 2 1 3 10 VDIBA
X2 3 1 1 11 VDIBA


.SUBCKT VDIBA  5   6  7  8
 *           VP VN IZ VW
*V3 11 0 AC 0.1
*V1 12 0 AC 0
*V2 6 0 AC 0
*VP=5, VN=6, IZ=7, VW=8
*V2 7 0 DC 0
*vp 5 0 ac .1
```

```
*vn 6 0 ac -.1
IB 4 2 DC 100U
M1 3 5 4 4 NMOS W=18U L=1.08U
M2 7 6 4 4 NMOS W=18U L=1.08U
M3 3 3 1 1 PMOS W=18U L=1.08U
M4 7 3 1 1 PMOS W=18U L=1.08U
M5 1 1 8 8 NMOS W=54U L=0.18U
M6 8 7 2 2 NMOS W=54U L=0.18U
*C1 7 11 25P
*C2 5 12 10P
*R1 5 8 1.67K


.MODEL NMOS NMOS (                      LEVEL   = 7
+VERSION = 3.1          TNOM    = 27          TOX     = 4.1E-9
+XJ      = 1E-7         NCH     = 2.3549E17     VTH0    = 0.3725327
+K1      = 0.5933684    K2      = 2.050755E-3   K3      = 1E-3
+K3B     = 4.5116437    W0      = 1E-7          NLX     = 1.870758E-7
+DVT0W   = 0            DVT1W   = 0             DVT2W   = 0
+DVT0    = 1.3621338    DVT1    = 0.3845146     DVT2    = 0.0577255
+U0      = 259.5304169  UA      = -1.413292E-9  UB      = 2.229959E-18
+UC      = 4.525942E-11 VSAT    = 9.411671E4    A0      = 1.7572867
+AGS     = 0.3740333    B0      = -7.087476E-9  B1      = -1E-7
+KETA    = -4.331915E-3 A1      = 0             A2      = 1
+RDSW    = 111.886044   PRWG    = 0.5           PRWB    = -0.2
+WR      = 1            WINT    = 0             LINT    = 1.701524E-8
+XL      = 0            XW      = -1E-8         DWG     = -1.365589E-8
+DWB     = 1.045599E-8  VOFF    = -0.0927546    NFACTOR = 2.4494296
+CIT     = 0            CDSC    = 2.4E-4        CDSCD   = 0
+CDSCB   = 0            ETA0    = 3.175457E-3   ETAB    = 3.494694E-5
+DSUB    = 0.0175288    PCLM    = 0.7273497     PDIBLC1 = 0.1886574
+PDIBLC2 = 2.617136E-3  PDIBLCB = -0.1          DROUT   = 0.7779462
+PSCBE1  = 3.488238E10  PSCBE2  = 6.841553E-10  PVAG    = 0.0162206
+DELTA   = 0.01         RSH     = 6.5           MOBMOD  = 1
+PRT     = 0            UTE     = -1.5          KT1     = -0.11
+KT1L    = 0            KT2     = 0.022         UA1     = 4.31E-9
+UB1     = -7.61E-18    UC1     = -5.6E-11      AT      = 3.3E4
+WL      = 0            WLN     = 1             WW      = 0
+WWN     = 1            WWL     = 0             LL      = 0
+LLN     = 1            LW      = 0             LWN     = 1
+LWL     = 0            CAPMOD  = 2             XPART   = 0.5
+CGDO    = 8.53E-10     CGSO    = 8.53E-10      CGBO    = 1E-12
+CJ      = 9.513993E-4  PB      = 0.8           MJ      = 0.3773625
+CJSW    = 2.600853E-10 PBSW    = 0.8157101     MJSW    = 0.1004233
+CJSWG   = 3.3E-10      PBSWG   = 0.8157101     MJSWG   = 0.1004233
+CF      = 0            PVTH0   = -8.863347E-4  PRDSW   = -3.6877287
+PK2     = 3.730349E-4  WKETA   = 6.284186E-3   LKETA   = -0.0106193
+PU0     = 16.6114107   PUA     = 6.572846E-11  PUB     = 0
+PVSAT   = 1.112243E3   PETA0   = 1.002968E-4   PKETA   = -2.906037E-3   )


*
.MODEL PMOS PMOS (                      LEVEL   = 7
+VERSION = 3.1          TNOM    = 27          TOX     = 4.1E-9
+XJ      = 1E-7         NCH     = 4.1589E17     VTH0    = -0.3948389
```

```
+K1      = 0.5763529      K2      = 0.0289236      K3      = 0
+K3B     = 13.8420955     W0      = 1E-6           NLX     = 1.337719E-7
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
+DVT0    = 0.5281977      DVT1    = 0.2185978      DVT2    = 0.1
+U0      = 109.9762536    UA      = 1.325075E-9    UB      = 1.577494E-21
+UC      = -1E-10         VSAT    = 1.910164E5     A0      = 1.7233027
+AGS     = 0.3631032      B0      = 2.336565E-7    B1      = 5.517259E-7
+KETA    = 0.0217218      A1      = 0.3935816      A2      = 0.401311
+RDSW    = 252.7123939    PRWG    = 0.5            PRWB    = 0.0158894
+WR      = 1              WINT    = 0              LINT    = 2.718137E-8
+XL      = 0              XW      = -1E-8          DWG     = -4.363993E-8
+DWB     = 8.876273E-10   VOFF    = -0.0942201     NFACTOR = 2
+CIT     = 0              CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0              ETA0    = 0.2091053      ETAB    = -0.1097233
+DSUB    = 1.2513945      PCLM    = 2.1999615      PDIBLC1 = 1.238047E-3
+PDIBLC2 = 0.0402861      PDIBLCB = -1E-3          DROUT   = 0
+PSCBE1  = 1.034924E10    PSCBE2  = 2.991339E-9    PVAG    = 15
+DELTA   = 0.01           RSH     = 7.5            MOBMOD  = 1
+PRT     = 0              UTE     = -1.5           KT1     = -0.11
+KT1L    = 0              KT2     = 0.022          UA1     = 4.31E-9
+UB1     = -7.61E-18      UC1     = -5.6E-11       AT      = 3.3E4
+WL      = 0              WLN     = 1              WW      = 0
+WWN     = 1              WWL     = 0              LL      = 0
+LLN     = 1              LW      = 0              LWN     = 1
+LWL     = 0              CAPMOD  = 2              XPART   = 0.5
+CGDO    = 6.28E-10       CGSO    = 6.28E-10       CGBO    = 1E-12
+CJ      = 1.160855E-3    PB      = 0.8484374      MJ      = 0.4079216
+CJSW    = 2.306564E-10   PBSW    = 0.842712       MJSW    = 0.3673317
+CJSWG   = 4.22E-10       PBSWG   = 0.842712       MJSWG   = 0.3673317
+CF      = 0              PVTH0   = 2.619929E-3    PRDSW   = 1.0634509
+PK2     = 1.940657E-3    WKETA   = 0.0355444      LKETA   = -3.037019E-3
+PU0     = -1.0227548     PUA     = -4.36707E-11   PUB     = 1E-21
+PVSAT   = -50            PETA0   = 1E-4           PKETA   = -5.167295E-3    )


VDD 1 0 DC 0.9
VSS 2 0 DC -0.9
.ENDS


.AC DEC 100 10K 100MEG
*.PRINT AC I(V2)
.PRINT AC 'VDB(1)+20'
```

1.6 Analysis of frequency variation programming at 100µA.

```
T-Spice - Tanner SPICE
Version 13.00
Standalone hardware lock
Product Release ID: T-Spice Win32 13.00.20080321.01:01:33
Copyright © 1993-2008 Tanner EDA
```

```
*
V1 5 0 AC 0
V2 4 0 AC 0
V3 2 0 AC 0.1
C1 3 4 10P
C2 1 5 5P


X1 2 1 3 10 VDIBA
X2 3 1 1 11 VDIBA


.SUBCKT VDIBA  5   6  7  8
 *            VP VN IZ VW
*V3 11 0 AC 0.1
*V1 12 0 AC 0
*V2 6 0 AC 0
*VP=5, VN=6, IZ=7, VW=8
*V2 7 0 DC 0
*vp 5 0 ac .1
*vn 6 0 ac -.1
IB 4 2 DC 100U
M1 3 5 4 4 NMOS W=18U L=1.08U
M2 7 6 4 4 NMOS W=18U L=1.08U
M3 3 3 1 1 PMOS W=18U L=1.08U
M4 7 3 1 1 PMOS W=18U L=1.08U
M5 1 1 8 8 NMOS W=54U L=0.18U
M6 8 7 2 2 NMOS W=54U L=0.18U
*C1 7 11 25P
*C2 5 12 10P
*R1 5 8 1.67K


.MODEL NMOS NMOS (                          LEVEL   = 7
+VERSION = 3.1          TNOM    = 27          TOX     = 4.1E-9
+XJ      = 1E-7         NCH     = 2.3549E17   VTH0    = 0.354505
+K1      = 0.5733393    K2      = 3.177172E-3 K3      = 27.3563303
+K3B     = -10          W0      = 2.341477E-5 NLX     = 1.906617E-7
+DVT0W   = 0            DVT1W   = 0           DVT2W   = 0
+DVT0    = 1.6751718    DVT1    = 0.4282625   DVT2    = 0.036004
+U0      = 327.3736992  UA      = -4.52726E-11 UB     = 4.46532E-19
+UC      = -4.74051E-11 VSAT    = 8.785346E4  A0      = 1.6897405
+AGS     = 0.2908676    B0      = -8.224961E-9 B1     = -1E-7
+KETA    = 0.021238     A1      = 8.00349E-4  A2      = 1
+RDSW    = 105          PRWG    = 0.5         PRWB    = -0.2
+WR      = 1            WINT    = 0           LINT    = 1.351737E-8
+XL      = -2E-8        XW      = -1E-8
+ DWG     = 1.610448E-9
+DWB     = -5.108595E-9 VOFF    = -0.0652968  NFACTOR = 2.4901845
+CIT     = 0            CDSC    = 2.4E-4      CDSCD   = 0
+CDSCB   = 0            ETA0    = 0.0231564   ETAB    = -0.058499
```

```
+DSUB    = 0.9467118      PCLM    = 0.8512348      PDIBLC1 = 0.0929526
+PDIBLC2 = 0.01           PDIBLCB = -0.1           DROUT   = 0.5224026
+PSCBE1  = 7.979323E10    PSCBE2  = 1.522921E-9    PVAG    = 0.01
+DELTA   = 0.01           RSH     = 6.8            MOBMOD  = 1
+PRT     = 0              UTE     = -1.5           KT1     = -0.11
+KT1L    = 0              KT2     = 0.022          UA1     = 4.31E-9
+UB1     = -7.61E-18      UC1     = -5.6E-11       AT      = 3.3E4
+WL      = 0              WLN     = 1              WW      = 0
+WWN     = 1              WWL     = 0              LL      = 0
+LLN     = 1              LW      = 0              LWN     = 1
+LWL     = 0              CAPMOD  = 2              XPART   = 0.5
+CGDO    = 7.7E-10        CGSO    = 7.7E-10        CGBO    = 1E-12
+CJ      = 1.010083E-3    PB      = 0.7344298      MJ      = 0.3565066
+CJSW    = 2.441707E-10   PBSW    = 0.8005503      MJSW    = 0.1327842
+CJSWG   = 3.3E-10        PBSWG   = 0.8005503      MJSWG   = 0.1327842
+CF      = 0              PVTH0   = 1.307195E-3    PRDSW   = -5
+PK2     = -1.022757E-3   WKETA   = -4.466285E-4   LKETA   = -9.715157E-3
+PU0     = 12.2704847     PUA     = 4.421816E-11   PUB     = 0
+PVSAT   = 1.707461E3     PETA0   = 1E-4           PKETA   = 2.348777E-3    )


*
.MODEL PMOS PMOS (                       LEVEL   = 7
+VERSION = 3.1            TNOM    = 27             TOX     = 4.1E-9
+XJ      = 1E-7           NCH     = 4.1589E17      VTH0    = -0.4120614
+K1      = 0.5590154      K2      = 0.0353896      K3      = 0
+K3B     = 7.3774572      W0      = 1E-6           NLX     = 1.103367E-7
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
+DVT0    = 0.4301522      DVT1    = 0.2156888      DVT2    = 0.1
+U0      = 128.7704538    UA      = 1.908676E-9    UB      = 1.686179E-21
+UC      = -9.31329E-11   VSAT    = 1.658944E5     A0      = 1.6076505
+AGS     = 0.3740519      B0      = 1.711294E-6    B1      = 4.946873E-6
+KETA    = 0.0210951      A1      = 0.0244939      A2      = 1
+RDSW    = 127.0442882    PRWG    = 0.5            PRWB    = -0.5
+WR      = 1              WINT    = 5.428484E-10   LINT    = 2.468805E-8
+XL      = -2E-8          XW      = -1E-8
+DWG     = -2.453074E-8
+DWB     = 6.408778E-9    VOFF    = -0.0974174     NFACTOR = 1.9740447
+CIT     = 0              CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0              ETA0    = 0.1847491      ETAB    = -0.2531172
+DSUB    = 1.5            PCLM    = 4.8842961      PDIBLC1 = 0.0156227
+PDIBLC2 = 0.1            PDIBLCB = -1E-3          DROUT   = 0
+PSCBE1  = 1.733878E9     PSCBE2  = 5.002842E-10   PVAG    = 15
+DELTA   = 0.01           RSH     = 7.7            MOBMOD  = 1
+PRT     = 0              UTE     = -1.5           KT1     = -0.11
+KT1L    = 0              KT2     = 0.022          UA1     = 4.31E-9
+UB1     = -7.61E-18      UC1     = -5.6E-11       AT      = 3.3E4
+WL      = 0              WLN     = 1              WW      = 0
+WWN     = 1              WWL     = 0              LL      = 0
+LLN     = 1              LW      = 0              LWN     = 1
+LWL     = 0              CAPMOD  = 2              XPART   = 0.5
```

```
+CGDO    = 7.11E-10      CGSO    = 7.11E-10      CGBO    = 1E-12
+CJ      = 1.179334E-3   PB      = 0.8545261     MJ      = 0.4117753
+CJSW    = 2.215877E-10  PBSW    = 0.6162997     MJSW    = 0.2678074
+CJSWG   = 4.22E-10      PBSWG   = 0.6162997     MJSWG   = 0.2678074
+CF      = 0             PVTH0   = 2.283319E-3   PRDSW   = 5.6431992
+PK2     = 2.813503E-3   WKETA   = 2.438158E-3   LKETA   = -0.0116078
+PU0     = -2.2514581    PUA     = -7.62392E-11  PUB     = 4.502298E-24
+PVSAT   = -50           PETA0   = 1E-4          PKETA   = -1.047892E-4   )
VDD 1 0 DC 0.9
VSS 2 0 DC -0.9
.ENDS


.AC DEC 100 10K 100MEG
*.PRINT AC I(V2)
.PRINT AC 'VDB(1)+20'


.alter k2
V1 5 0 AC 0
V2 4 0 AC 0.1
V3 2 0 AC 0


.ALTER K3
V1 5 0 AC 0.1
V2 4 0 AC 0
V3 2 0 AC 0


.ALTER K4
V1 5 0 AC 0.1
V2 4 0 AC 0
V3 2 0 AC 0.1


.ALTER K5
V1 5 0 AC 0.1
V2 4 0 AC 0.1
V3 2 0 AC 0.1
```

1.7 Analysis of frequency variation programming at 150µA.

```
T-Spice - Tanner SPICE
Version 13.00
Standalone hardware lock
Product Release ID: T-Spice Win32 13.00.20080321.01:01:33
```

```
*
V1 5 0 AC 0
V2 4 0 AC 0
V3 2 0 AC 0.1
C1 3 4 10P
C2 1 5 5P


X1 2 1 3 10 VDIBA
X2 3 1 1 11 VDIBA


.SUBCKT VDIBA  5   6  7  8
 *           VP VN IZ VW
*V3 11 0 AC 0.1
*V1 12 0 AC 0
*V2 6 0 AC 0
*VP=5, VN=6, IZ=7, VW=8
*V2 7 0 DC 0
*vp 5 0 ac .1
*vn 6 0 ac -.1
IB 4 2 DC 150U
M1 3 5 4 4 NMOS W=18U L=1.08U
M2 7 6 4 4 NMOS W=18U L=1.08U
M3 3 3 1 1 PMOS W=18U L=1.08U
M4 7 3 1 1 PMOS W=18U L=1.08U
M5 1 1 8 8 NMOS W=54U L=0.18U
M6 8 7 2 2 NMOS W=54U L=0.18U
*C1 7 11 25P
*C2 5 12 10P
*R1 5 8 1.67K


.MODEL NMOS NMOS (                          LEVEL   = 7
+VERSION = 3.1          TNOM    = 27          TOX     = 4.1E-9
+XJ      = 1E-7         NCH     = 2.3549E17   VTH0    = 0.354505
+K1      = 0.5733393    K2      = 3.177172E-3 K3      = 27.3563303
+K3B     = -10          W0      = 2.341477E-5 NLX     = 1.906617E-7
+DVT0W   = 0            DVT1W   = 0           DVT2W   = 0
+DVT0    = 1.6751718    DVT1    = 0.4282625   DVT2    = 0.036004
+U0      = 327.3736992  UA      = -4.52726E-11 UB     = 4.46532E-19
+UC      = -4.74051E-11 VSAT    = 8.785346E4  A0      = 1.6897405
+AGS     = 0.2908676    B0      = -8.224961E-9 B1     = -1E-7
+KETA    = 0.021238     A1      = 8.00349E-4  A2      = 1
+RDSW    = 105          PRWG    = 0.5         PRWB    = -0.2
+WR      = 1            WINT    = 0           LINT    = 1.351737E-8
+XL      = -2E-8        XW      = -1E-8
+ DWG     = 1.610448E-9
```

```
+DWB    = -5.108595E-9   VOFF    = -0.0652968     NFACTOR = 2.4901845
+CIT    = 0              CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB  = 0              ETA0    = 0.0231564      ETAB    = -0.058499
+DSUB   = 0.9467118      PCLM    = 0.8512348      PDIBLC1 = 0.0929526
+PDIBLC2 = 0.01          PDIBLCB = -0.1           DROUT   = 0.5224026
+PSCBE1  = 7.979323E10   PSCBE2  = 1.522921E-9    PVAG    = 0.01
+DELTA   = 0.01          RSH     = 6.8            MOBMOD  = 1
+PRT     = 0             UTE     = -1.5           KT1     = -0.11
+KT1L    = 0             KT2     = 0.022          UA1     = 4.31E-9
+UB1     = -7.61E-18     UC1     = -5.6E-11       AT      = 3.3E4
+WL      = 0             WLN     = 1              WW      = 0
+WWN     = 1             WWL     = 0              LL      = 0
+LLN     = 1             LW      = 0              LWN     = 1
+LWL     = 0             CAPMOD  = 2              XPART   = 0.5
+CGDO    = 7.7E-10       CGSO    = 7.7E-10        CGBO    = 1E-12
+CJ      = 1.010083E-3   PB      = 0.7344298      MJ      = 0.3565066
+CJSW    = 2.441707E-10  PBSW    = 0.8005503      MJSW    = 0.1327842
+CJSWG   = 3.3E-10       PBSWG   = 0.8005503      MJSWG   = 0.1327842
+CF      = 0             PVTH0   = 1.307195E-3    PRDSW   = -5
+PK2     = -1.022757E-3  WKETA   = -4.466285E-4   LKETA   = -9.715157E-3
+PU0     = 12.2704847    PUA     = 4.421816E-11   PUB     = 0
+PVSAT   = 1.707461E3    PETA0   = 1E-4           PKETA   = 2.348777E-3    )


*
.MODEL PMOS PMOS (                       LEVEL   = 7
+VERSION = 3.1           TNOM    = 27             TOX     = 4.1E-9
+XJ      = 1E-7          NCH     = 4.1589E17      VTH0    = -0.4120614
+K1      = 0.5590154     K2      = 0.0353896      K3      = 0
+K3B     = 7.3774572     W0      = 1E-6           NLX     = 1.103367E-7
+DVT0W   = 0             DVT1W   = 0              DVT2W   = 0
+DVT0    = 0.4301522     DVT1    = 0.2156888      DVT2    = 0.1
+U0      = 128.7704538   UA      = 1.908676E-9    UB      = 1.686179E-21
+UC      = -9.31329E-11  VSAT    = 1.658944E5     A0      = 1.6076505
+AGS     = 0.3740519     B0      = 1.711294E-6    B1      = 4.946873E-6
+KETA    = 0.0210951     A1      = 0.0244939      A2      = 1
+RDSW    = 127.0442882   PRWG    = 0.5            PRWB    = -0.5
+WR      = 1             WINT    = 5.428484E-10   LINT    = 2.468805E-8
+XL      = -2E-8         XW      = -1E-8
+DWG     = -2.453074E-8
+DWB     = 6.408778E-9   VOFF    = -0.0974174     NFACTOR = 1.9740447
+CIT     = 0             CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0             ETA0    = 0.1847491      ETAB    = -0.2531172
+DSUB    = 1.5           PCLM    = 4.8842961      PDIBLC1 = 0.0156227
+PDIBLC2 = 0.1           PDIBLCB = -1E-3          DROUT   = 0
+PSCBE1  = 1.733878E9    PSCBE2  = 5.002842E-10   PVAG    = 15
+DELTA   = 0.01          RSH     = 7.7            MOBMOD  = 1
+PRT     = 0             UTE     = -1.5           KT1     = -0.11
+KT1L    = 0             KT2     = 0.022          UA1     = 4.31E-9
+UB1     = -7.61E-18     UC1     = -5.6E-11       AT      = 3.3E4
+WL      = 0             WLN     = 1              WW      = 0
```

```
+WWN     = 1            WWL     = 0            LL      = 0
+LLN     = 1            LW      = 0            LWN     = 1
+LWL     = 0            CAPMOD  = 2            XPART   = 0.5
+CGDO    = 7.11E-10     CGSO    = 7.11E-10     CGBO    = 1E-12
+CJ      = 1.179334E-3  PB      = 0.8545261    MJ      = 0.4117753
+CJSW    = 2.215877E-10 PBSW    = 0.6162997    MJSW    = 0.2678074
+CJSWG   = 4.22E-10     PBSWG   = 0.6162997    MJSWG   = 0.2678074
+CF      = 0            PVTH0   = 2.283319E-3  PRDSW   = 5.6431992
+PK2     = 2.813503E-3  WKETA   = 2.438158E-3  LKETA   = -0.0116078
+PU0     = -2.2514581   PUA     = -7.62392E-11 PUB     = 4.502298E-24
+PVSAT   = -50          PETA0   = 1E-4         PKETA   = -1.047892E-4  )

VDD 1 0 DC 0.9
VSS 2 0 DC -0.9
.ENDS


.AC DEC 100 10K 100MEG
*.PRINT AC I(V2)
.PRINT AC 'VDB(1)+20'


.alter k2
V1 5 0 AC 0
V2 4 0 AC 0.1
V3 2 0 AC 0


.ALTER K3
V1 5 0 AC 0.1
V2 4 0 AC 0
V3 2 0 AC 0


.ALTER K4
V1 5 0 AC 0.1
V2 4 0 AC 0
V3 2 0 AC 0.1


.ALTER K5
V1 5 0 AC 0.1
V2 4 0 AC 0.1
V3 2 0 AC 0.1
```

1.8 Analysis of frequency variation programming at 200µA.

```
*
V1 5 0 AC 0
```

```
V2 4 0 AC 0
V3 2 0 AC 0.1
C1 3 4 10P
C2 1 5 5P


X1 2 1 3 10 VDIBA
X2 3 1 1 11 VDIBA
.SUBCKT VDIBA  5   6  7  8
 *           VP VN IZ VW
*V3 11 0 AC 0.1
*V1 12 0 AC 0
*V2 6 0 AC 0
*VP=5, VN=6, IZ=7, VW=8
*V2 7 0 DC 0
*vp 5 0 ac .1
*vn 6 0 ac -.1
IB 4 2 DC 200U
M1 3 5 4 4 NMOS W=18U L=1.08U
M2 7 6 4 4 NMOS W=18U L=1.08U
M3 3 3 1 1 PMOS W=18U L=1.08U
M4 7 3 1 1 PMOS W=18U L=1.08U
M5 1 1 8 8 NMOS W=54U L=0.18U
M6 8 7 2 2 NMOS W=54U L=0.18U
*C1 7 11 25P
*C2 5 12 10P
*R1 5 8 1.67K
.MODEL NMOS NMOS (                          LEVEL   = 7
+VERSION = 3.1          TNOM    = 27          TOX     = 4.1E-9
+XJ      = 1E-7         NCH     = 2.3549E17   VTH0    = 0.354505
+K1      = 0.5733393    K2      = 3.177172E-3 K3      = 27.3563303
+K3B     = -10          W0      = 2.341477E-5 NLX     = 1.906617E-7
+DVT0W   = 0            DVT1W   = 0           DVT2W   = 0
+DVT0    = 1.6751718    DVT1    = 0.4282625   DVT2    = 0.036004
+U0      = 327.3736992  UA      = -4.52726E-11 UB     = 4.46532E-19
+UC      = -4.74051E-11 VSAT    = 8.785346E4  A0      = 1.6897405
+AGS     = 0.2908676    B0      = -8.224961E-9 B1     = -1E-7
+KETA    = 0.021238     A1      = 8.00349E-4  A2      = 1
+RDSW    = 105          PRWG    = 0.5         PRWB    = -0.2
+WR      = 1            WINT    = 0           LINT    = 1.351737E-8
+XL      = -2E-8        XW      = -1E-8
+ DWG    = 1.610448E-9
+DWB     = -5.108595E-9 VOFF    = -0.0652968  NFACTOR = 2.4901845
+CIT     = 0            CDSC    = 2.4E-4      CDSCD   = 0
+CDSCB   = 0            ETA0    = 0.0231564   ETAB    = -0.058499
+DSUB    = 0.9467118    PCLM    = 0.8512348   PDIBLC1 = 0.0929526
+PDIBLC2 = 0.01         PDIBLCB = -0.1        DROUT   = 0.5224026
+PSCBE1  = 7.979323E10  PSCBE2  = 1.522921E-9 PVAG    = 0.01
+DELTA   = 0.01         RSH     = 6.8         MOBMOD  = 1
+PRT     = 0            UTE     = -1.5        KT1     = -0.11
+KT1L    = 0            KT2     = 0.022       UA1     = 4.31E-9
```

```
+UB1    = -7.61E-18     UC1    = -5.6E-11      AT     = 3.3E4
+WL     = 0             WLN    = 1             WW     = 0
+WWN    = 1             WWL    = 0             LL     = 0
+LLN    = 1             LW     = 0             LWN    = 1
+LWL    = 0             CAPMOD = 2             XPART  = 0.5
+CGDO   = 7.7E-10       CGSO   = 7.7E-10       CGBO   = 1E-12
+CJ     = 1.010083E-3   PB     = 0.7344298     MJ     = 0.3565066
+CJSW   = 2.441707E-10  PBSW   = 0.8005503     MJSW   = 0.1327842
+CJSWG  = 3.3E-10       PBSWG  = 0.8005503     MJSWG  = 0.1327842
+CF     = 0             PVTH0  = 1.307195E-3   PRDSW  = -5
+PK2    = -1.022757E-3  WKETA  = -4.466285E-4  LKETA  = -9.715157E-3
+PU0    = 12.2704847    PUA    = 4.421816E-11  PUB    = 0
+PVSAT  = 1.707461E3    PETA0  = 1E-4          PKETA  = 2.348777E-3    )


*
.MODEL PMOS PMOS (                      LEVEL  = 7
+VERSION = 3.1          TNOM   = 27            TOX    = 4.1E-9
+XJ     = 1E-7          NCH    = 4.1589E17     VTH0   = -0.4120614
+K1     = 0.5590154     K2     = 0.0353896     K3     = 0
+K3B    = 7.3774572     W0     = 1E-6          NLX    = 1.103367E-7
+DVT0W  = 0             DVT1W  = 0             DVT2W  = 0
+DVT0   = 0.4301522     DVT1   = 0.2156888     DVT2   = 0.1
+U0     = 128.7704538   UA     = 1.908676E-9   UB     = 1.686179E-21
+UC     = -9.31329E-11  VSAT   = 1.658944E5    A0     = 1.6076505
+AGS    = 0.3740519     B0     = 1.711294E-6   B1     = 4.946873E-6
+KETA   = 0.0210951     A1     = 0.0244939     A2     = 1
+RDSW   = 127.0442882   PRWG   = 0.5           PRWB   = -0.5
+WR     = 1             WINT   = 5.428484E-10  LINT   = 2.468805E-8
+XL     = -2E-8         XW     = -1E-8
+DWG    = -2.453074E-8
+DWB    = 6.408778E-9   VOFF   = -0.0974174    NFACTOR = 1.9740447
+CIT    = 0             CDSC   = 2.4E-4        CDSCD  = 0
+CDSCB  = 0             ETA0   = 0.1847491     ETAB   = -0.2531172
+DSUB   = 1.5           PCLM   = 4.8842961     PDIBLC1 = 0.0156227
+PDIBLC2 = 0.1          PDIBLCB = -1E-3        DROUT  = 0
+PSCBE1 = 1.733878E9    PSCBE2 = 5.002842E-10  PVAG   = 15
+DELTA  = 0.01          RSH    = 7.7           MOBMOD = 1
+PRT    = 0             UTE    = -1.5          KT1    = -0.11
+KT1L   = 0             KT2    = 0.022         UA1    = 4.31E-9
+UB1    = -7.61E-18     UC1    = -5.6E-11      AT     = 3.3E4
+WL     = 0             WLN    = 1             WW     = 0
+WWN    = 1             WWL    = 0             LL     = 0
+LLN    = 1             LW     = 0             LWN    = 1
+LWL    = 0             CAPMOD = 2             XPART  = 0.5
+CGDO   = 7.11E-10      CGSO   = 7.11E-10      CGBO   = 1E-12
+CJ     = 1.179334E-3   PB     = 0.8545261     MJ     = 0.4117753
+CJSW   = 2.215877E-10  PBSW   = 0.6162997     MJSW   = 0.2678074
+CJSWG  = 4.22E-10      PBSWG  = 0.6162997     MJSWG  = 0.2678074
+CF     = 0             PVTH0  = 2.283319E-3   PRDSW  = 5.6431992
+PK2    = 2.813503E-3   WKETA  = 2.438158E-3   LKETA  = -0.0116078
```

```
+PU0    = -2.2514581    PUA    = -7.62392E-11   PUB    = 4.502298E-24
+PVSAT  = -50           PETA0  = 1E-4           PKETA  = -1.047892E-4   )


VDD 1 0 DC 0.9
VSS 2 0 DC -0.9
.ENDS

.AC DEC 100 10K 100MEG
*.PRINT AC I(V2)
.PRINT AC 'VDB(1)+20'


.alter k2
V1 5 0 AC 0
V2 4 0 AC 0.1
V3 2 0 AC 0

.ALTER K3
V1 5 0 AC 0.1
V2 4 0 AC 0
V3 2 0 AC 0


.ALTER K4
V1 5 0 AC 0.1
V2 4 0 AC 0
V3 2 0 AC 0.1


.ALTER K5
V1 5 0 AC 0.1
V2 4 0 AC 0.1
V3 2 0 AC 0.1
```

1.9 Analysis of frequency variation programming at 250 µA

```
T-Spice - Tanner SPICE
Version 13.00
Standalone hardware lock
Product Release ID: T-Spice Win32 13.00.20080321.01:01:33
Copyright © 1993-2008 Tanner EDA


*
V1 5 0 AC 0
V2 4 0 AC 0
V3 2 0 AC 0.1
```

```
C1 3 4 10P
C2 1 5 5P


X1 2 1 3 10 VDIBA
X2 3 1 1 11 VDIBA

.SUBCKT VDIBA  5   6  7  8
 *           VP VN IZ VW
*V3 11 0 AC 0.1
*V1 12 0 AC 0
*V2 6 0 AC 0
*VP=5, VN=6, IZ=7, VW=8
*V2 7 0 DC 0
*vp 5 0 ac .1
*vn 6 0 ac -.1
IB 4 2 DC 250U
M1 3 5 4 4 NMOS W=18U L=1.08U
M2 7 6 4 4 NMOS W=18U L=1.08U
M3 3 3 1 1 PMOS W=18U L=1.08U
M4 7 3 1 1 PMOS W=18U L=1.08U
M5 1 1 8 8 NMOS W=54U L=0.18U
M6 8 7 2 2 NMOS W=54U L=0.18U
*C1 7 11 25P
*C2 5 12 10P
*R1 5 8 1.67K


.MODEL NMOS NMOS (                          LEVEL   = 7
+VERSION = 3.1          TNOM    = 27          TOX     = 4.1E-9
+XJ      = 1E-7         NCH     = 2.3549E17   VTH0    = 0.354505
+K1      = 0.5733393    K2      = 3.177172E-3 K3      = 27.3563303
+K3B     = -10          W0      = 2.341477E-5 NLX     = 1.906617E-7
+DVT0W   = 0            DVT1W   = 0           DVT2W   = 0
+DVT0    = 1.6751718    DVT1    = 0.4282625   DVT2    = 0.036004
+U0      = 327.3736992  UA      = -4.52726E-11 UB     = 4.46532E-19
+UC      = -4.74051E-11 VSAT    = 8.785346E4  A0      = 1.6897405
+AGS     = 0.2908676    B0      = -8.224961E-9 B1     = -1E-7
+KETA    = 0.021238     A1      = 8.00349E-4  A2      = 1
+RDSW    = 105          PRWG    = 0.5         PRWB    = -0.2
+WR      = 1            WINT    = 0           LINT    = 1.351737E-8
+XL      = -2E-8        XW      = -1E-8
+ DWG     = 1.610448E-9
+DWB     = -5.108595E-9 VOFF    = -0.0652968  NFACTOR = 2.4901845
```

```
+CIT     = 0            CDSC    = 2.4E-4        CDSCD   = 0
+CDSCB   = 0            ETA0    = 0.0231564     ETAB    = -0.058499
+DSUB    = 0.9467118    PCLM    = 0.8512348     PDIBLC1 = 0.0929526
+PDIBLC2 = 0.01         PDIBLCB = -0.1          DROUT   = 0.5224026
+PSCBE1  = 7.979323E10  PSCBE2  = 1.522921E-9   PVAG    = 0.01
+DELTA   = 0.01         RSH     = 6.8           MOBMOD  = 1
+PRT     = 0            UTE     = -1.5          KT1     = -0.11
+KT1L    = 0            KT2     = 0.022         UA1     = 4.31E-9
+UB1     = -7.61E-18    UC1     = -5.6E-11      AT      = 3.3E4
+WL      = 0            WLN     = 1             WW      = 0
+WWN     = 1            WWL     = 0             LL      = 0
+LLN     = 1            LW      = 0             LWN     = 1
+LWL     = 0            CAPMOD  = 2             XPART   = 0.5
+CGDO    = 7.7E-10      CGSO    = 7.7E-10       CGBO    = 1E-12
+CJ      = 1.010083E-3  PB      = 0.7344298     MJ      = 0.3565066
+CJSW    = 2.441707E-10 PBSW    = 0.8005503     MJSW    = 0.1327842
+CJSWG   = 3.3E-10      PBSWG   = 0.8005503     MJSWG   = 0.1327842
+CF      = 0            PVTH0   = 1.307195E-3   PRDSW   = -5
+PK2     = -1.022757E-3 WKETA   = -4.466285E-4  LKETA   = -9.715157E-3
+PU0     = 12.2704847   PUA     = 4.421816E-11  PUB     = 0
+PVSAT   = 1.707461E3   PETA0   = 1E-4          PKETA   = 2.348777E-3    )


*
.MODEL PMOS PMOS (                      LEVEL   = 7
+VERSION = 3.1          TNOM    = 27            TOX     = 4.1E-9
+XJ      = 1E-7         NCH     = 4.1589E17     VTH0    = -0.4120614
+K1      = 0.5590154    K2      = 0.0353896     K3      = 0
+K3B     = 7.3774572    W0      = 1E-6          NLX     = 1.103367E-7
+DVT0W   = 0            DVT1W   = 0             DVT2W   = 0
+DVT0    = 0.4301522    DVT1    = 0.2156888     DVT2    = 0.1
+U0      = 128.7704538  UA      = 1.908676E-9   UB      = 1.686179E-21
+UC      = -9.31329E-11 VSAT    = 1.658944E5    A0      = 1.6076505
+AGS     = 0.3740519    B0      = 1.711294E-6   B1      = 4.946873E-6
+KETA    = 0.0210951    A1      = 0.0244939     A2      = 1
+RDSW    = 127.0442882  PRWG    = 0.5           PRWB    = -0.5
+WR      = 1            WINT    = 5.428484E-10  LINT    = 2.468805E-8
+XL      = -2E-8        XW      = -1E-8
+DWG     = -2.453074E-8
+DWB     = 6.408778E-9  VOFF    = -0.0974174    NFACTOR = 1.9740447
+CIT     = 0            CDSC    = 2.4E-4        CDSCD   = 0
+CDSCB   = 0            ETA0    = 0.1847491     ETAB    = -0.2531172
+DSUB    = 1.5          PCLM    = 4.8842961     PDIBLC1 = 0.0156227
+PDIBLC2 = 0.1          PDIBLCB = -1E-3         DROUT   = 0
```

```
+PSCBE1  = 1.733878E9     PSCBE2  = 5.002842E-10   PVAG    = 15
+DELTA   = 0.01          RSH     = 7.7           MOBMOD  = 1
+PRT     = 0             UTE     = -1.5          KT1     = -0.11
+KT1L    = 0             KT2     = 0.022         UA1     = 4.31E-9
+UB1     = -7.61E-18     UC1     = -5.6E-11      AT      = 3.3E4
+WL      = 0             WLN     = 1             WW      = 0
+WWN     = 1             WWL     = 0             LL      = 0
+LLN     = 1             LW      = 0             LWN     = 1
+LWL     = 0             CAPMOD  = 2             XPART   = 0.5
+CGDO    = 7.11E-10      CGSO    = 7.11E-10      CGBO    = 1E-12
+CJ      = 1.179334E-3   PB      = 0.8545261     MJ      = 0.4117753
+CJSW    = 2.215877E-10  PBSW    = 0.6162997     MJSW    = 0.2678074
+CJSWG   = 4.22E-10      PBSWG   = 0.6162997     MJSWG   = 0.2678074
+CF      = 0             PVTH0   = 2.283319E-3   PRDSW   = 5.6431992
+PK2     = 2.813503E-3   WKETA   = 2.438158E-3   LKETA   = -0.0116078
+PU0     = -2.2514581    PUA     = -7.62392E-11  PUB     = 4.502298E-24
+PVSAT   = -50           PETA0   = 1E-4          PKETA   = -1.047892E-4   )


VDD 1 0 DC 0.9
VSS 2 0 DC -0.9
.ENDS


.AC DEC 100 10K 100MEG
*.PRINT AC I(V2)
.PRINT AC 'VDB(1)+20'


.alter k2
V1 5 0 AC 0
V2 4 0 AC 0.1
V3 2 0 AC 0


.ALTER K3
V1 5 0 AC 0.1
V2 4 0 AC 0
V3 2 0 AC 0


.ALTER K4
V1 5 0 AC 0.1
V2 4 0 AC 0
```

V3 2 0 AC 0.1
.ALTER K5
V1 5 0 AC 0.1
V2 4 0 AC 0.1
V3 2 0 AC 0.1

LIST OF PUBLICATIONS

[1] Praveen Kumar Yadav, guide name, 2017, “Universal filter with variable frequency using VDIBA”, -----*Journal Name*----

CURRICULUM VITAE

Praveen Kumar Yadav is pursing M.Tech at Ganga Technical Campus) Soldha, Bahadurgarh (affiliated to M. D. University, Rohtak, Haryana) in VLSI Design. He received his B.Tech degree in Electronics and Communication Engineering from Dr. Abdul Kalam University, Lucknow in 2018.

His areas of interest are in designing of analog signal processing circuits and low power CMOS VLSI design. During his graduation he worked on the projects which were related to RFID based library management system.

Recently he has successfully published paper on Universal filter with variable frequency using VDIBA and in International Journal ------journal name-----