Group size: 2 students
Expectation: 1. At least two paper to be read
2. Understand the problem addressed in the paper
3. Understand the problem given in problem statement in this document
4. Propose new solution to the problem. Workout the complete solution.
5. Implement your proposed solution and perform basic experiment to validate the working of
your solution.

Evaluation:
First presentation: March End (Problem understanding and possible solution)
Final Presentation: April End (Implementation and experimental results)

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Project 1: Polynomial time formal verification (BDD based) of arithmetic circuit

fvac1: Dreschler et al, PolyAdd: Polynomial Formal Verification of Adder Circuit
Paper 2: find out a relevant paper to read

Problem statement: The primary problem or limitation of the formal verification methodology is the time and space complexity of the verification algorithm. Therefore, the objective of doing a research is to design an efficient algorithm which would perform the verification in linear time complexity for a moderate to complex designs. Example, designing an formal verification techniques to verify a complex adder circuit or multiplier circuit. The other aspect of this research is to find out those suitable complex circuits (combinational or sequential) which can be verified in polynomial time. The design could be a sub-circuit of the complex design which can be verified in polynomial time.

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Project 2: Automatic Test Pattern Generation to Minimize Test Data Volume

Paper 1:
atpg1: Stephan Eggersglüß, Sylwester Milewski, Janusz Rajski, Jerzy Tyszer:
On Reduction of Deterministic Test Pattern Sets. 260-267, ITC 2021.

Paper 2: Of your choice to be read

Problem Statement:
As the design complexity grows along with the shrinking of transistor size as well as advent of newer transistor technology, the size of test pattern set also been increasing accordingly. The test pattern volume has been growing exponentially which intern has impacted the test time and energy required for testing a given chip. The problem of high test data volume for the complex designs needs to be addressed accordingly. The idea of this work is to find out some of the big-data algorithm such as dimensionality reduction to minimize the data volume while keeping the test coverage intact.

The idea is to find out the common pool of tests which are applicable to multiple clusters of faults to keep the n-detect number intact or higher than the existing techniques. For example, ct1, ct2, ct3 ct4 be the

common test pool. Let t1, t2, t3, t4, t5, t6, t7, t8, t9, t10, t11, etc be the test sets for fs1, fs2, fs3,
fs4, fs5, fs6, fs7, fs8, fs9, fs10, fs11 respectively. Now to improve the d-detect the test pattern needs to
be applied as follows:

{ct1, t2} -> fs1
{ct2, t1} -> fs2
similarly to detect other set.
This kind of structuring of the test pattern can be better compressed to minimize the test data volume.

Other related problems: A experiments needs to be performed to find out how does the pattern volume changes
with the complexity of design and transistor dimensionality. Find out the correlation between Moore's law
and test data volume. And similarly the experiment can be performed to figure out the correlation for test
time and compression ratio.

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Project 3: Improving performance of SAT based ATPG

sat1.paper1: Fujita et al, Efficient SAT-based ATPG Techniques for all multiple stuck-at faults
https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7035351

sat2.paper2:

Problem Statement:
The problem to solve is to develop a SAT based ATPG methodology for some of the complex circuit. The SAT
based ATPG compared to the state-of-art D-algorithm based ATPG is better in many of the aspects such as
pattern count, fault coverage etc. Additionally the SAT based ATPG can be easily combined with SAT based
verification to generate pattern which can be used for structural faults as well as for functional bugs. The
particular problem to be tackled here is to design an efficient SAT ATPG to test multiple stuck-at faults
and the others faults such as bridging, and toggling faults.

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Project 4: Testing the Latent Delay Defects

delay1.paper1: Hung et al, Power Supply Noise-Aware At-Speed Delay Fault Testing of Monolithic 3-D ICs.
Link: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=9537894

Paper2: find out a relevant paper to read

Problem Statement:
The broad idea of the problem is to activate the hidden delays due to the neighbouring effect in a
functional path and to test such delay. Many

It is a well established fact that the delay of a path depend on the activity of the nodes on that path.
Different inputs to the node induces different delays. Therefore, while generating/ applying a test pattern it is

important to consider the delay that the pattern induces. The most optimistic way to test the delay faults
would be to impose as much delay as possible in the path and then test it. Therefore, to induce the maximum
possible delay in a path the pattern should be capable of inducing the maximum delay. Two important problem
has to be solved: 1) How to induce the maximum delay, 2) Are the maximum activity pattern sufficient to
induce the maximum delay. Also the other problem that is to be addressed is the side effect of load in the
fan out module.

Our idea is also to test the paths which are likely to incur additional delay in the near future due to
aging effect. So the high activity test pattern would induce the additional delay which are caused to aging.
Definitely it is a topic for further discussion whether the low Vdd test or high activity patter test is
more suitable for aging related delay test?

Background reading: J. Segura, S.A. Bota,, J.L. Rossell, M. Rosales, "Low V_D_D vs. Delay: Is it Really a Good
Correlation Metric for Nanometer ICs?", , vol. 00, no. , pp. 358-363, 2006, doi: 10.1109/VTS.2006.44

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Project 5: Essential Testing: Fault grading based on criticality to the functionality of a design

Paper1: A. Chaudhuri, J. Talukdar and K. Chakrabarty, "Probabilistic Fault Grading for AI Accelerators using
Neural Twins," 2022 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Nicosia, Cyprus, 2022, pp.
333-338.
Link: https://ieeexplore.ieee.org/document/9912036

Paper2: Find out one paper relevant to this research work.

Problem Statement:
As the design gradually progress towards nano-scale transistors several, traditionally less
important, problems are emerging as a super challenge for modern processor design. Power consumption has
become an important problem for several reasons in the realm of processor and SoC design. Now, all the
contemporary designs are equipped with power-awareness in it. Often, it is observed that for the cause of
power-awareness most of the design technique includes a set of additional circuitry. Most of these additional
circuitry does not interfere in the functionality of the design, but they are essential for power regulation
or minimization. The observation from such design is that the presence of any structural fault in such
circuit should not matter in strict sense of functional correctness. The fault present in the augmented circuit
(the circuit which are used only for the purpose of secondary parameter optimization) does not affect the
correct functionality of the design, therefore, even in the presence of such fault the design could still be
categorized as a functionally correct.

Therefore, the idea is to identify those faults in such kind of circuit which would severely affect the
design specification.

Direction for Solution:
For such approach to succeed, it is essential that the design must be such that the augmented circuit must be isolated cleanly in terms of fault (stuck-at, delay faults etc.). Similarly we
could make the synthesis tool aware of such kind of design approach. We could target the augmented circuit
which are used for power minimization, for security, for debug and diagnosis. One quick approach is to find
out such path and declare them as false path and therefore the ATPG would bypass the test generation for
such path. There could be much more smarter methodology which would really evaluate the design considering
the presence of such faults.

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Project 6: Formal verification of low-power design

fvpower1: . Sharafinejad, B. Alizadeh and M. Fujita, "UPF-based formal verification of low power techniques
in modern processors," 2015 IEEE 33rd VLSI Test Symposium (VTS), Napa, CA, USA, 2015, pp. 1-6, doi:
10.1109/VTS.2015.7116288.

Paper2: find out one relevant paper to this research.

Problem statement:

The interesting part that is coming up now in the modern design is verification challenge. Due to complexity
of the design and somewhat shortage of specification the verification has become one of the challenging
problem. Simulation based approach is certainly a time consuming process, therefore, the property based
verification such as formal method has been taken with great seriousness for the modern design. Since the
modern designs are equipped with a lot more other circuitry for many other reasons apart from just the
functionality they pose a challenge in verification. Such design has to be verified for the purpose for
which they are designed to deliver. For example, the circuitry which are designed for power minimization
must be verified to see that the synthesized design meets the power specification. The recent development in
power specification such as UPF is one of the step towards a better solution to this problem.

Direction for Solution: A search must be in the direction of specification for power. If we chose to perform
a formal verification we need to have a language to specify the power such that it can capture the essential
properties which are intended for the designer. The next direction that must be addressed is to perform
formal method on such specification language.

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Project 7:

Any problem of your interest based on the course syllabus.

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