VLSI Term Project

Testing the Latent Delay Defects

Referred Papers:

1. **Logic Fault Diagnosis of Hidden Delay Defects** -Stefan Holst1, Matthias Kampmann2, Alexander Sprenger2, Jan Dennis Reimer2,Sybille Hellebrand2, Hans-Joachim Wunderlich3, and Xiaoqing Wen1
2. **Power Supply Noise-Aware At-Speed Delay Fault Testing of Monolithic 3-D IC**s by Shao-Chun Hung , Yi-Chen Lu , Sung Kyu Lim and Krishnendu Chakrabarty
   Link:
3. **Small-Delay Defect Detection in the Presence of Process Variations by** Rajeshwary Tayade _, Savithri Sundereswaran †, Jacob Abraham

Important Points:

Latent defects-hidden undetected flaws in testing which can't be identified by any user until some special set of operation are performed. These flaws can be detected only when a specific task is performed in unusual circumstances. Latent defects can cause undesirable delays in the circuit & affect circuit reliability. generally modeled as small-delay defects,

Aging is a technique of gradually increasing the priority of processes that wait in the system for a long time.

Paper 1:-

- Hidden delay defects (HDDs) are small delay defects that pass all at-speed tests at nominal capture time. It is important indicator of latent defects that lead to early-life failures and aging problems that are serious especially in autonomous and medical applications
- An effective way to screen out HDDs is to use Faster-than-At-Speed Testing (FAST) to observe outputs of sensitized non-critical paths which are expected to be stable earlier than nominal capture time.

- Normally Faster-than-At-Speed Testing (FAST) technique is used- effective way to screen out HDDs, to observe outputs of sensitized non-critical paths which are expected to be stable earlier than nominal capture time.
- Even with aggressive FAST testing, HDDs generate only very few failing test response bits
- Steps to overcome defects- presented the very first **logic fault diagnosis technique** that is able to identify HDD by analyzing fail logs produced by FAST.
- The technique uses **MRD back-propagation** to obtain initial HDD candidates which are then scored and ranked using simulation and variation-tolerant observation matching.
- The experimental results show a success rate of 94% even with very limited amount of failure data.
- FAST diagnosis established in this work provides the last missing component to rapidly improve yield and reliability by learning from otherwise unknown HDDs.

Paper 2

- Proposed a framework to conduct dynamic power and rail analysis for M3-D ICs.
- The magnitude of the voltage-droop problem in scan test mode depends on the switching activities in the top tier of a two-tier design.
- We can identify test pattern that are likely to fail a fault-free chip, that is, cause yield loss, due to the droop-induced added delay on sensitized paths
- Presented an ILP-based X-filling algorithm and a simulated annealing-based algorithm for M3-D pattern reshaping
- Experimental results for OpenCore and the ISPD 2012 benchmark show that the average WSA of the top tier is reduced after pattern reshaping and there is no decrease in the slack of sensitized paths.
- The proposed methods significantly mitigate the PSN-induced yield-loss problem during scan capture for M3-D designs. As part of ongoing work, we are assessing our solutions for M3-D designs with more than two tiers.

Paper 3

- One method to detect latent defects is to estimate the slack interval of the path being tested. In the presence of process variations, however, it is difficult to determine if the deviation in circuit delay is due to random process parameters or due to the presence of a latent defect.
- In this paper we analyze resistive interconnect defects (in this context) and suggest a test approach that will increase the probability of detection of small-delay defects that can otherwise escape detection due to the uncertainty caused by process variations.
- The paper addresses the problem of uncertainty in determining if the delay increment in a path is due to process variations or a resistive interconnect defect.
- The set of detectable delay defects through a net can be maximized when the smallest detectable (**Rdmin**) resistive open value through the net is minimized.
- A path selection procedure to find the minimum-Rdmin path through a net is proposed.
- The proposed approach increases the probability of detecting defects that would otherwise escape detection due to the uncertainty caused by process variations.