Indian Institute of Technology Tirupati

Department of Electrical Engineering

Digital VLSI Design (EE535L)

Instructor: Dr. Vikramkumar Pudi

Assignment 2

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Chapter 1

Assignments

1.1 Assignment 2

45 nm PTM model

1.1.1 Problem 1

Plot the voltage transfer characteristics (VTC) of a CMOS Inverter for β n/β p = 1, 2, 1⁄2 and 3.

a) Make all the observations and report your analysis

The transient analysis of the inverter is presented in the Fig. 1-3.

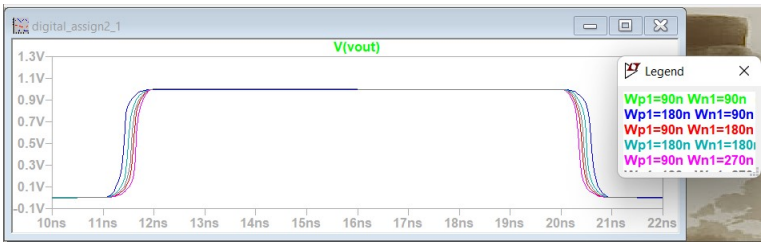

Figure 1.1: Transient analysis of inverter with various given β n/β p ratio

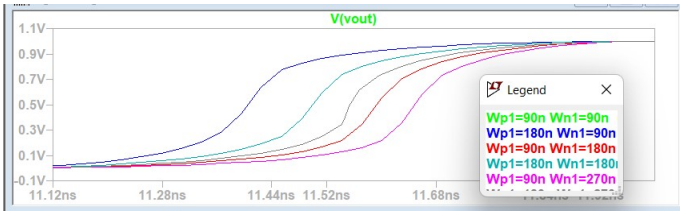

Figure 1.2: Transient analysis representing output voltage of inverter with various given β n/β p ratio

Figure 1.3: Transient analysis representing input and output voltage of inverter with various given β n/β p ratio

The voltage transfer characteristics is presented in Fig. 1.4 and 1.5. The VTC curve shifts to the left when β n/ β p >1. The VTC curve shifts to the right when β n/ β p <1.

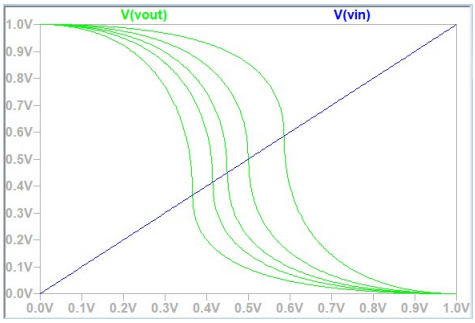

Figure 1.4: Voltage transfer characteristics of the inverter

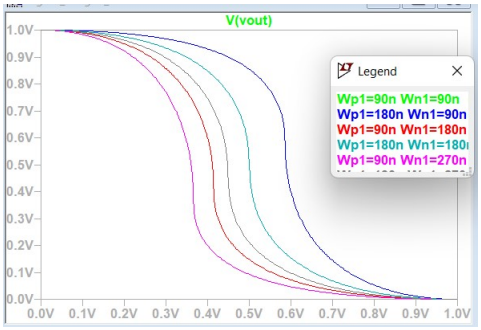

Figure 1.5: Voltage transfer characteristics of the inverter

b) Calculate the VOH, VOL, VIL, VIH for different βn/βp ratios

The Differentiation of the Vout is performed wrt to Vin using D operator and the point of -1 (slope) is mapped to the x and y- axis to obtain VOH, VOL, VIH and VIL. The vaules for different βn/βp is reported below. The Fig.1.6 shows the calculation of the voltage margines.

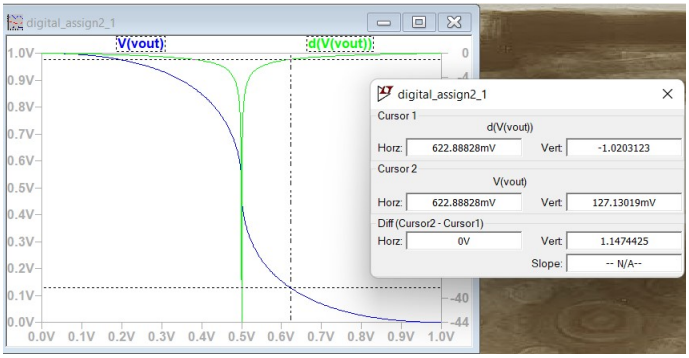

Figure 1.6: DVout/DVin graph

1) βn=βp=90nm

VOH=864.86 mV

VOL=127.13 mV

VIL=385.2 mV

VIH=622.88 mV

2) βn=180nm βp=90nm

VOH=874.26 mV

VOL=134.58 mV

VIL=286.103 mV

VIH=6510.62 mV

3) βn=90nm βp=180nm

VOH=865.417 mV

VOL=103.666 mV

VIL=488.28 mV

VIH=734.059 mV

4) βn=270nm βp=90nm

VOH=8867.36 mV

VOL=89.64 mV

VIL=551.498 mV

VIH=789.10082 mV

c) Obtain the Noise Margin levels for all the βn/βp ratios

The Noise margin is calculated as:

NM_H=VOH-VIH

NM_L=VIL-VOL

1) βn= βp=90nm

NM_H= 241.98 mV

NM_L=143.22 mV

2) βn=180nm βp=90nm

NM_H= 363.64 mV

NM_L=151.523 mV

3) βn=90nm βp=180nm

NM_H= 121.358 mV

NM_L=384.614 mV

4) βn=270nm βp=90nm

NM_H= 87.26 mV

NM_L=461.858 mV

d) Calculate the total power and dynamic power of the CMOS Inverter

The power waveform obtained by ploting Vdd*I(Vdd) is presented in Fig. 1.7

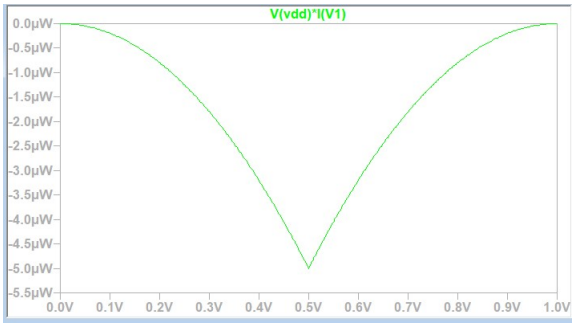

Figure 1.7: Power calculation, plot of Vdd*I

The average power is calculated using the tool and is presented in Fig. 1.8.

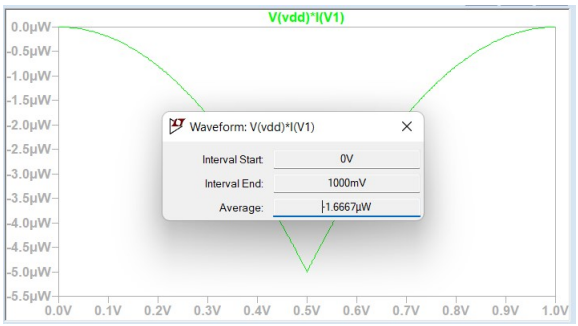

Figure 1.8: Average power calculation

The average power is obtained by plotting the product of the current drawn from the source and the voltage of the source. The dynamic power is the power drawn when both the transistors operate in the saturation region. This is obtained by mapping the Vin=Vout point in the curve and the corresponding power represents the dynamic power.

1) βn= βp=90nm

Avg Power =1.667 μW

Dynamic Power=5 μW

2) βn=90nm βp=180nm

Avg Power =2.2876 μW

Dynamic Power=6.85 μW

3) βn=180nm βp=90nm

Avg Power =2.2876 μW

Dynamic Power=6.85 μW

4) βn=270nm βp=90nm

Avg Power =2.6795 μW

Dynamic Power=8.0085 μW

Observation:

The power increases with the increase in the width.

e) Calculate the rise time, fall time and propagation delay for all the βn/βp ratios

The Propagation delay calculation waveform is given in the Fig. 1.9.

- The rise time is calculated in the output waveform as the time duration for the capacitor to charge from 10% to 90% of Vdd.
- The fall time is calculated in the output waveform as the time duration for the capacitor to discharge from 90% to 10% of Vdd.
- The propagation delay is calculated as the time duration form the 50% of the input waveform to the 50% of the output waveform.
  tp=(tph1+tpl2)/2

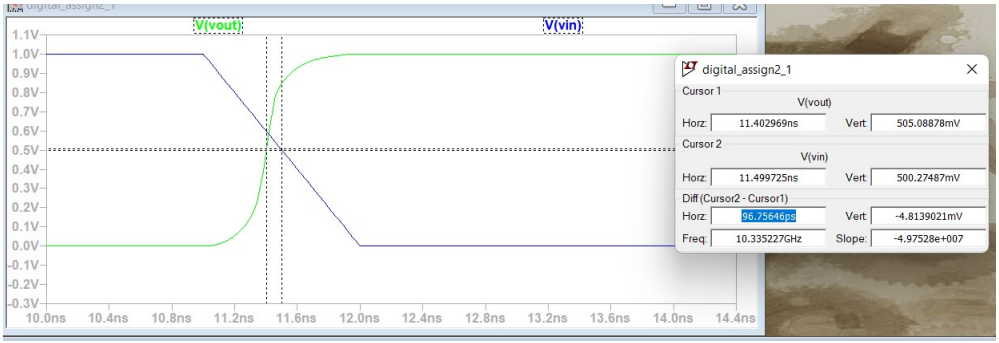

Figure 1.9: Propagation delay calculation

1) βn= βp=90nm

tr=307.2017ps

tf=308.72ps

tp=5.89ps

2) βn=180nm βp=90nm

tr=303.46ps

tf=299.835ps

tp=80.48ps

3) βn=90nm βp=180nm

tr=298.18ps

tf=301.26ps

tp=93.73ps

4) βn=270 βp=90nm

tr=285.8ps

tf=276.102ps

tp=153.13ps

Observation:

Delay increase when PMOS width is less beacuse of the pull up network strength.

f) Calculate the rise time and fall time for inverter-1 by varying the βn/βp ratio (1, 2, 1⁄2 and 3) of inverter-2.

The first inverter PMOS width is 180nm and NMOS width is 90nm. The variation in the width is for the second inverter. The rise and the fall time for inverter-1 are obtained as follows:

1) βn= βp=90nm

tr=296.866ps

tf=297.78ps

2) βn=180nm βp=90nm

tr=297.256ps

tf=297.78ps

3) βn=90nm βp=180nm

tr=297.56ps

tf=297.526ps

4) βn=270nm βp=90nm

tr=300.69ps

tf=299.303ps

Observation:

The rise and fall time is increasing the the increase in the width of the load inverter due loading effect (increase in the load capacitance).

1.1.2 Problem 2

Plot the Voltage Transfer characteristics of CMOS NAND and NOR gates and calculate the rise time, fall time and propagation delays (consider βn/βp = 1, 2, 1⁄2 and 3).

NAND

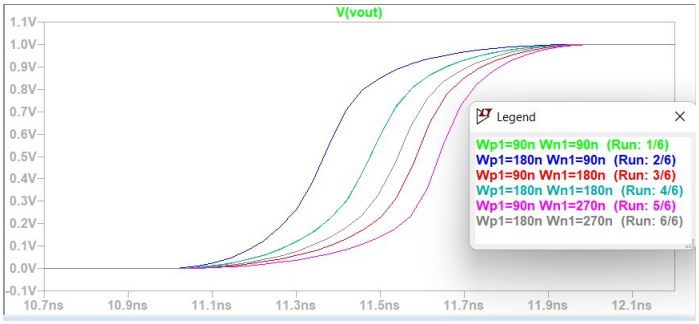

Figure 1.10: Transient analysis of NAND gate with one input fixed and other input variable

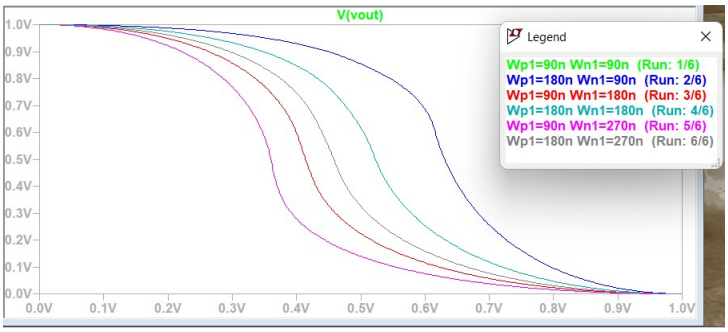

Figure 1.11: Voltage Tranfer characteristics of NAND gate with one input fixed and other input variable

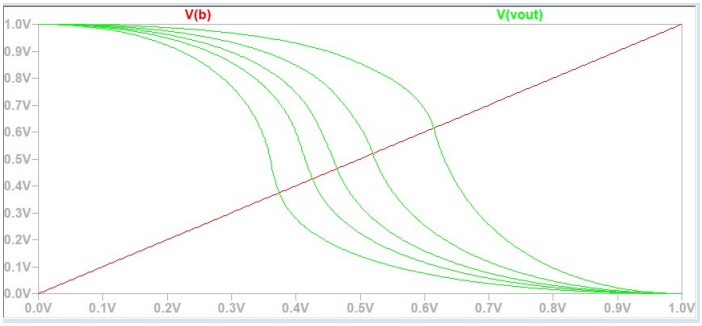

Figure 1.12: Voltage Tranfer characteristics of NAND gate with one input fixed and other input variable

1) βn= βp=90nm

tr=379.18ps

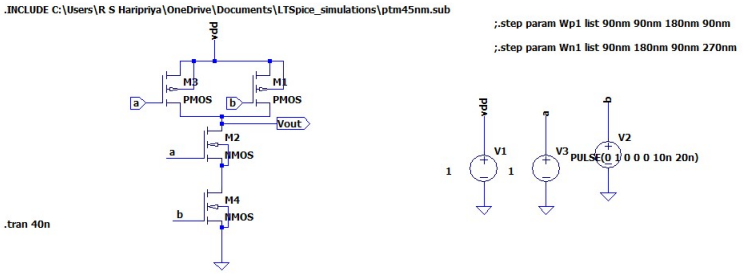

Figure 1.13: Schematic diagram of NAND gate

tf=375.634ps

tp=20.3045ps

2) βn=180nm βp=90nm

tr=366.135ps

tf=367.1405ps

tp=91.37ps

3) βn=90nm βp=180nm

tr=357.394ps

tf=353.765ps

tp=128.64ps

4) βn=270nm βp=90nm

tr=339.287ps

tf=339.945ps

tp=143.34ps

NOR

1) βn= βp=90nm

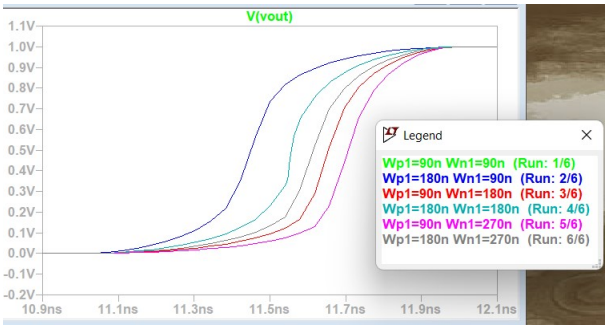

Figure 1.14: Transient analysis of NAND gate with one input fixed and other input variable

tr=336.97ps

tf=332.746ps

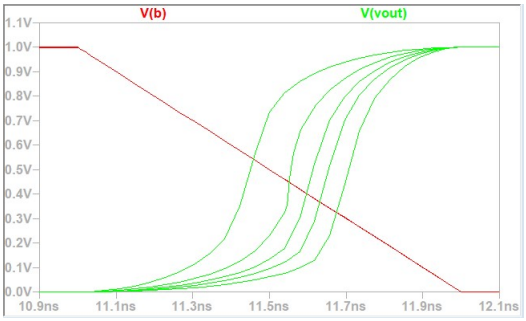

Figure 1.15: Transient analysis of NAND gate with one input fixed and other input variable

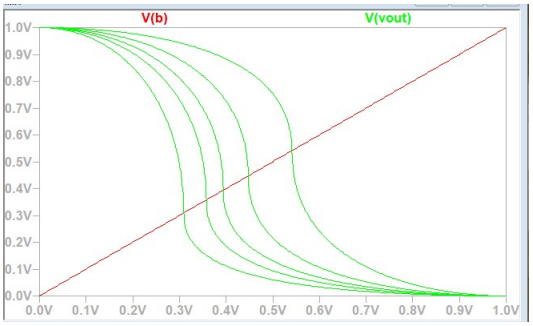

Figure 1.16: Voltage Tranfer characteristics of NOR gate with one input fixed and other input variable

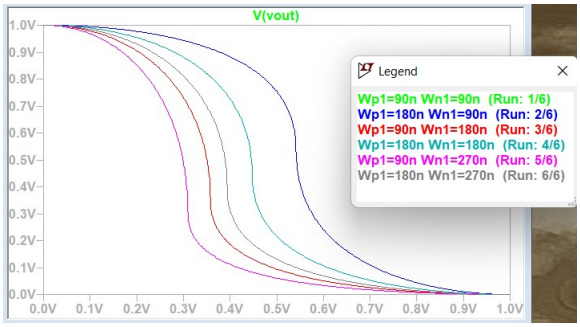

Figure 1.17: Voltage Tranfer characteristics of NOR gate with one input fixed and other input variable

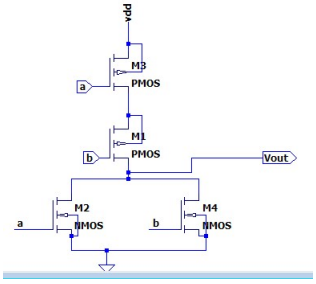

Figure 1.18: Schematic diagram of NOR gate

tp=48ps

2) βn=180nm βp=90nm

tr=340.1667ps

tf=341ps

tp=38.73ps

3) βn= βp=90nm

tr=287.63ps

tf=293.024ps

tp=158.544ps

4) βn= βp=90nm

tr=254.7945ps

tf=255.305ps

tp=228.58ps

Observation:

NAND delay is less than NOR delay.

32 nm PTM model

1.1.3 Problem 1

Plot the voltage transfer characteristics (VTC) of a CMOS Inverter for β n/β p = 1, 2, 1⁄2 and 3.

a) Make all the observations and report your analysis

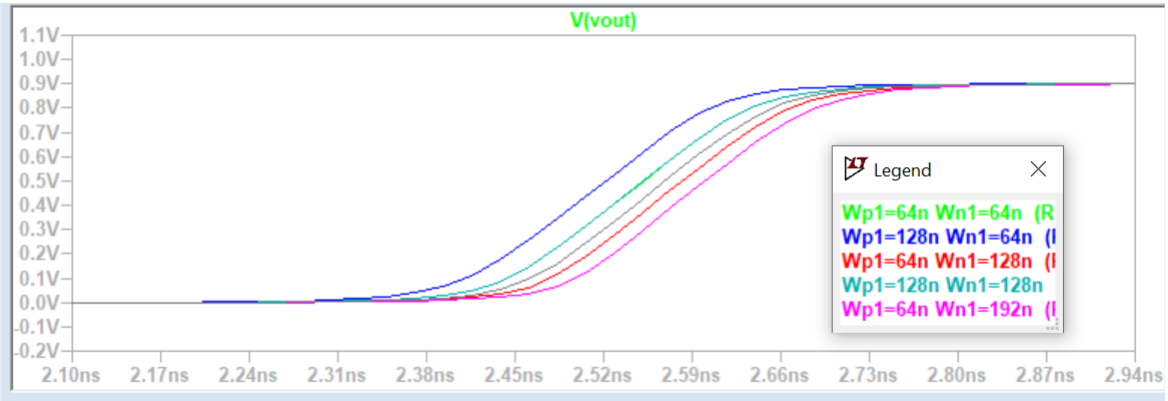

Figure 1.19: Transient analysis of inverter with various given β n/β p ratio

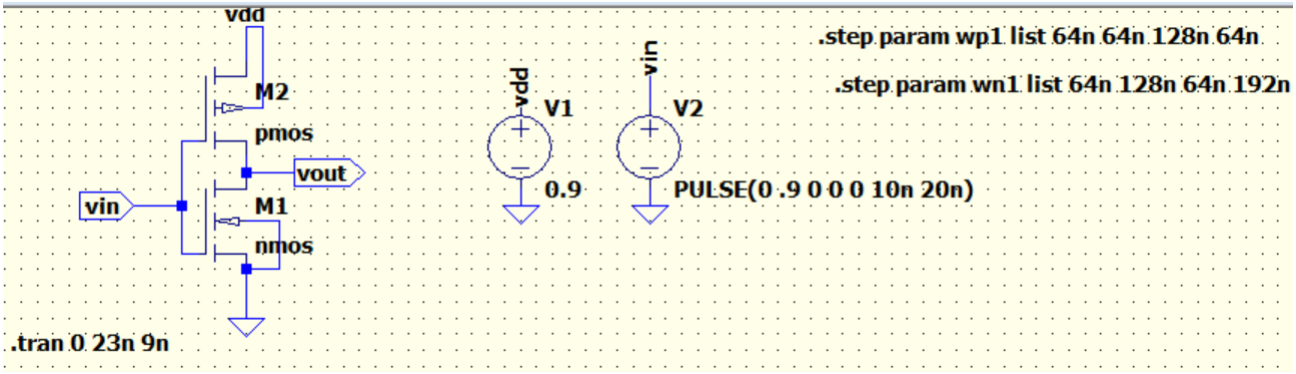

Figure 1.20: Inverter schematic

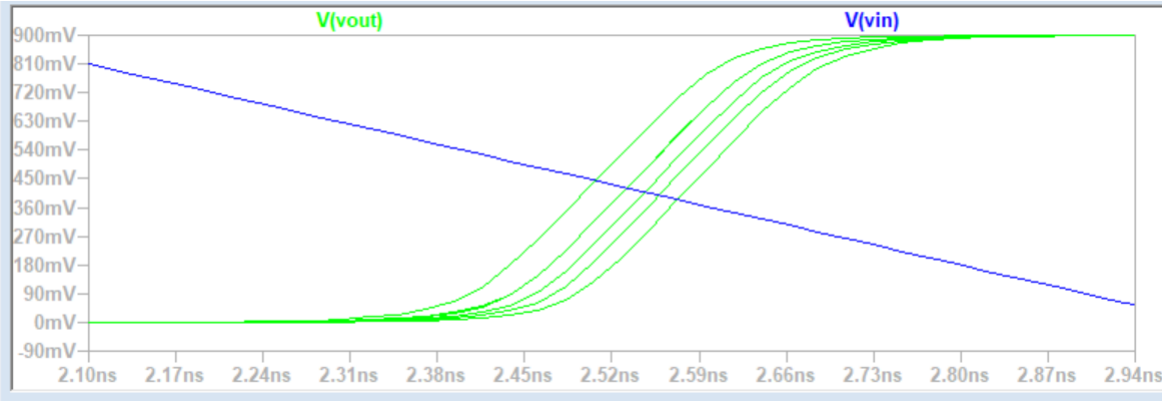

Figure 1.21: Transient analysis representing input and output voltage of inverter with various given β n/β p ratio

b) Calculate the VOH, VOL, VIL, VIH for different βn/βp ratios

1) βn=βp=64nm

VOH=853.451 mV

VOL=47.814 mV

VIL=303.074 mV

VIH=525.768 mV

2) βn=128nm βp=64nm

VOH=8854.676 mV

VOL=45.500 mV

VIL=270.131 mV

VIH=495.461 mV

3) βn=64nm βp=128nm

VOH=854.085 mV

VOL=49.134 mV

VIL=333.382 mV

VIH=557.343 mV

4) βn=192nm βp=64nm

VOH=855.322 mV

VOL=40.857 mV

VIL=253.001 mV

VIH=480.966 mV

c) Obtain the Noise Margin levels for all the βn/βp ratios

The Noise margin is calculated as:

NM_H=VOH-VIH

NM_L=VIL-VOL

1) βn= βp=64nm

NM_H= 327.683 mV

NM_L=255.260 mV

2) βn=128nm βp=64nm

NM_H= 360.215 mV

NM_L=224.631 mV

3) βn=64nm βp=128nm

NM_H= 296.742 mV

NM_L=284.248 mV

4) βn=192nm βp=64nm

NM_H= 374.356 mV

NM_L=4212.144 mV

d) Calculate the total power and dynamic power of the CMOS Inverter

1) βn= βp=64nm

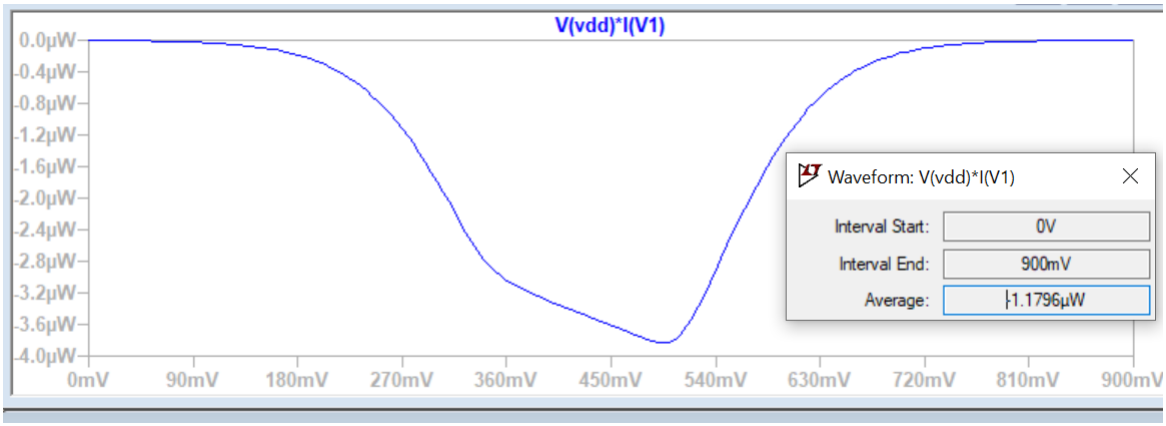

Figure 1.22: Average Power calculation, plot of Vdd*I

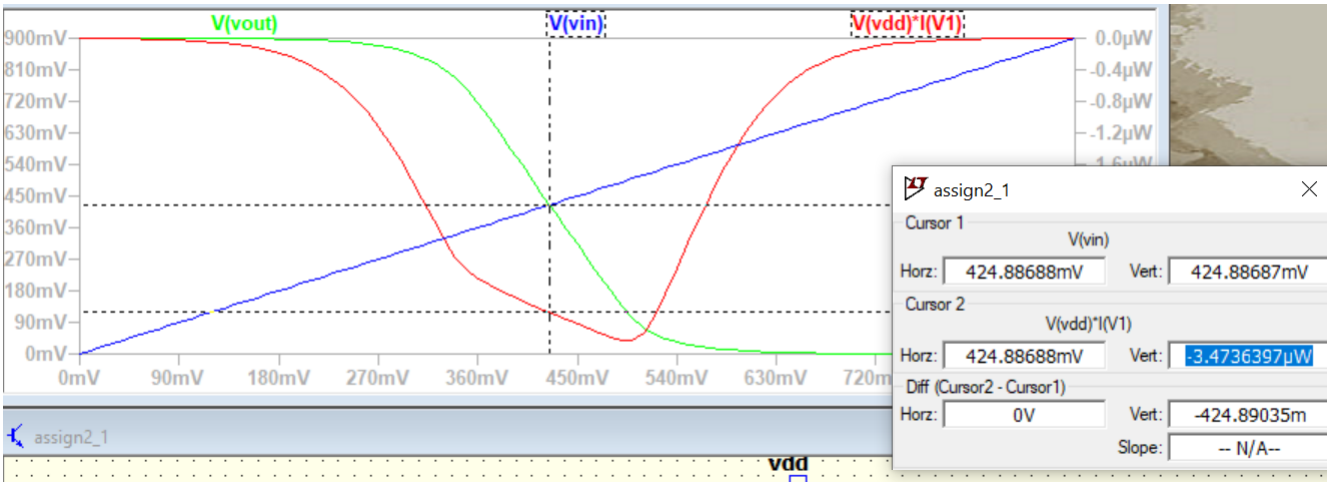

Figure 1.23: Dynamic power calculation

Avg Power =1.179 μW

Dynamic Power=3.834 μW

2) βn=128nm βp=64nm

Avg Power =1.664 μW

Dynamic Power=4.84 μW

3) βn=64nm βp=128nm

Avg Power =1.738 μW

Dynamic Power=5.13 μW

4) βn=192nm βp=64nm

Avg Power =1.980 μW

Dynamic Power=5.759 μW

e) Calculate the rise time, fall time and propagation delay for all the βn/βp ratios

1) βn= βp=64nm

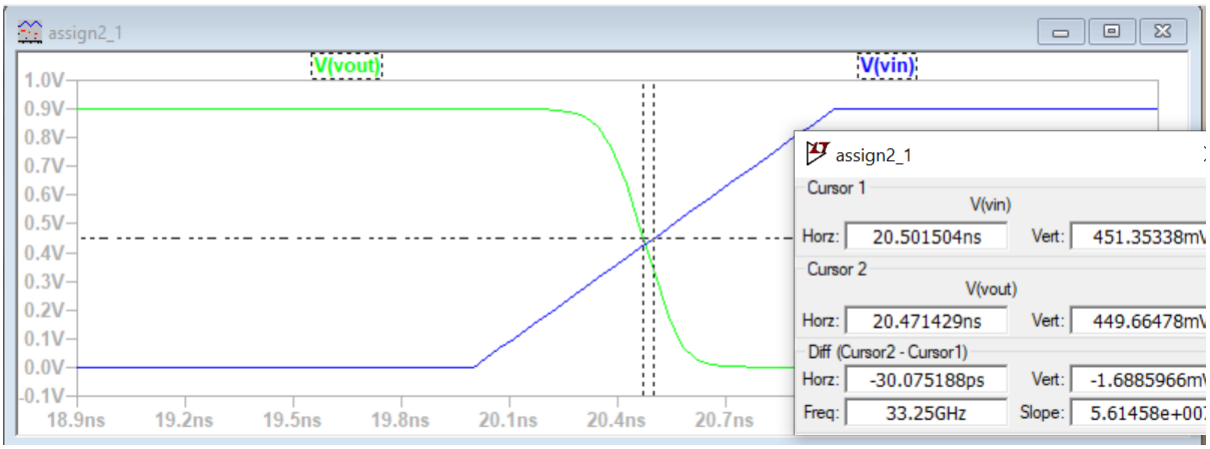

Figure 1.24: Propagation delay calculation

tr=217.32ps

tf=217.20ps

tp=30.07ps

2) βn=128nm βp=64nm

tr=220.51ps

tf=213.19ps

tp=59.35ps

3) βn=192 βp=64nm

tr=164.57ps

tf=142.98ps

tp=62.65ps

4) βn=64 βp=128nm

tr=218ps

tf=214ps

tp=1.42ps

f) Calculate the rise time and fall time for inverter-1 by varying the βn/βp ratio (1, 2, 1⁄2 and 3) of inverter-2.

The first inverter PMOS width is 128nm and NMOS width is 64nm. The variation in the width is for the second inverter. The rise and the fall time for inverter-1 are obtained as follows:

1) βn= βp=64nm

tr=228.905ps

tf=217.085ps

2) βn=128nm βp=64nm

tr=218.54ps

tf=215.63ps

3) βn=64 βp=128nm

tr=224.01ps

tf=224.06ps

4) βn=192 βp=64nm

tr=231.37ps

tf=216.54ps

1.1.4 Problem 2

Plot the Voltage Transfer characteristics of CMOS NAND and NOR gates and calculate the rise time, fall time and propagation delays (consider βn/βp = 1, 2, 1⁄2 and 3).

NAND

1) βn= βp=64nm

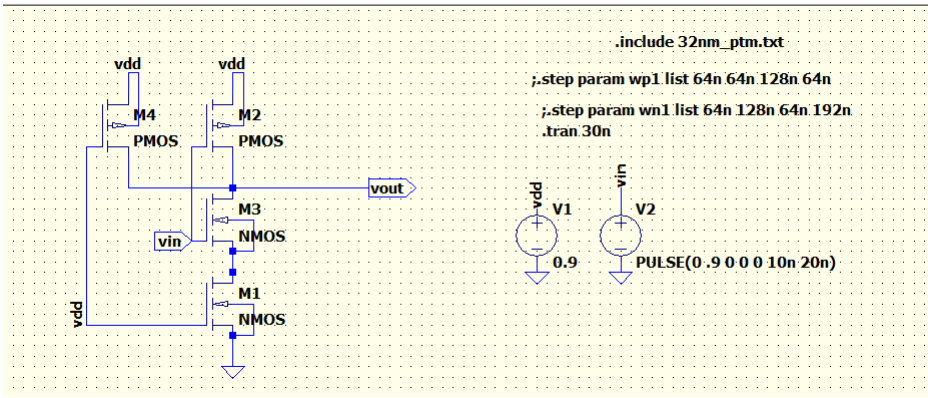

Figure 1.25: Schematic of NAND gate

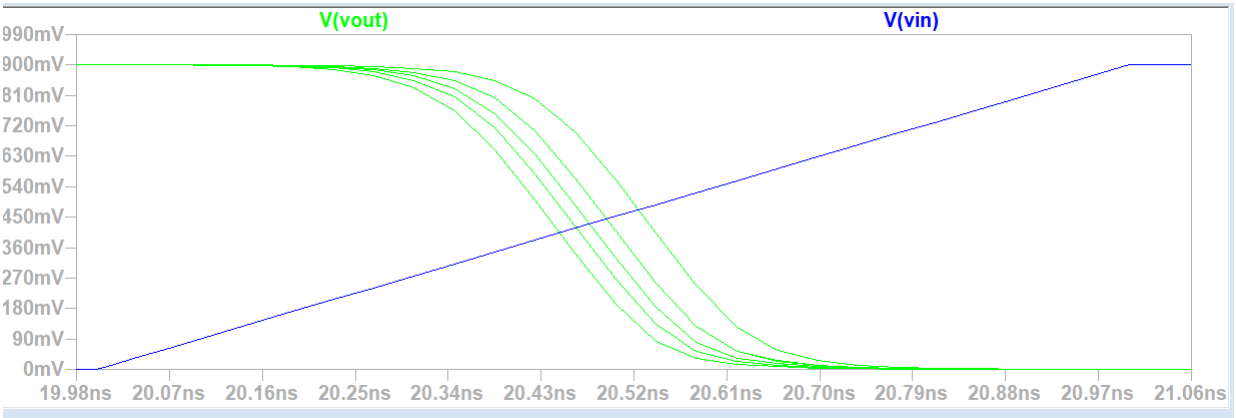

Figure 1.26: Transient analysis of Nand input and output with one input fixed and other input variable

tr=214.118ps

tf=211.720ps

tp=28.904ps

2) βn=128nm βp=64nm

tr=216.673ps

tf=215.453ps

tp=83.67ps

3) βn=64 βp=128nm

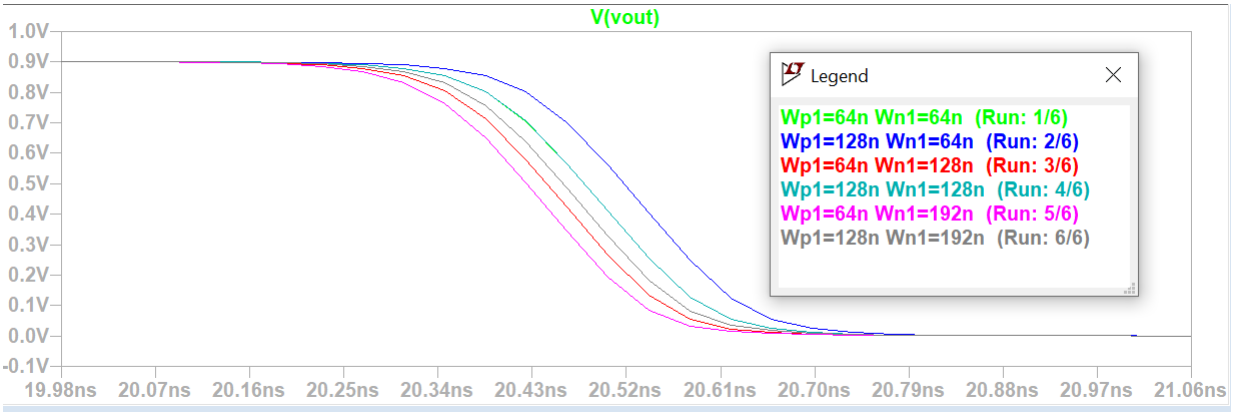

Figure 1.27: Transient analysis representing input and output voltage of Nand with various given β n/β p ratio

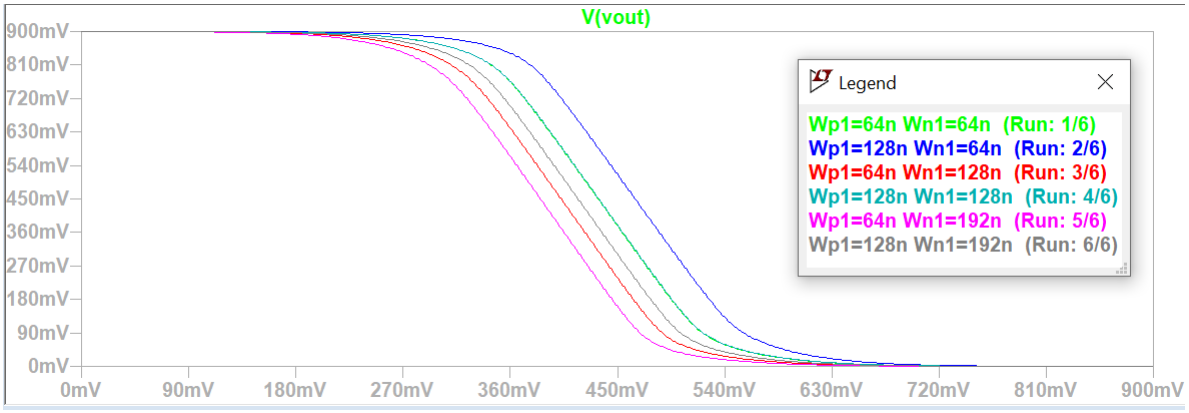

Figure 1.28: Voltage Tranfer characteristics of NOR gate with one input fixed and other input variable with various given β n/β p ratio

tr=219.121ps

tf=212.6185ps

tp=4.002ps

4) βn=192 βp=64nm

tr=209.44ps

tf=214.61ps

tp=83.324ps

NOR

1) βn= βp=64nm

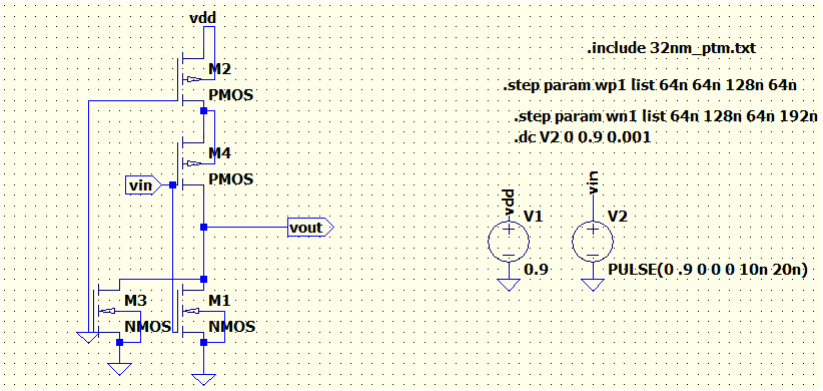

Figure 1.29: Schematic of Nor

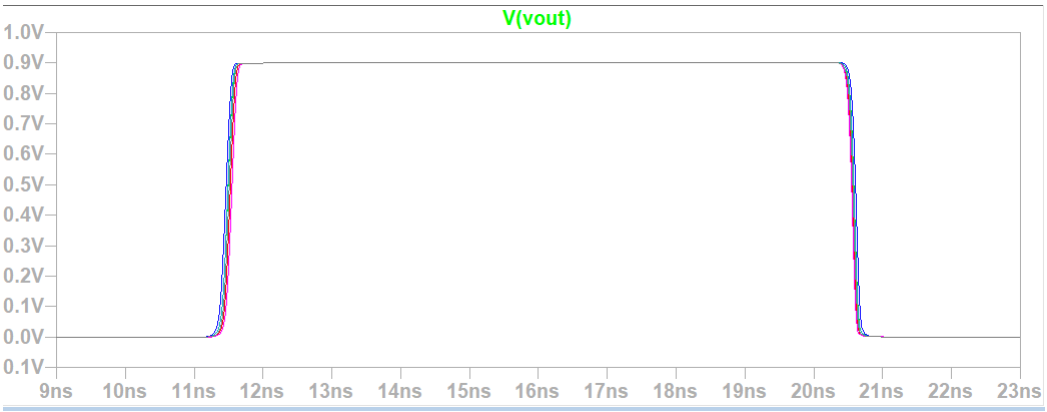

Figure 1.30: Transient analysis of Nor gate with one input fixed and other input variable

tr=158.754ps

tf=127.57ps

tp=81.712ps

2) βn=128nm βp=64nm

tr=155.381ps

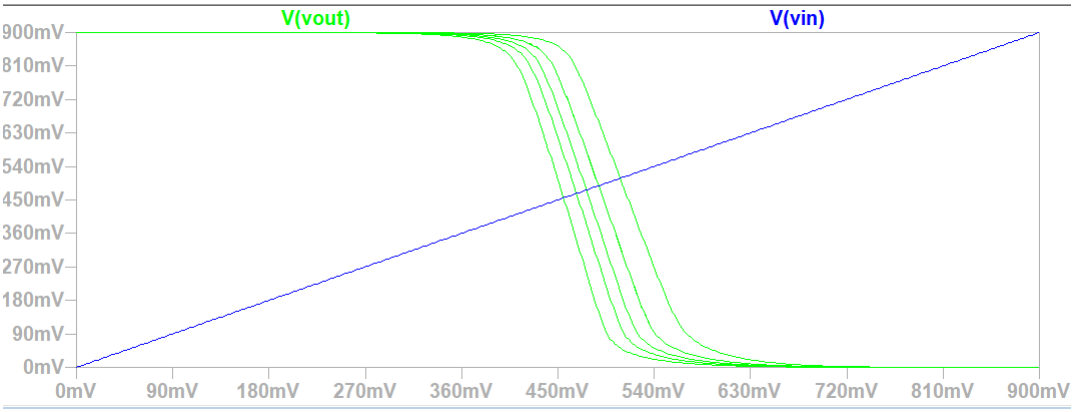

Figure 1.31: Voltage Tranfer characteristics of NOR gate with one input fixed and other input variable

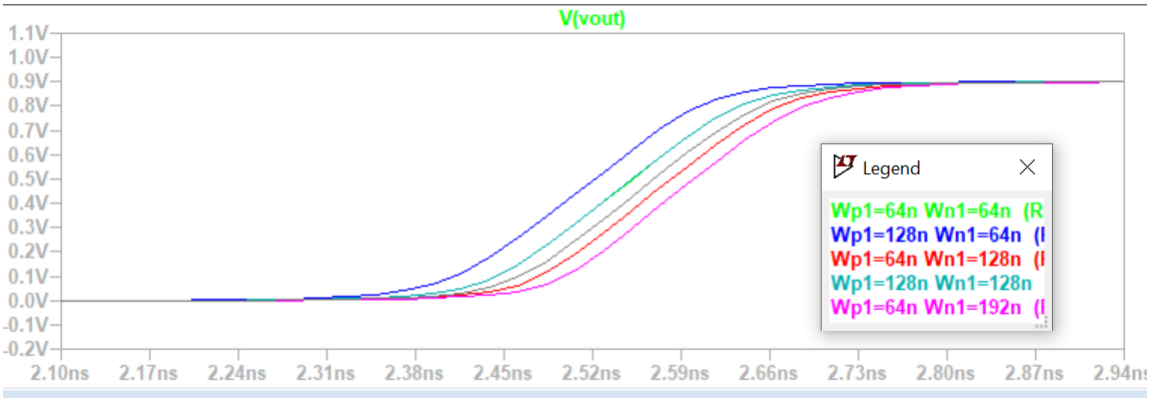

Figure 1.32: Transient analysis representing output voltage of Nor with various given β n/β p ratio

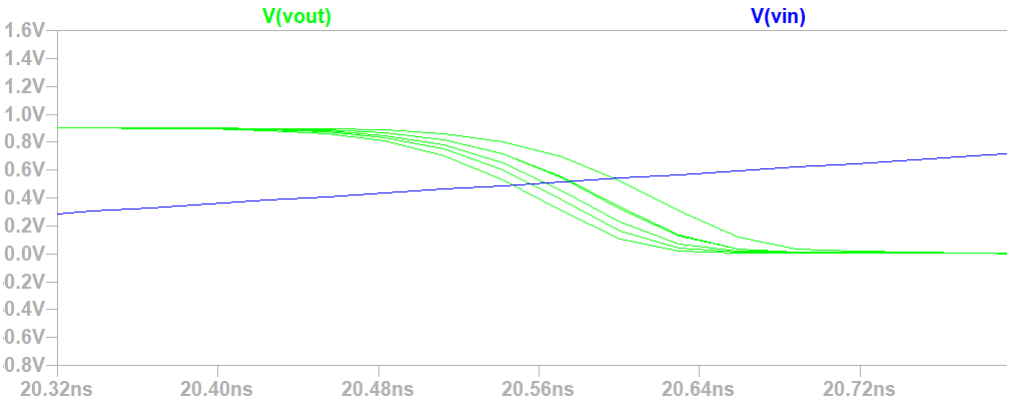

Figure 1.33: Transient analysis representing input and output voltage of Nor with various given β n/β p ratio

tf=127.404ps
tp=60.700ps
3) βn=64nm βp=128nm
tr=162.443ps
tf=132.240ps
tp=109.838ps
4) βn=192nm βp=64nm
tr=156.753ps
tf=123.680ps
tp=51.901ps

Observation:

- The power dissipation is more in 45nm than in 32nm.
- The delay is more in 45nm than in 32nm.
- In the NAND gate Fig. 1.13, if we apply the changing input in 'a', the waveform will be different from the waveform when the changing input is applied to 'b' due to threshold voltage variation (due to body effect).