Analyze the following circuits presented in the papers.
From the paper entitled as "

A Novel High-Speed and Energy Efficient
10 Transistor Full Adder Design", consider Fig.6 (all circuits) and Fig.4. Analyze the circuits presents in the Fig.6 in LtSpice with proper W/L ratios and compare the obtained results with Fig.4 Demonstrate your observations why the Fig.4 is better ?

Form the paper entitled as "

Design of Low Area and Low Power Systolic Serial
Parallel Multiplier using CNTFETs", consider Fig.4 and simulate it LtSpice and report your observations. If the voltage levels are not rail to rail swing, modify the circuit accordingly