A Novel High-Speed and Energy Efficient 10-Transistor Full Adder Design

Jin-Fa Lin, Yin-Tsung Hwang, *Member, IEEE*, Ming-Hwa Sheu, *Member, IEEE*, and Cheng-Che Ho

***Abstract*—In this paper, we propose a novel full adder design using as few as ten transistors per bit. Compared with other low-gate-count full adder designs using pass transistor logic, the proposed design features lower operating voltage, higher computing speed and lower energy (power delay product) operation. The design adopts inverter buffered XOR/XNOR designs to alleviate the threshold voltage loss problem commonly encountered in pass transistor logic design. This problem usually prevents the full adder design from operating in low supply voltage or cascading directly without extra buffering. The proposed design successfully embeds the buffering circuit in the full adder design and the transistor count is minimized. The improved buffering helps the design operate under lower supply voltage compared with existing works. It also enhances the speed performance of the cascaded operation significantly while maintaining the performance edge in energy consumption. For performance comparison, both dc andperformances of the proposed design against various full adder designs are evaluated via extensive HSPICE simulations. The simulation results, based on TSMC 2P4M 0.35-μm process models, indicate that the proposed design has the lowest working V_{dd} and highest working frequency among all designs using ten transistors. It also features the lowest energy consumption per addition among these designs. In addition, the performance edge of the proposed design in both speed and energy consumption becomes even more significant as the word length of the adder increases.**

***Index Terms*—Energy efficient, full adder design, low-voltage operation, pass transistor logic.**

I. Introduction

With the advance of VLSI technology, many computing intensive applications such as multimedia processing, digital communication can now be realized in hardware to either speed up the operation or reduce the power/energy consumption. The essence of the digital computing lies in the full adder design. The design criteria of a full adder are usually multi-fold. Transistor count is, of course, a primary concern which largely affects the design complexity of many function units such as multiplier and algorithmic logic unit (ALU). Two other important yet often conflicting design criteria are power consumption and speed. A better metric would be the power delay product or energy consumption per operation to indicate the optimal design tradeoffs. Related to the power consumption is the lowest supply voltage in which the design can still operate properly. Numerous full adder designs [1]–[8] in the categories of static CMOS, dynamic circuit, transmission gate, or pass transistor logic have been presented in the literature. The full adder design in static CMOS with complementary pull-up pMOS and pull-down nMOS networks is the most conventional one but it requires as many as 28 transistors. Dynamic circuits can significantly reduce the transistor count but the incurred power consumption, including that of the clock tree, is usually high. Building logic in transmission gate is another alternative to reduce the circuit complexity. In [1], a transmission gate plus inverter based full adder design using 20 transistors was presented. The circuit can operate with full output voltage swing. In [2], the designs were further reduced to only 16 transistors while maintaining the full output voltage swing operation. To pursue even lower transistor count full adder designs, pass transistor logic (PTL) can be used in lieu of transmission gate. In [3], PTL based XOR/XNOR circuits were devised using only 4 transistors. Despite the saving in transistor count, the output voltage level is degraded at certain input combinations. This XOR circuit was adopted in [4] and the full adder design consists of only 14 transistors. In this design, an inverter is employed to generate the complementary signal of $A \oplus B$. The design also features full swing operations. The design was further improved in [5], where a 16-transistor full adder design was proposed. At the cost of two additional transistors, this design can eliminate the inverter from the critical path and thus avoid the possible short circuit power consumption for low power operation.

As the designs with fewer transistor count and lower power consumption are pursued, it becomes more and more difficult and even obsolete to keep full voltage swing operation. Note that in pass transistor logic, the output voltage swing may be degraded due to the threshold loss problem. That is, the output high (or low) voltage is deviated from the V_{dd} (or ground) by a multiple of threshold voltage V_T. The reduction in voltage swing, on one hand, is beneficial to power consumption. On the other hand, this may lead to slow switching in the case of cascaded operation such as ripple carry adder. At low V_{dd} operation, the degraded output may even cause circuit malfunction. Therefore, for designs using reduced voltage swing, special attention must be paid to balance the power consumption and the speed. In [6], a PTL based new static energy-recovery full (SERF)

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adder with as few as ten transistors was presented. In spite of its claimed superiority in energy consumption, the design is relatively slower than peer designs and cannot be cascaded at low V_{dd} operation due to multiple-threshold loss problem. In [7], improved 10-transistor full adder designs were derived based on systematic exploration of the combinations of various XOR/XNOR, Sum and Cout modules. Out of 41 circuit combinations, three designs with better power consumption were selected. Again, these designs suffer from the severe threshold loss problem and cannot operate properly in cascade under low supply voltage. The lowest possible power supply is limited to $2V_{Tn} + V_{Tp}$, where V_{Tn} and V_{Tp} are the threshold voltages of nMOS and pMOS respectively. In [8], another 10-transistor full adder design consisting of two pass transistor based XORs and a 2-to-1 multiplexer was presented. Its Cout voltage swing $(V_{dd} - V_{Tn} \sim 2V_{Tp})$ is degraded by a total of 3 V_T's. As usual, the cascaded operation in low supply voltage becomes problematic. In this paper, we will propose a novel 10-transistor full adder design with alleviated threshold loss problem. This leads to faster ripple carry additions while maintaining the performance edge in energy consumption per operation. The design can also sustain lower V_{dd} operation than peer designs.

II. Proposed CLRCL Full Adder Cell

A. Basic Building Blocks

The logic function of a full adder can be represented as

$$\text{Sum} = (A \oplus B) \oplus C\text{in} \tag{1}$$

$$C\text{out} = A \cdot B + C\text{in} \cdot (A \oplus B). \tag{2}$$

The above equations can rewritten as

$$\text{Sum} = (A \odot B) \cdot C\text{in} + (A \oplus B) \cdot \overline{C\text{in}} \tag{3}$$

$$C\text{out} = (A \oplus B) \cdot C\text{in} + (A \odot B) \cdot A. \tag{4}$$

From (3) and (4), we can easily identify two basic modules needed in implementing the functions, i.e., XOR and 2-to-1 multiplexer. As illustrated in Fig. 1, an XOR/XNOR function can be achieved with only 4 transistors in PTL [3]. Circuits in (a) and (b) are inverter based structures while circuits in (c) and (d) are PTL based structures. Assume both inputs have full voltage swing, the output voltages subject to different input combinations are compiled in Table I. In inverter based circuits, both output high and low voltages are degraded by the magnitude of a threshold voltage under certain input combinations. In PTL based circuits, the situation is improved and only output high or output low voltage is degraded. If the degraded output is used to control the gate of the subsequent stage in pass transistor logic, further voltage degradation may occur. However, degraded outputs do not necessarily imply adverse effect on the circuit performance. It depends on whether they cause further voltage drop in the following stage or not.

As for the 2-to-1 multiplexer, possible circuit designs are illustrated in Fig. 2. In (a), two transmission gates are employed and complementary select control signals are required. Despite its merit of full output voltage swing, the circuit complexity is considered too high. In (b)–(d), pass transistors are used in lieu of the transmission gate to reduce the circuit complexity. The price to pay is the degraded output voltage swing. Assume all inputs have full voltage swings, the output voltage levels of these circuits are summarized in Table II.

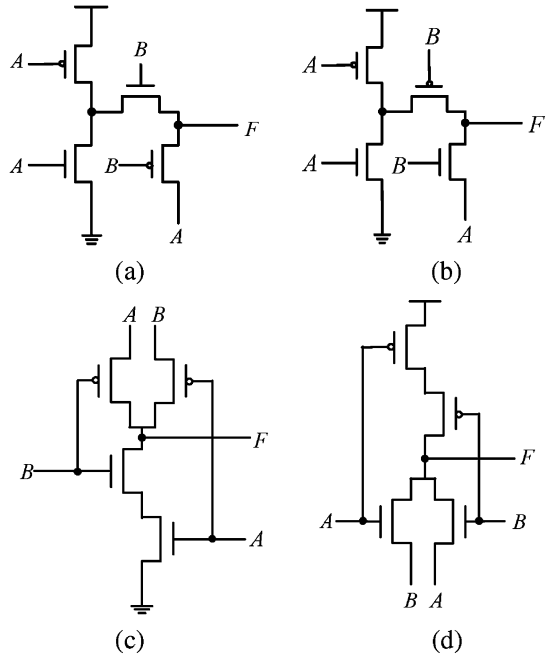

Fig. 1. 4-transistor XOR/XNOR circuits.

TABLE I
Output Voltage Levels of the 4T XOR/XNOR Circuits

inputs		(a)	(b)	(c)	(d)
A	*B*	XOR	XNOR	XOR	XNOR
0	0	$\lvert V_{Tp}\rvert$	V_{dd}	$\lvert V_{Tp}\rvert$	V_{dd}
0	1	V_{dd}-V_{Tn}	*Gnd*	V_{dd}	*Gnd*
1	0	V_{dd}	$\lvert V_{Tp}\rvert$	V_{dd}	*Gnd*
1	1	*Gnd*	V_{dd}-V_{Tn}	*Gnd*	V_{dd}-V_{Tn}

B. Full Adder Design With CLRCL

In this paper, we will propose a novel full adder design featuring complementary and level restoring carry logic (CLRCL). The goal is to reduce the circuit complexity and to achieve faster cascaded operation. The strategy is to avoid multiple threshold voltage losses in carry chain by proper level restoring. We first rewrite the full adder Sum and Cout Boolean functions as

$$\text{Sum} = (A \oplus C\text{in}) \cdot \overline{C\text{out}} + (A \odot C\text{in}) \cdot B \tag{5}$$

$$C\text{out} = (A \oplus C\text{in}) \cdot B + (A \odot C\text{in}) \cdot A. \tag{6}$$

The logic block diagram of the proposed design is shown in Fig. 3. The design rationales are as follows: First, try to avoid the usage of degraded output in the following stage as gate control signals. This is the common problem existing in most 10-transistor full adder designs. It will lead to multiple threshold voltage losses and may hinder the cascaded circuit from correct operation. Second, try to eliminate unbuffered carry signal propagation in a pass transistor chain. According to Elmore formula,

TABLE II
COMPARISON OF 2-TO-1 MULTIPLEXER CIRCUITS

2-to-1 multiplexer circuits	Transistor count	Complementary control select	Output high (min)	Output low (max)
(a) transmission gate	4	Yes	V_{dd}	*Gnd*
(b) pass transistor	2	No	V_{dd}-V_{Tn}	$\|V_{Tp}\|$
(c) double NMOS	2	Yes	V_{dd}-V_{Tn}	*Gnd*
(d) double PMOS	2	Yes	V_{dd}	$\|V_{Tp}\|$

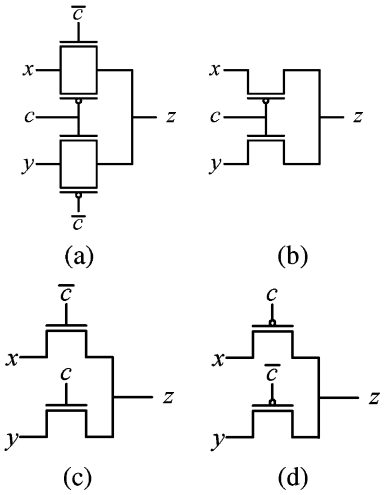

Fig. 2. 2-to-1 multiplexer circuits.

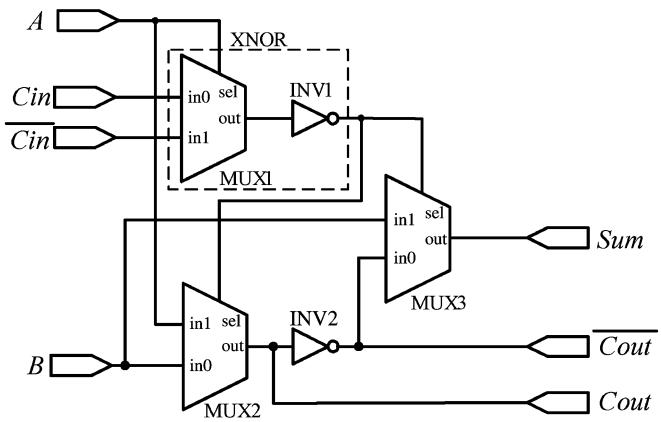

Fig. 3. Logic block diagram of the CLRCL full adder.

the propagation delay is a quadratic function of the number of cascaded pass transistors. Even for moderate number of cascade length, the delay is still intolerable.

As shown in Fig. 3, the XNOR circuit adopted in the proposed design is realized by a 2-to-1 multiplexer followed by an inverter. The role of the inverter is 3-fold. Firstly, it is used as a level restoring circuit to combat the output threshold voltage loss. The level restored output is then fed to MUX 2/3 to generate Sum and Cout signals. The threshold voltage loss of Sum and Cout will be confined to only one $|V_T|$ away from the power supplies. Secondly, the inverter (INV 2) serves as a buffer along the carry chain to speed up the carry propagation. Thirdly, the inverter (INV 2) provides complementary signals needed in the following stage. The availability of complementary signals also helps simplify the XNOR design, where only one signal is

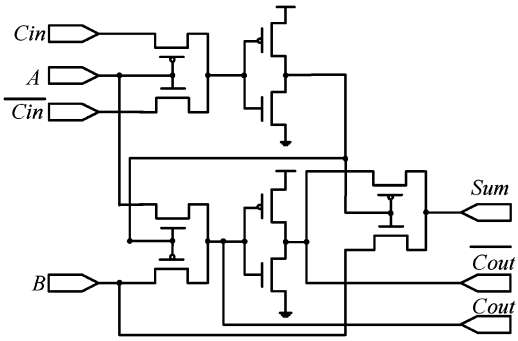

Fig. 4. MOS circuit schematic design of the CLRCL full adder.

needed in selection control. The MOS circuit schematic design of a CLRCL full adder is depicted in Fig. 4. We adopt the circuit in Fig. 2(b) to implement the 2-to-1 multiplexer in that it is the one without using complementary select controls. The entire full adder circuit requires only ten transistors (5 pMOS and 5 nMOS)—the one with the least transistor count we have learned so far from the literature. In the following section, we will conduct various analyses and simulations to demonstrate the performance superiority of the proposed adder over other designs.

III. PERFORMANCE ANALYSES AND SIMULATION RESULTS

A. Other Comparable Full Adder Designs

In this paper, several comparable full adder designs are included for performance comparison. Since the design goals are low circuit complexity and high-speed operation subject to competitive energy consumption, we focus mainly on low- gate-count and static pass transistor based full adder designs. Besides the proposed CLRCL full adder design, nine more designs are employed in our comparison. The first one, denoted as 28T, is a static CMOS logic design containing 28 transistors. This design, as shown in Fig. 5(a), is used as the basis of comparison. It has a full voltage swing and buffered Sum and Cout signals. The second one denoted as TG-CMOS is shown in Fig. 5(b). It contains 20 transistors and uses only transmission gates and inverters to implement XOR and multiplexing functions.

The third one called transmission-function full adder (TFA) is illustrated in Fig. 5(c). It consists of 16 transistors. The basic XOR circuit used in the design requires one of its two inputs in complementary forms. An additional inverter is thus needed, which leads to a 6-transistor XOR design. The design employs 4 CMOS transmission gates and can achieve full voltage swing operations. The fourth one [4] is a 14T full adder design as

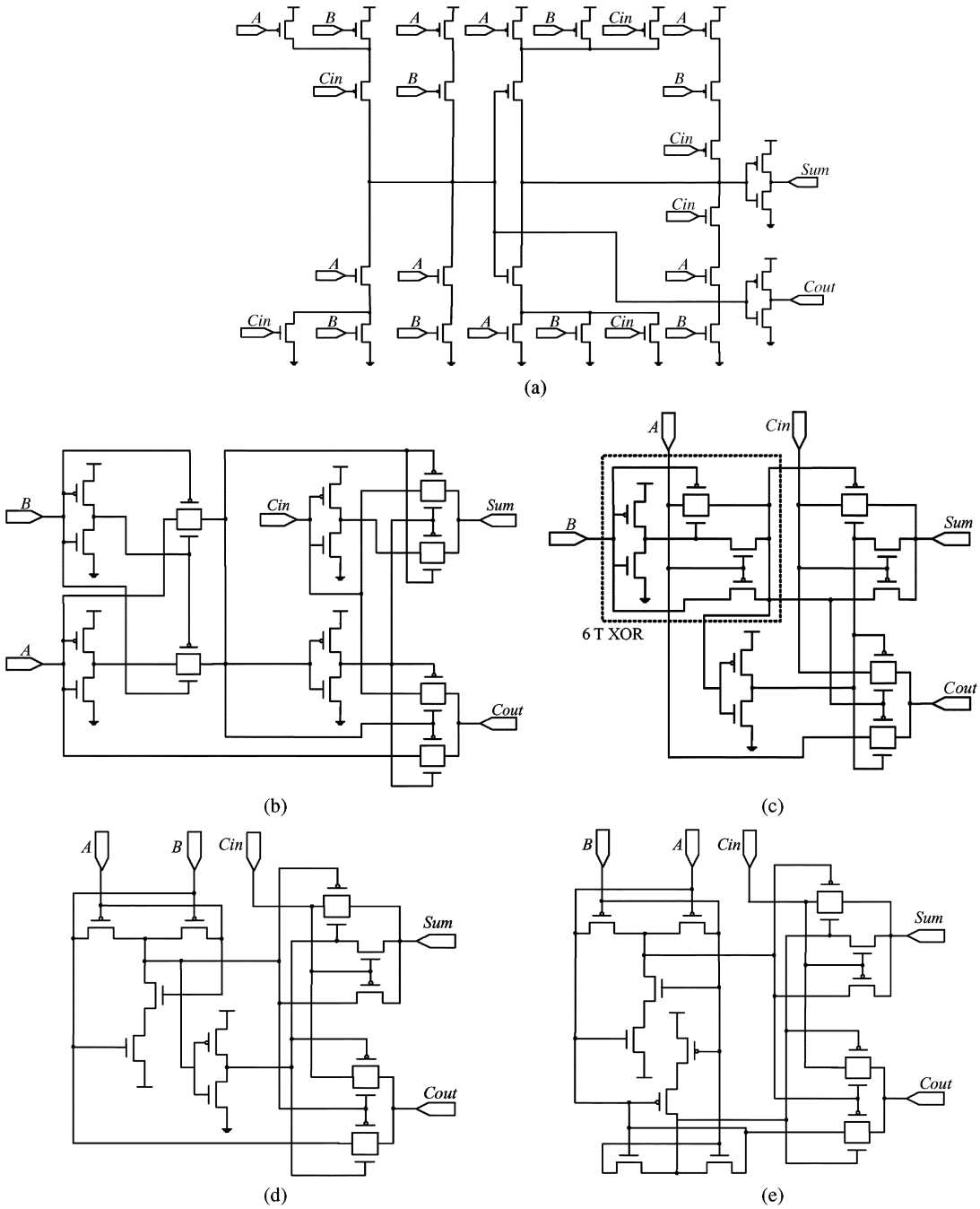

Fig. 5. High-gate-count full adder designs. (a) Static CMOS full adder design-28T. (b) Transmission gate based CMOS full adder design—TG-CMOS. (c) TFA full adder design. (d) 14T full adder design. (e) 16T full adder design.

shown in Fig. 5(d). It contains a 4T XOR circuit [the same as the one in Fig. 1(c)], an inverter and two transmission gate based multiplexer designs (same as those used in TFA) for Sum and $C\mathrm{out}$ signals. Despite the threshold voltage loss in internal nodes, this design maintains a full output voltage swing. The fifth one, as shown in Fig. 5(e) and denoted as 16T, is derived from the 14T design. Instead of using an inverter to generate the complementary signal of $A \oplus B$, a 4-transistor XNOR circuit Fig. 1(d) is employed to eliminate the possible short circuit power consumption introduced by the inverter. Similar to the 14T design, it has a threshold voltage loss problem in internal nodes but the loss is not propagated to the output nodes. The sixth one [6] is the first 10-transistor full adder design in the literatures. The design, denoted as SERF (static energy recovery full adder), emphasizes the low power consumption. As shown in Fig. 6(a), it uses two 4-transistor XNOR circuits Fig. 1(d) and one 2-to-1 multiplexer Fig. 2(b). The design is claimed to be extremely low power because it doesn't contain direct path to the ground and it can re-apply the load charge to the control gate (energy recovery). The seventh to the ninth designs under comparison are presented in [7]. They are derived from a systematic exploration of circuit combinations from various XOR/XNOR and 2-to-1 MUX modules. These circuits, denoted as 9A, 9B and 13A, are the best three out of 41 possible com-

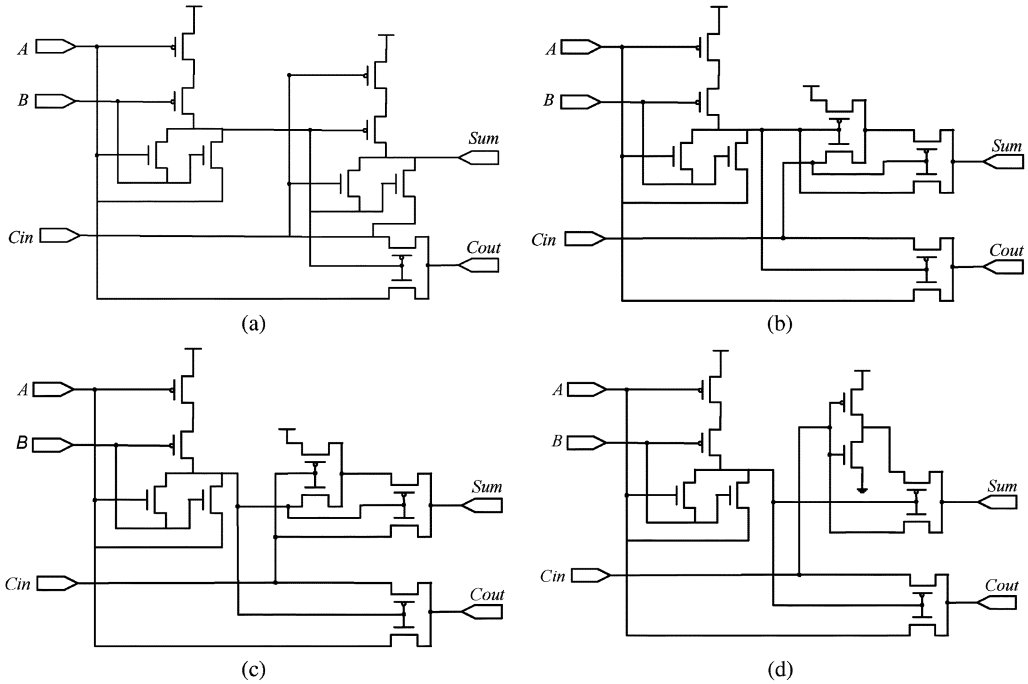

Fig. 6. Conventional 10T full adder designs. (a) SERF full adder design. (b) 9A full adder design. (c). 9B full adder designs. (d) 13A full adder designs.

binations. The designs are illustrated in Fig. 6(b)–(d). Note that designs SERF, 9A, 9B, and 13A are the ones with minimum transistor count (10) known in the literatures so far.

B. Circuit Analyses and Simulation Results of a Single Full Adder

We will first conduct static circuit analyses to determine the voltage swings of different adder designs. We compare only those 10-transistor (10T in short) designs, where the threshold voltage loss problem comes hand in hand with the low-gate-count approach. Among the three inputs of a full adder, inputs A and B are assumed to be perfect and have full voltage swing (from V_{dd} to Gnd). InputCin, however, is drawn from the $Cout$ of another full adder to faithfully reflect the situation of cascaded operation in most parallel adder designs. In other words, Cin signal might be degraded due to the threshold voltage loss. The theoretical analysis results are summarized in Table III. For simplicity, body effect is ignored and all nMOS (pMOS) transistors are assumed to have a fixed threshold voltage $V_{Tn}(V_{Tp})$. Note that the two values in each table entry for the proposed CLRCL circuit correspond to $Cout$ and $\overline{Cout}$ respectively. Among these 10T designs, SERF, 9A, 9B and 13A all have double threshold voltage losses in $Cout\_high$. The proposed CLRCL design, however, encounters only one threshold voltage loss along the unbuffered $Cout$ signal. Similarly, all other 10T designs encounter 2 threshold voltage losses in $\mathrm{Sum\_high}$ signal while the proposed CLRCL design suffers only one threshold voltage loss. In consequence, the proposed design requires the minimum V_{dd} among all 10T designs. Besides theoretical analyses, the HSPICE simulation results are given in Table IV.

The simulations are based on circuit dc analysis using TSMC 0.35-μm 2P4M [9] process and a 3.3-V power supply (except $V_{dd,\min}$ simulations). Typical transistor sizes, i.e., $(W/L)_{\mathrm{p}} = 2\ \mu\mathrm{m}/0.35\ \mu\mathrm{m}$ and $(W/L)_{\mathrm{n}} = 1\ \mu\mathrm{m}/0.35\ \mu\mathrm{m}$ are employed.

TABLE III
THEORETICAL DC ANALYSIS RESULTS OF DIFFERENT 10T FULL ADDER DESIGNS

Designs	$Cout\_high_{min}$	$Cout\_low_{max}$	Sum_high_{min}	Sum_low_{max}	$V_{dd,min}$
SERF	V_{dd}-$2V_{Tn}$	$\lvert V_{Tp}\rvert$	V_{dd}-$2V_{Tn}$	*Gnd*	$2V_{Tn}+\lvert V_{Tp}\rvert$
9A	V_{dd}-$2V_{Tn}$	$\lvert V_{Tp}\rvert$	V_{dd}-$2V_{Tn}$	$\lvert V_{Tp}\rvert$	$2V_{Tn}+\lvert V_{Tp}\rvert$
9B	V_{dd}-$2V_{Tn}$	$\lvert V_{Tp}\rvert$	V_{dd}-$2V_{Tn}$	$\lvert V_{Tp}\rvert$	$2V_{Tn}+\lvert V_{Tp}\rvert$
13A	V_{dd}-$2V_{Tn}$	$\lvert V_{Tp}\rvert$	V_{dd}-$2V_{Tn}$	$\lvert V_{Tp}\rvert$	$2V_{Tn}+\lvert V_{Tp}\rvert$
CLRCL	V_{dd}-V_{Tn}/V_{dd}	$\lvert V_{Tp}\rvert$/*Gnd*	V_{dd}-V_{Tn}	$\lvert V_{Tp}\rvert$	$V_{Tn}+\lvert V_{Tp}\rvert$

TABLE IV
HSPICE DC ANALYSIS RESULTS OF DIFFERENT 10T FULL ADDER DESIGNS

Designs	$Cout\_high_{min}$	$Cout\_low_{max}$	Sum_high_{min}	Sum_low_{max}	$V_{dd,min}$
SERF	1.59	0.97	1.59	0	2.8
9A	1.58	0.98	1.58	0.96	2.8
9B	1.58	0.98	1.58	0.94	2.8
13A	1.59	0.98	1.59	0.96	2.8
CLRCL	2.36/3.3	0.97/0	2.21	0.98	1.9

TABLE V
$V_{dd,\min}$ VERSUS WORKING FREQUENCY FOR VARIOUS 10T FULL ADDER DESIGNS

$V_{dd,min}$	100MHz	125MHz	250MHz	500MHz	1GHz
SERF	2.8	2.8	2.9	3.1	3.3
9A	2.8	2.8	2.9	3.1	3.3
9B	2.8	2.8	2.8	3.1	3.3
13A	2.8	2.8	2.8	3.1	3.3
CLRCL	2.0	2.1	2.2	2.5	2.9

The worst case output voltage levels are recorded. The numbers (all measured in volts) are in accord with the theoretical analysis results shown in Table III. To measure the minimum V_{dd} in

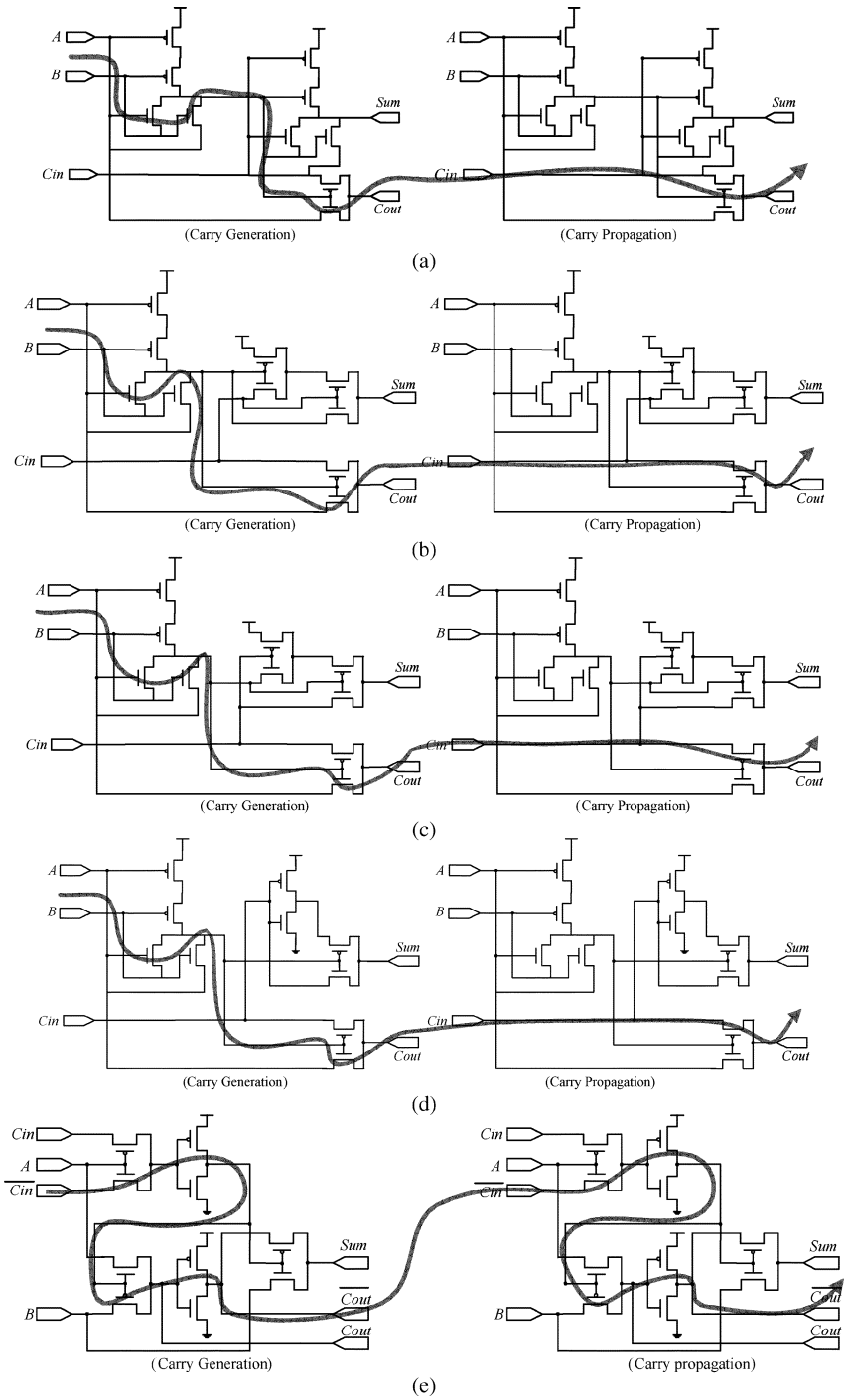

Fig. 7. Critical path analysis of different 10T based ripple adder designs. (a) SERF. (b) 9A. (c) 9B. (d) 13A. (e) CLRCL.

which the circuits can still function properly, every output of the full adder designs is loaded with a typical size inverter, where $(W/L)_{\rm p} = 1.4\ \mu$m$/0.35\ \mu$m and $(W/L)_{\rm n} = 0.7\ \mu$m$/0.35\ \mu$m. A full adder design is considered working properly subject to a power supply if its output voltage swing is larger than the range confined by the V_{IH} and the V_{IL} of the loading inverter. As we can see from Table IV, the proposed CLRCL design has the lowest $V_{dd,\min}$ among all 10-transistor full adder designs.

In other words, the proposed design can endure extremely low power supply operations to save power consumption. Note that $V_{dd,\min}$ numbers in Table IV are obtained under the steady state condition. $V_{dd,\min}$ increases with the working frequency as shorter time period is allowed for higher frequency operations. Table V summarizes the $V_{dd,\min}$ values at different working frequencies. Again, the proposed CLRCL design has the lowest $V_{dd,\min}$ value among all 10T designs at different working frequencies. It should be noted that the numbers in Table V are only for a single full adder. If multiple adders are cascaded, the speed performance will be further degraded and even higher $V_{dd,\min}$ is needed to boost the operation speed.

TABLE VI
SPEED ANALYSES OF DIFFERENT RIPPLE ADDER DESIGNS

	Word length	2-bit	4-bit	8-bit	16-bit
category	designs	Delay (ns)	Delay (ns)	Delay (ns)	Delay (ns)
10T	CLRCL	1.57/1.89	3.44/3.73	7.15/7.43	14.48/14.86
	9A	2.99*	9.03*	22.54*	77.3*
	9B	3.52	10.04	30.8	106
	13A	3.53	8.78	24.9	77
	SERF	2.93	7.99	22.45	70.8
Higher gate count	14T	0.775	1.43	3.66	11.51
	16T	0.608	1.26	3.1	9.7
	TFA	0.547	1.13	2.845	8.386
	TG-CMOS	0.502	1.082	3.05	10.21
	28T	0.793	1.411	2.66	5.097

* measurement for $C\mathrm{out}$ only, Sum signal is void

C. Simulation Results of Ripple Adder Designs

After static analyses of various single-bit adder designs, we examine their dynamic performances. Since the speed performance of PTL based designs tends to degrade drastically with the depth of logic chaining, the simulations will be based on ripple carry adder designs. The results can thus faithfully reflect the design performance in real practice. The simulations will be conducted subject to different adder sizes ranging from 2, 4, 8, to 16 bits. The performance indexes include worst case delay (maximum working frequency) and average energy consumption per addition. Note that the average energy consumption per addition is equivalent to the power delay product or normalized power consumption per megahertz. To evaluate the worst case delays, we need to first identify the critical path of each design and then derive the required input patterns for signals to propagate along the critical path. For a ripple carry adder, the most critical timing lies in the path of carry propagation from the least significant bit (LSB) to the most significant bit (MSB). Therefore, a carry must be generated in the LSB position and propagated all the way to the MSB position. Among various input patterns leading to carry generation or propagation in each bit of full adder, only the one that results in the longest delay (usually degraded outputs) will be selected. Because the pattern selected depends on the structure of the full adder, different input patterns must be applied to different designs. Fig. 7 illustrates the critical paths of different full adder designs. For simplicity, only 2-bit cascade is shown.

Since many 10T full adder designs fail to function properly at low V_{dd} operations, we use $V_{dd} = 3.3$ V in our worst case delay simulations. The rise time and the fall time are set to be 0.01 ns. The delay (in nanoseconds) is the period between the applying of input pattern and the availability of $C\mathrm{out}$ at MSB. The simulations are conducted for different adder sizes, ranging from 2-bit to 16-bit. The results are summarized in Table VI. Since the proposed CLRCL design has complementary carry signals, two delay numbers are given. The maximum working frequency ($f_{\max}$ in megahertz) is the reciprocal of the larger delay. Among the ten designs under comparison, CLRCL, 9A, 9B, 13A, and SERF are 10T designs. The remaining 5 designs, i.e., 14T, 16T, TFA, TG-CMOS and 28T, are higher gate count designs with full voltage swing operations. They are considered to have better speed performance, when compared with 10T designs, at the cost of increased circuit complexity. From the table,

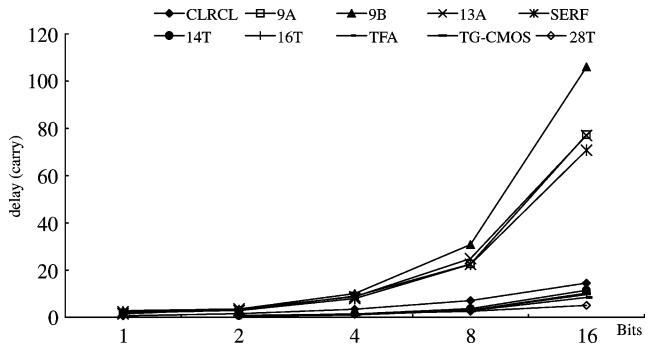

Fig. 8. Worst case delays of different ripple adder designs.

it is clear that the proposed CLRCL design has the minimum delays among all 10T designs. And the delay gap between our design and the other designs becomes even wider as the size of ripple adder grows. When the word length is equal to 16 bit, the delay of the CLRCL design is almost a magnitude order smaller than that of the other 10T designs. As for those higher gate count designs, the delays tend to decrease with the increase of transistor count in full adder design (with exception of TG-CMOS). The speed discrepancy becomes even more evident in the case of large word length. This seems reasonable because extra transistors can be used to enhance the driving capability. Compared with those higher gate count designs, the proposed CLRCL design is inferior in speed but the delay remains in the same magnitude order. This is mainly attributed to the inverter buffering strategy of the design. The worst case delays in Table VI can be better visualized by the delay plot in Fig. 8. The delays of all 10T designs, except that of CLRCL, tend to increase dramatically with the adder size. This is due to the inadequate signal driving strength along the carry propagation chain. Note that in 9A design, despite correct carry propagation, the Sum output fails because of triple threshold voltage drops on $\mathrm{Sum\_high}$ signal. It is thus not suitable for cascaded operation (unless a higher V_{dd} is employed).

We next examine the power/energy consumption issues of these designs. The index term (Φ) we use is the average energy consumption per addition (or per input transition). It is defined as the product of average power and the clock period under the condition of working at $f_{\max}$. The equation is given in (7). Since

TABLE VII
POWER CONSUMPTION AT $f_{\max}$ ANALYSIS FOR DIFFERENT ADDER DESIGNS

Word length	2-bit		4-bit		8-bit		16-bit	
designs	power	f_{max}	power	f_{max}	power	f_{max}	power	f_{max}
CLRCL	0.398	490	0.551	257	0.783	132	1.170	67
9A	0.181	334	0.358	110	0.783	44	1.624	13
9B	0.110	95	0.315	49	0.776	19	1.740	6.1
13A	0.219	263	0.489	105	1.082	37	2.322	11
SERF	0.187	341	0.370	125	0.785	44	1.616	14
14T	0.596	1290	0.667	699	0.812	273	1.317	87
16T	0.768	1644	0.789	794	0.977	322	1.547	103
TFA	0.839	1828	1.002	885	1.026	351	1.632	119
TG-CMOS	1.170	1992	1.210	924	1.190	328	1.578	98
28T	1.013	1193	1.186	685	1.291	369	1.368	195

the power delay product is equal to the energy, the index actually corresponds to the energy consumption per addition.

$$\Phi = P_{\text{av}} \cdot T_{\min}|_{V_{dd}} = (P_{\text{av}}/f_{\max})|_{V_{dd}}. \tag{7}$$

From (7), Φ is also equal to the average power consumption normalized by the frequency. This index serves as a better term to compare the power behaviors of two designs working at different frequencies. The test patterns are classified into two groups. In group 1, test patterns leading to a propagation of signal "1" from LSB to MSB and those patterns leading to a propagation of signal "0" from LSB to MSB are applied in an interleaving manner. Various test patterns are further generated by arbitrarily interchanging the two inputs A, B in each bit position. This group of test patterns represents scenarios of worse power consumption. In group 2, random test patterns are used and a total of 58 test patterns are included. The figure of power consumption is then calculated by averaging the numbers obtained in the two test pattern groups. The V_{dd} value is set to 3.3 V in our simulations. The power consumptions at $f_{\max}$ of these designs are compiled into Table VII. The unit of the power consumption is milliwatts. The frequencies ($f_{\max}$ in megahertz) of applying test patterns are also indicated in the table. From the data in Table VII, the energy consumption behaviors of these adder designs are illustrated in Figs. 9 and 10. Fig. 9 shows the Φ index comparison of the five 10T designs. The proposed CLRCL design has the smallest figures in all adder word lengths and the performance edges over the other designs become larger and larger with the increase of word length. This is mainly because the other 10T based designs, lacking proper driving capabilities in cascaded operations, take much longer time to accomplish the computation. The energy consumption, i.e., the power delay product, thus deteriorates accordingly. Note that designs 9A and SERF have almost identical energy consumption behavior. Design 9B has the worst energy performance in that it suffers from the slowest operation. To compare the energy performances of those designs with different gate counts, a new performance index Ψ called area weighted energy consumption is devised. It is defined as the product of area, power and delay.

$$\Psi = A \cdot P_{\text{av}} \cdot T_{\min}|_{V_{dd}} \tag{8}$$

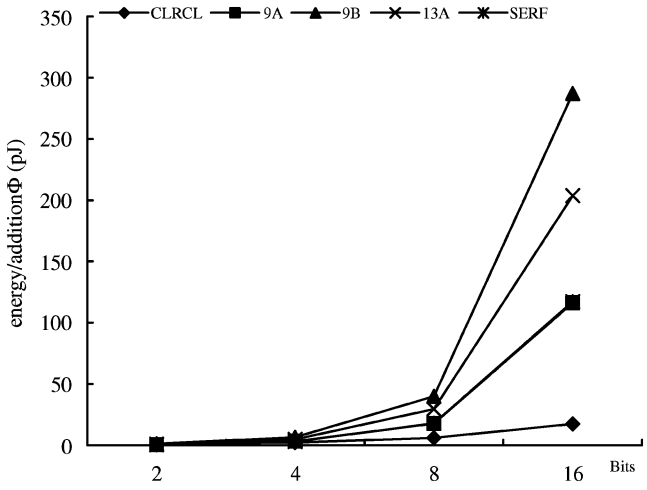

Fig. 9. Comparison of energy consumption per addition (Φ) for different 10T based designs.

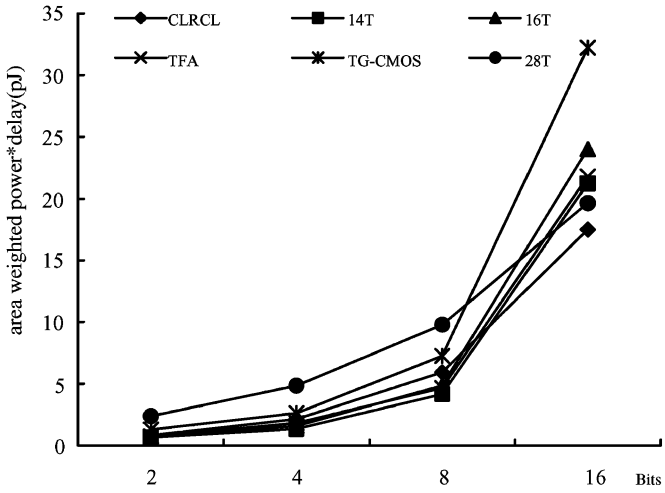

Fig. 10. Comparison of area weighted energy consumption per addition (Ψ) for CLRCL versus high-gate-count full adder designs.

In Fig. 10, we show the comparison results of the proposed CLRCL design versus the other high-gate-count designs mea-

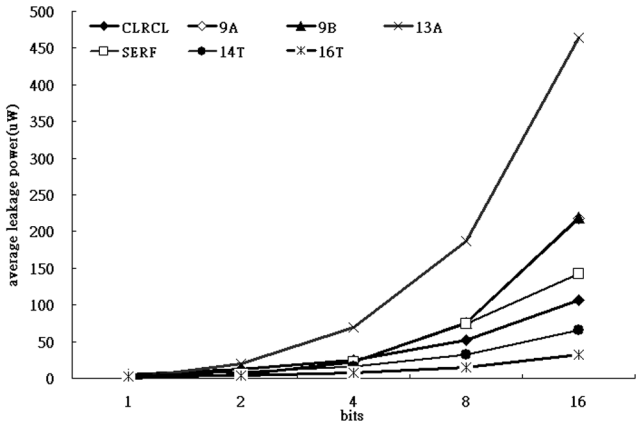

Fig. 11. DC power consumptions of various adder designs.

sured in Ψ. When the word length is less than 8-bit, the Ψ values among different designs (except the 28T design) do not vary much. However, when the word length reaches 16-bit, the Ψ values of 14T, 16T, TFA and TG-CMOS designs start to soar. On the other hand, the CLRCL and the 28T designs exhibit only mild increase in Ψ values. Meanwhile, the CLRCL design enjoys the lowest Ψ value among all the 16-bit designs. This, again, demonstrates the superiority of the proposed design.

Besides the dynamic power consumption behavior, we also examine the dc or leakage power consumption behavior of these adder schemes. For the proposed CLRCL design, since two inverters are employed to combat the threshold voltage loss problem, dc power consumption will occur if degraded inputs (outputs of MUX1 or 2) are applied to the inverters. Fortunately, in our design, not all adder input combinations lead to the presence of degraded signals at these inverters and the amount of degradation is confined to one V_T at most. These factors will limit the scale of dc power consumption caused by the inverters due to simultaneous conduction of P and N logic networks. Since inverters are also employed in designs 14T and 13A, they thus encounter a similar dc power consumption problem. However, for these low-gate-count full adder designs, the major dc power consumption comes from not just the inverters but also any circuit connecting to V_{dd} and controlled by a degraded signal. If the control signal is degraded by more than one V_T, the device can conduct heavily and significant dc power consumption will be drawn. Among all the full adder designs addressed, high-gate-count designs 28T, TG-CMOS and TFA have full swing signals and the dc power consumptions are negligible. For the remaining designs, the average dc power dissipations (subject to random input patterns) for different adder word lengths are simulated. The results are shown in Fig. 11. The proposed CLRCL design has the least dc power consumption among all 10T designs. As mentioned, the inferior dc power consumption behaviors of the other 10T designs are mainly attributed to the severely degraded carry signals which serve as the input to the next stage in cascaded operations. Design 13A, in particular, has the worst dc power consumption in that the $2V_T$ degraded carry out signal is fed to the inverter of the Sum logic in the next stage.

Fig. 11 also shows that the dc power consumption improves with the increase of transistor count used in full adder designs. The 16T and 14T designs thus have better dc power consumption than all the 10T designs. This is reasonable because extra transistors help intact signal propagation. On the other hand, the proposed CLRCL design, using as few as ten transistors, has successfully controlled the adverse dc power consumption to a satisfactory level. If we compare the dc power consumption of the CLRCL design with the total power consumption at $f_{\max}$, the percentage is only 9% for word length up to 16 bit. Note that the dc power consumption of the proposed design can be further reduced if the adder is in a standby mode. In this case, a specific input pattern, i.e., $A = 00\ldots0$, $B = 11\ldots1$ and $\mathrm{C}_0 = 1$, can be applied so that internal signals have full voltage swing. The dc power dissipation caused by the inverters can thus be eliminated and the total dc power consumption in standby mode will become negligible as the case in static CMOS logic.

IV. Conclusion

In conclusion, in this paper, we have presented a novel full adder design using as few as ten transistors per bit. The design adopts inverter buffered XOR/XNOR designs to alleviate the threshold voltage loss problem and to enhance the driving capability for cascaded operations. It successfully embeds the buffering circuit in the full adder design, so the transistor count is minimized. Enhanced driving capability also facilitates lower voltage or faster operations, which lead to less energy consumption. Extensive simulations are conducted to evaluate the performance of the proposed design against the other designs. In the dc aspect, the CLRCL design requires the lowest power supply among all 10T designs. In theaspect, under a fixed V_{dd}, the CLRCL design also enjoys the highest working frequency. What is notable is that this performance edge grows with the word length of the ripple adder. We also include other higher gate count full adder designs in our comparison. In spite of the threshold voltage loss problem common in 10T full adder designs, the CLRCL design can still achieve competitive speed performance while using much smaller gate count. In terms of energy efficiency, the CLRCL design features the lowest energy consumption per addition among all 10T designs. Its area weighted energy consumption index is also superior to that of higher gate count designs when word length equals to 16-bit. As for the dc power consumption problem, the level restoring strategy of the CLRCL design can successfully reduce the dc power dissipation caused by input signal degradation and thus performs better than the other 10T designs. If a specific input pattern is applied, the standby power dissipation can be further minimized to leakage components only.

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