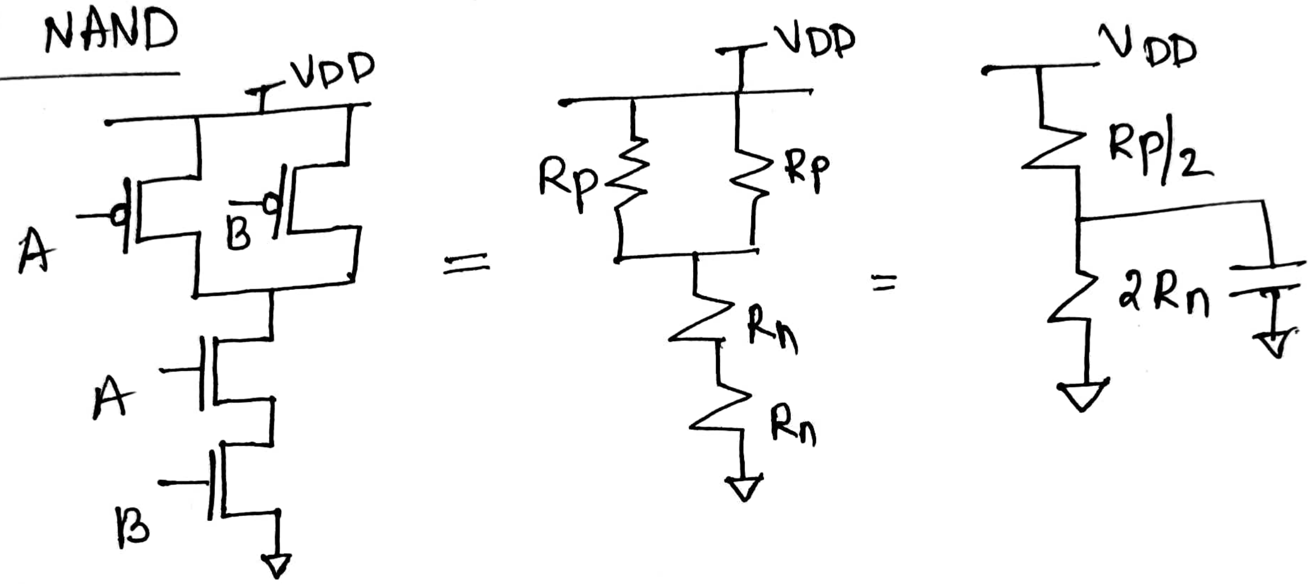
① Threshold voltage for CMOS inverter is

$$V_M = \frac{V_{DD} - |V_{tp}| + V_{tn}\sqrt{\frac{\beta_n}{\beta_p}}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

2-i/p NAND



$\boxed{R_p \propto \frac{1}{\beta_p}}$ & $\boxed{R_n \propto \frac{1}{\beta_n}}$

∴ Threshold voltage for 2-i/p NAND gate is

$$V_M = \frac{V_{DD} - |V_{tp}| + V_{tn}\sqrt{\frac{\beta_n/2}{2\beta_p}}}{1 + \sqrt{\frac{\beta_n/2}{2\beta_p}}}$$

$$\Rightarrow V_M = \frac{V_{DD} - |V_{tp}| + \frac{1}{2}V_{tn}\sqrt{\frac{\beta_n}{\beta_p}}}{1 + \frac{1}{2}\sqrt{\frac{\beta_n}{\beta_p}}}$$

For N-input NAND gate

$$\boxed{V_M = \frac{V_{DD} - |V_{tp}| + \frac{V_{tn}}{N}\sqrt{\frac{\beta_n}{\beta_p}}}{1 + \frac{1}{N}\sqrt{\frac{\beta_n}{\beta_p}}}}$$

we knowthat, $N \cdot M_L = V_{IL} - V_{OL}$, $\boxed{V_{OH} = V_{dd}}$

$N \cdot M_H = V_{OH} - V_{IH}$ $\boxed{V_{OL} = 0}$

For CMOS inverter:

$$V_{IH} = \frac{2V_{out} + V_{tn} + \frac{\beta_p}{\beta_n}(V_{DD} - |V_{tp}|)}{1 + \frac{\beta_p}{\beta_n}}$$

For 2-i/p NAND gate

$$\boxed{V_{IH_N} = \frac{2V_{out} + V_{tn} + 4\frac{\beta_p}{\beta_n}(V_{DD} - |V_{tp}|)}{1 + 4\frac{\beta_p}{\beta_n}}}$$

$\because R_p \rightarrow R_p/2$

$R_n \rightarrow 2R_n$

For CMOS inverter

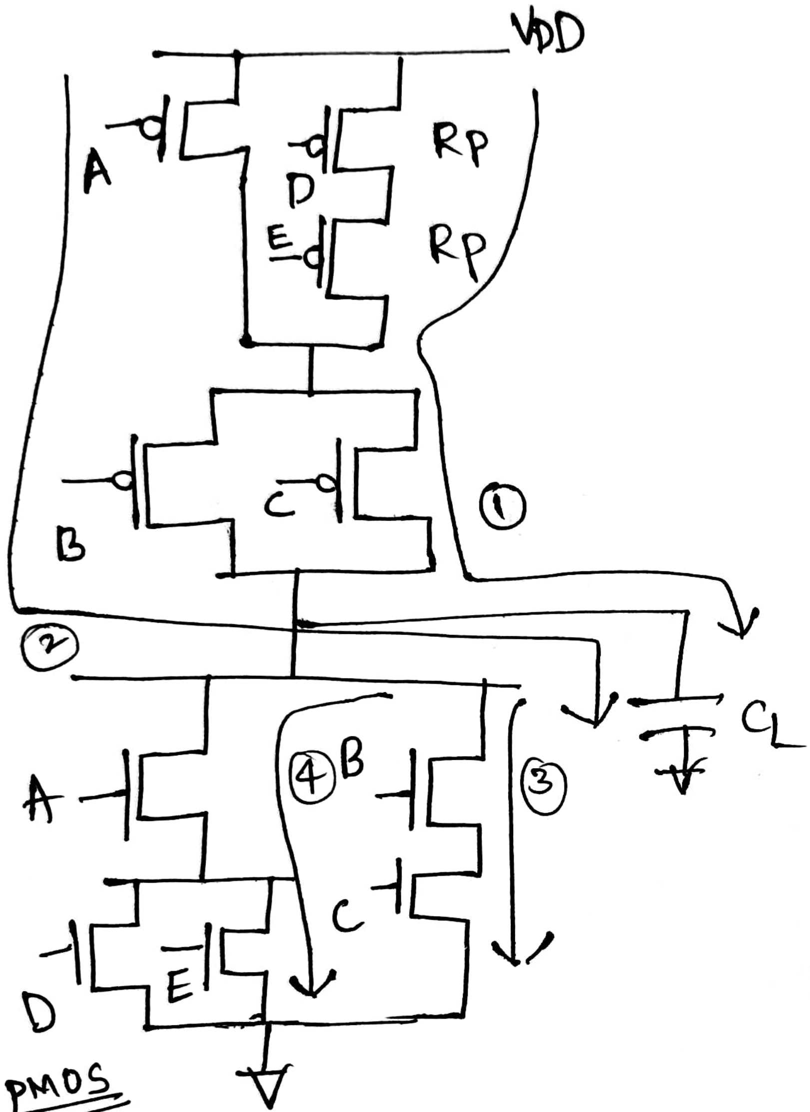
$$V_{IL} = \frac{2V_{out} - V_{DD} - |V_{Tp}| + \frac{\beta_n}{\beta_p}V_{tn}}{1 + \frac{\beta_n}{\beta_p}}$$

For 2-i/p NAND gate

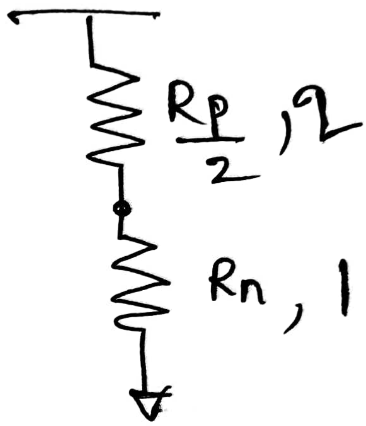
$$\boxed{V_{ILN} = \frac{2V_{out} - V_{DD} - |V_{Tp}| + \frac{1}{4}\beta_n/\beta_p}{1 + \frac{1}{4}\frac{\beta_n}{\beta_p}}}$$

(2) Given $F = \overline{A(D+E)+BC}$

CMOS implementation is



stand CMOS



PMOS

(1) $\Rightarrow R_p + R_p + R_p \rightarrow \frac{R_p}{2} \Rightarrow 3R_p \rightarrow \frac{R_p}{2} \Rightarrow W = 6 \Rightarrow W_D = W_E = W_B = W_C = 6$

(2) $\Rightarrow x + \frac{R_p}{6} = \frac{R_p}{2} \Rightarrow x = \frac{R_p}{3} \Rightarrow W_A = 3$

NMOS

(3) $\Rightarrow R_n + R_n \rightarrow R_n \Rightarrow 2R_n \rightarrow R_n \Rightarrow W = 2 \Rightarrow W_B = W_C = 2$

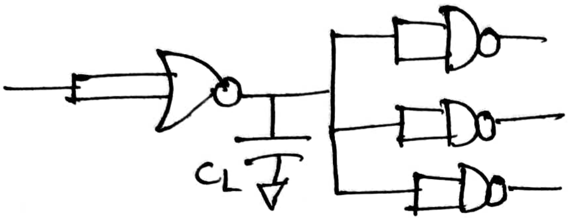
(4) $\Rightarrow R_n + R_n \rightarrow R_n \Rightarrow 2R_n \rightarrow R_n \Rightarrow W = 2 \Rightarrow W_A = W_E = 2$

$\Rightarrow W_D = 2$

③ Given $V_{DD} = 2V$, $C_{ox} = \frac{2fF}{\mu m^2}$, $C_{DBp} = 1fF$, $C_{DBn} = 0.5fF$

$\left(\frac{W}{L}\right)_p = \frac{4}{0.5}$, $k_p' = 100 \frac{\mu A}{V^2}$ $|V_{tp}| = 0.5V$

$\left(\frac{W}{L}\right)_n = 2/0.5$, $k_n' = 250 \frac{\mu A}{V^2}$, $V_{tn} = 0.6V$



a) $C_p = C_{DBp} + C_{DBn}$

$C_p = 1fF + 0.5fF \Rightarrow C_p = 1.5fF$

b) $C_{LC} = C_{g_1} + C_{g_2} + C_{g_3} = 3C_{ox} = \frac{6fF}{\mu m^2}$

c) $C_L = C_p + C_{CLC} = 1.5fF + \frac{6fF}{\mu m^2} = 7.5fF$

$R_p' = 2R_p$

d) $2R_p = \frac{2}{k_p' \left(\frac{W}{L}\right)_p (V_{DD} - |V_{tp}|)} = \frac{2}{100 \times 10^{-6} \times 8\,(2-0.5)} = 2\times 0.833 k\Omega$

e) $\tau = C_L R_p' = 7.5 \times 10^{-15} \times 0.833 \times 10^3 \times 2 = 6.24\,ps \times 2 = 12.48\,ps$

④ Given $\beta_n = 0.2 \frac{mA}{V^2}$, $\beta_p = 0.1 \frac{mA}{V^2}$ $V_{tn} = |V_{tp}| = 0.6$

$V_{DD} = 3.3V$

a) $V_M = \frac{V_{DD} - |V_{tp}| + V_{tn}\sqrt{\frac{\beta_n}{\beta_p}}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}} = \frac{3.3 - 0.6 + 0.6\sqrt{\frac{0.2}{0.1}}}{1 + \sqrt{\frac{0.2}{0.1}}}$

$\Rightarrow V_M \simeq \frac{3.548}{2.4142} \Rightarrow \boxed{V_M \simeq 1.45V}$

b) $R_p = \dfrac{1}{\beta_p(V_{DD} - |V_{tp}|)} = \dfrac{1}{0.1\times10^{-3}(3.3-0.6)} = 3.703\,k\Omega$

$R_n = \dfrac{1}{\beta_n(V_{DD} - V_{tn})} = \dfrac{1}{0.2\times10^{-3}(3.3-0.6)} = 1.851\,k\Omega$

c) $t_r = 2.2\,R_p C_p = 2.2\times3.703\times10^{3}\times9\times10^{-15} = 73.319\,ps$

$t_f = 2.2\,R_n C_p = 2.2\times1.851\times10^{3}\times9\times10^{-15} = 36.649\,ps$

d) $t_r = 2.2\,R_p(C_p + C_L) = 2.2\times3.703\times10^{3}\times34\times10^{-15} = 276.984\,ps$

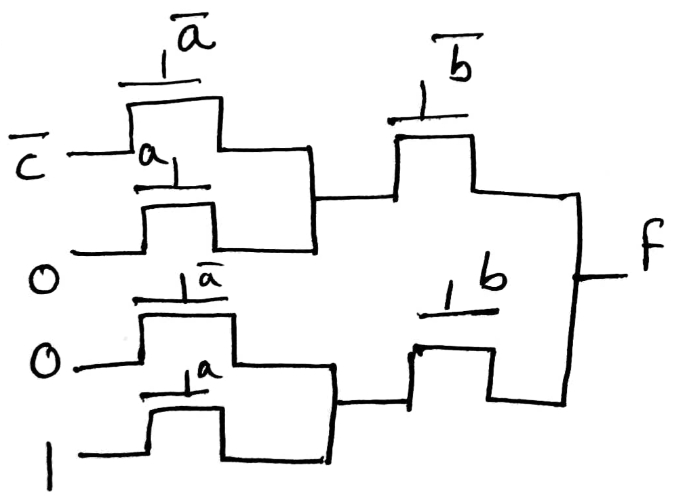
$t_f = 2.2\,R_n(C_p + C_L) = 2.2\times1.851\times34\times10^{-15} = 138.4548\,ps$

e) $t_{LH} = 0.693\,R_p(C_p + C_L) = 0.693\times3.703\times10^{3}(9+25)\times10^{-15}$
$= 87.179\,ps$

$t_{HL} = 0.693\,R_n(C_p + C_L) = 0.693\times1.851\times10^{3}(9+25)\times10^{-15}$
$= 43.589\,ps$

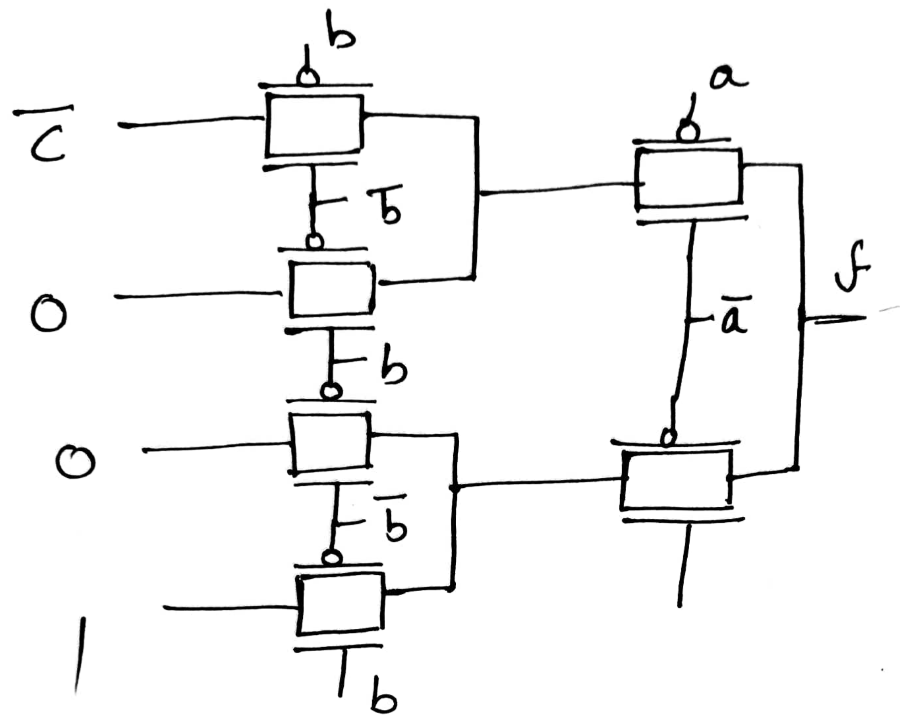
8) b)

$f(a,b,c) = ab + \bar{a}\bar{b}\bar{c}$

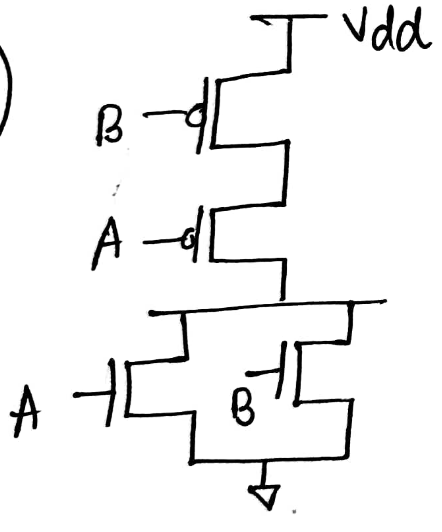


a	b	f
0	0	$\bar{c}$
0	1	0
1	0	0
1	1	1

a)



9)



case (i) A, B → long time zero & B → 0 to VDD

Then $R_{peq} = 2R_p$

$R_{neq} = R_n$

$\Rightarrow t_{LH} = 0.693(2R_p)c$ and

$t_{HL} = 0.693(R_n)c$ } → (1)

case (ii) A, B → long time zero & A, B → 0 to VDD

$\Rightarrow R_{peq} = 2R_p$ & $R_{neq} = \frac{R_n}{2}$

$t_{LH} = 0.693(2R_p)c$ } → (2)

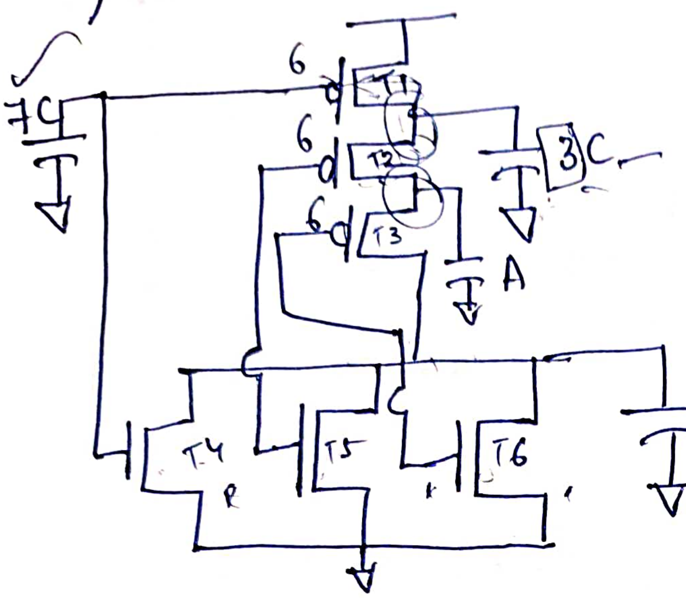
$t_{HL} = 0.693\left(\frac{R_n}{2}\right)c$

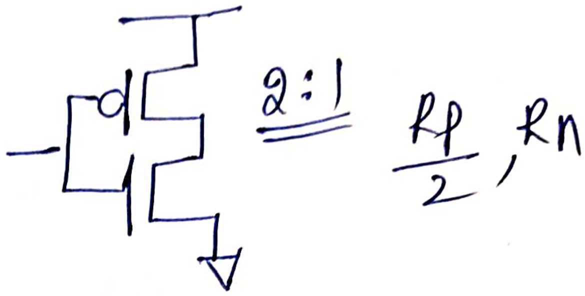
From (1) & (2)

$t_{pd_1} > t_{pd_2}$

∴ case (i) have more delay

10) Given circuit





Here $B = C_{d3} + C_{d4} + C_{d5} + C_{d6}$,, $A = 6C$

$= 6C + C + C + C$

$B = 9C$

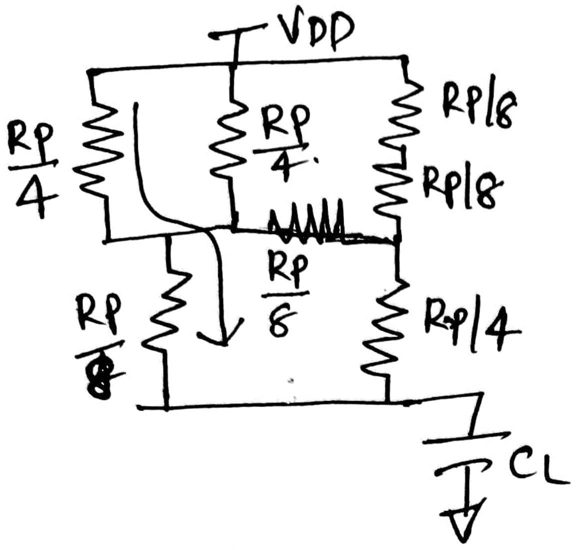
11) a) If $D = 0$ then $\overline{OUT} = ((AB)(E+F)) + CG$

If $D = 1$ then $\overline{OUT} = (AB + C) \cdot (E + F + G)$

Final Expression is

$$OUT = \overline{\bar{D}\left[(AB) \cdot (E+F) + CG\right] + D\left[(AB+C) \cdot (E+F+G)\right]}$$

11) b **Pull up Network** (equivalent circuit is)



input pattern, initially $E=F=G=D=0$, $A=B=C=1$ (This is one possibility)

Here the worst case resistance is

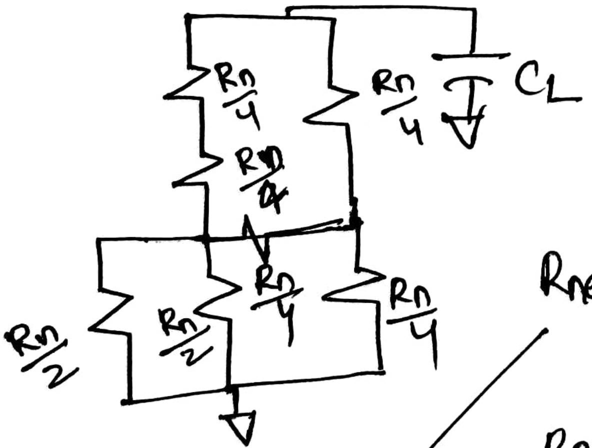
$$R_{Peq} = \frac{R_P}{8} + \frac{R_P}{8} + \frac{R_P}{8} + \frac{R_P}{4} = \frac{R_P + R_P + R_P + 2R_P}{8} = \frac{5R_P}{8}$$

or

$$R_{Peq} = \frac{R_P}{4} + \frac{R_P}{8} + \frac{R_P}{4} = \frac{2R_P + R_P + 2R_P}{8} = \frac{5R_P}{8}$$

Input pattern:

Pull down network (equivalent circuit)



Here the worst case resistance is

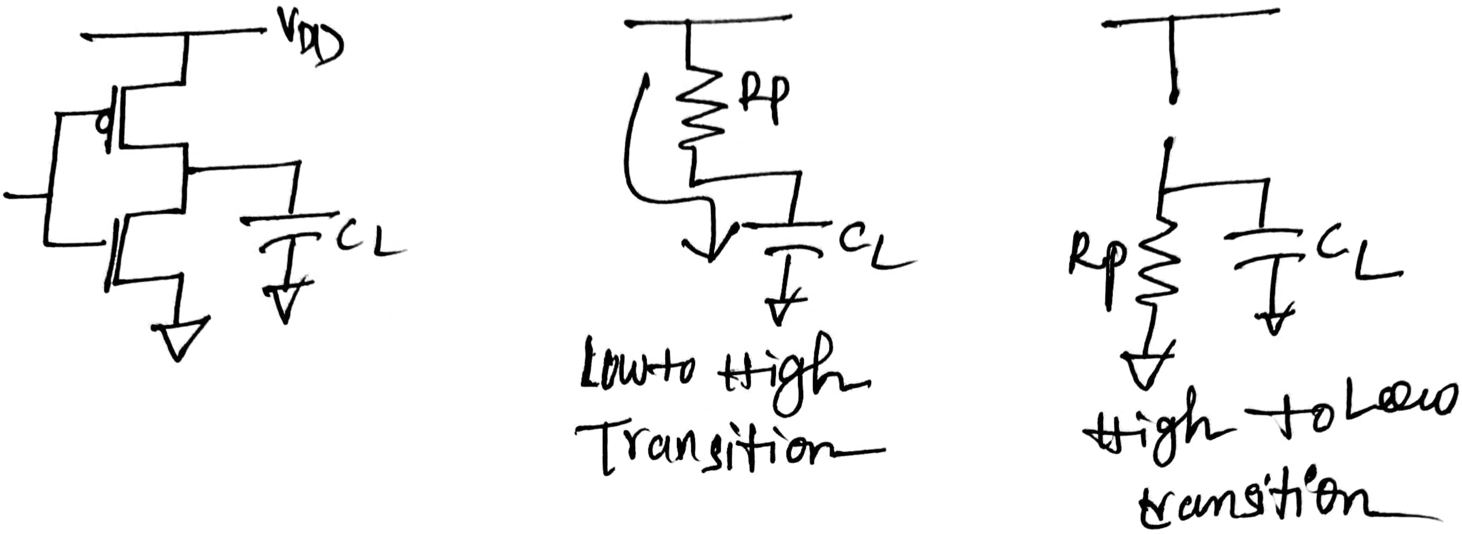
$$R_{neq} = \frac{R_n}{4} + \frac{R_n}{4} + \frac{R_n}{4} + \frac{R_n}{4} = R_n$$

or

$$R_{neq} = \frac{R_n}{4} + \frac{R_n}{4} + \frac{R_n}{2} = R_n$$

input pattern (Final) 1- $A=B=D=G=1$, $C=E=F=0$ (this is one possibility)

5) Dynamic power dissipation of CMOS inverter



During transition of the output from low to high, the energy drawn from the supply is given by

$$E_{0\to1} = \int_0^{Vdd} p(t)\,dt = \int_0^{Vdd} V_{dd}\, i(t)\,dt$$

$$= \int_0^{Vdd} V_{dd}\, C_L \frac{dV_o}{dt}\,dt$$

$$= V_{dd} C_L \int_0^{Vdd} dV_o$$

$$= V_{dd} C_L \times [V_{dd} - 0]$$

$$\boxed{E_{0\to1} = V_{dd}^2 C_L} \rightarrow (1)$$

The Energy stored in the capacitor is

$$E_C = \int_0^{Vdd} V_o \times C_L \frac{dV_o}{dt}\,dt$$

$$\Rightarrow \quad E_c = C_L \times \left.\frac{V_0^2}{2}\right]_0^{V_{dd}}$$

$$\Rightarrow \quad \boxed{E_c = \frac{C_L V_{dd}^2}{2}} \rightarrow (2)$$

From (1) & (2) I can say ~~that~~, out of total energy drawn from supply ($V_{dd}^2 C_L$), half of the energy stored in C_L and remaining half is dissipated in PMOS Network and remaining $\frac{1}{2} C_L V_{dd}^2$ (stored in C_L) is dissipated through NMOS Transistor

$$E_{dis} = \int_{V_{dd}}^{0} V_c(t)\, i(t)\, dt$$

$$= \int_{V_{dd}}^{0} V_c(t) \times -C_L \frac{d}{dt} V_c(t)\, dt$$

$$= -C_L \left.\frac{V_c^2}{2}\right]_{V_{dd}}^{0}$$

$$\boxed{E_{dis} = \frac{1}{2} C_L V_{DD}^2}$$

Now dynamic power dissipation

$$P_d = E_c \times t \Rightarrow P_d = \frac{1}{2} \frac{C_L V_{dd}^2}{T}$$

$$\Rightarrow P_d = \frac{1}{2} C_L V_{dd}^2 f$$

$$\Rightarrow \boxed{P_d = \frac{1}{2} \alpha_{0 \to 1} C_L V_{dd}^2 f}$$