भारतीय प्रौद्योगिकी संस्थान तिरुपति

TIRUPATI

Digital VLSI Design

Assignment 4

Submitted By:

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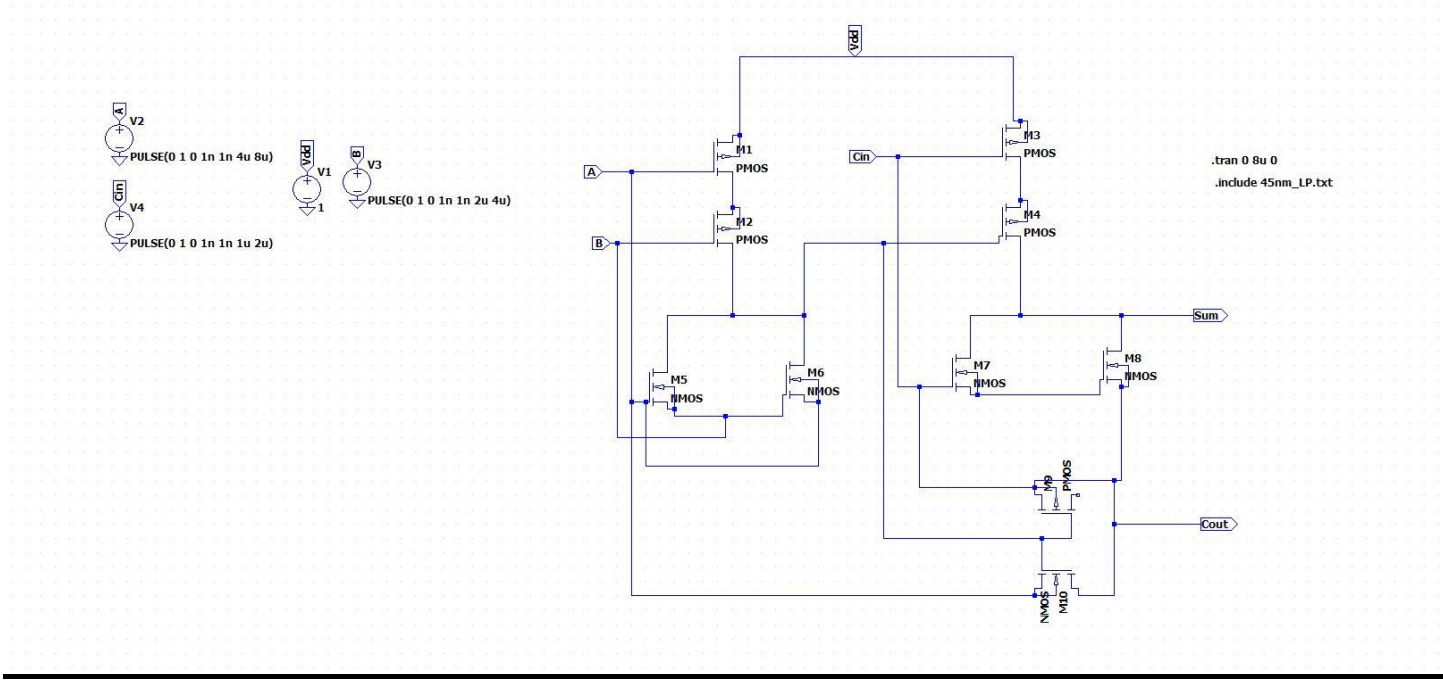
Submitted To:

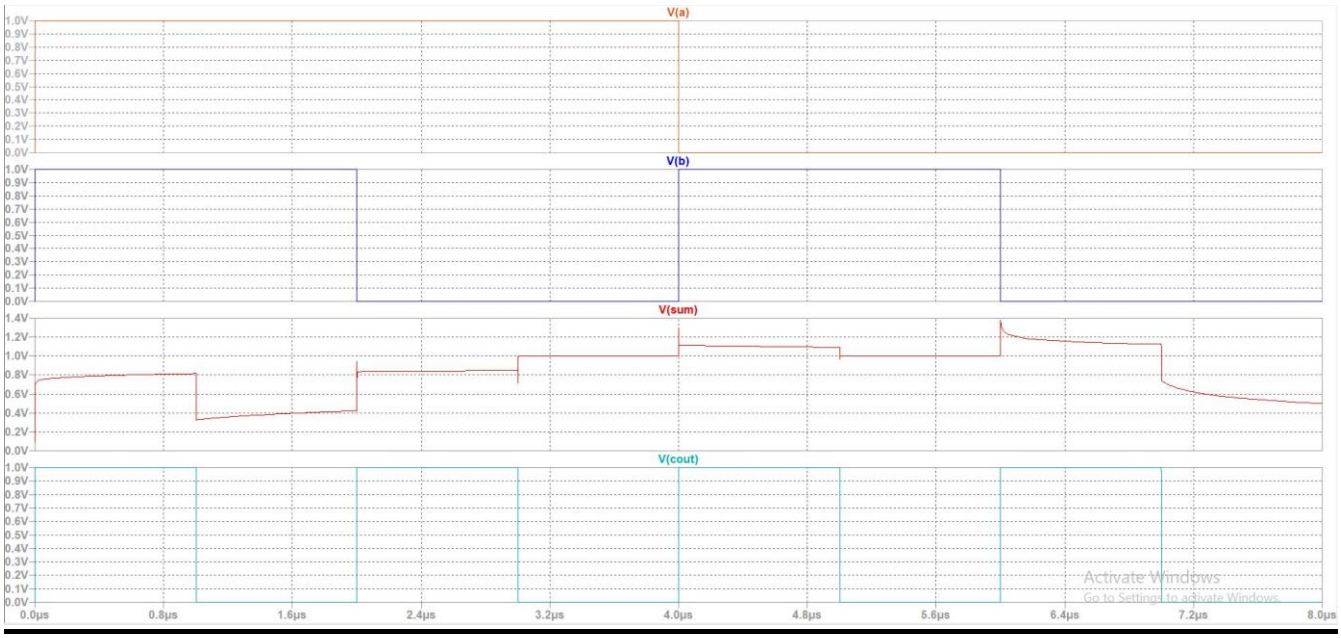
Dr. Vikram Pudi

Paper:-"A Novel High-Speed and Energy Efficient 10 Transistor Full Adder Design"

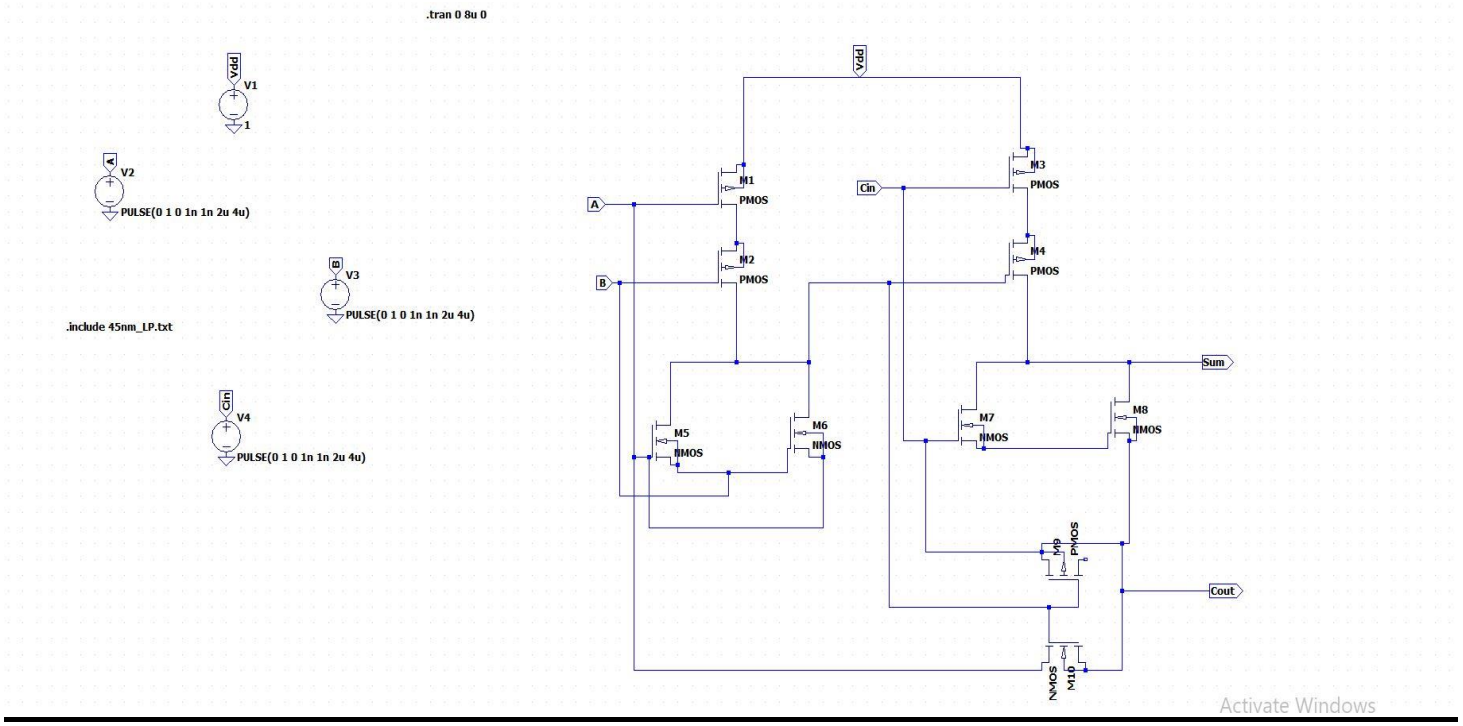
figure6

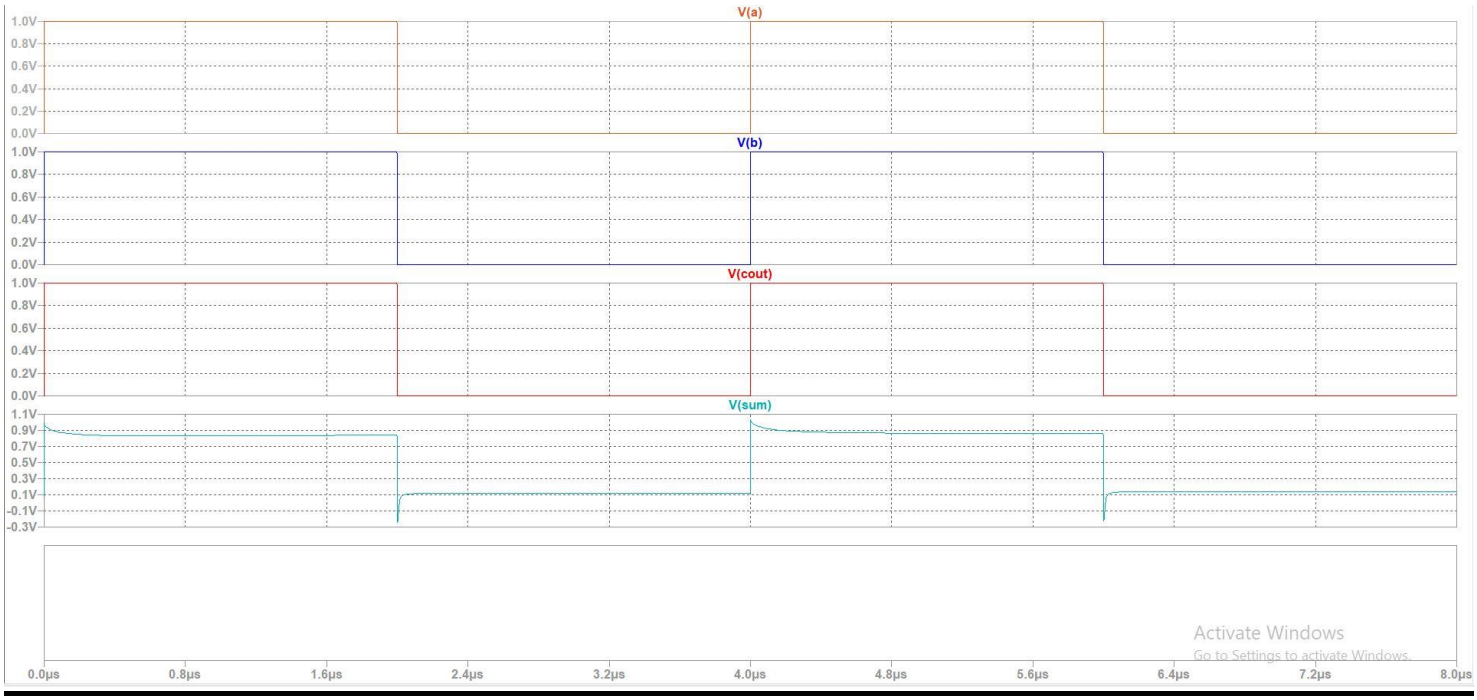
a)


A
V2
PULSE(0 1 0 1n 1n 4u 8u)
Cin
V4
PULSE(0 1 0 1n 1n 1u 2u)
Vdd
V1
1
B
V3
PULSE(0 1 0 1n 1n 2u 4u)
Vdd
M1
PMOS
M2
PMOS
M3
PMOS
M4
PMOS
M5
NMOS
M6
NMOS
M7
NMOS
M8
NMOS
Mp
PMOS
M10
NMOS
A
B
Cin
Sum
Cout
.tran 0 8u 0
.include 45nm_LP.txt

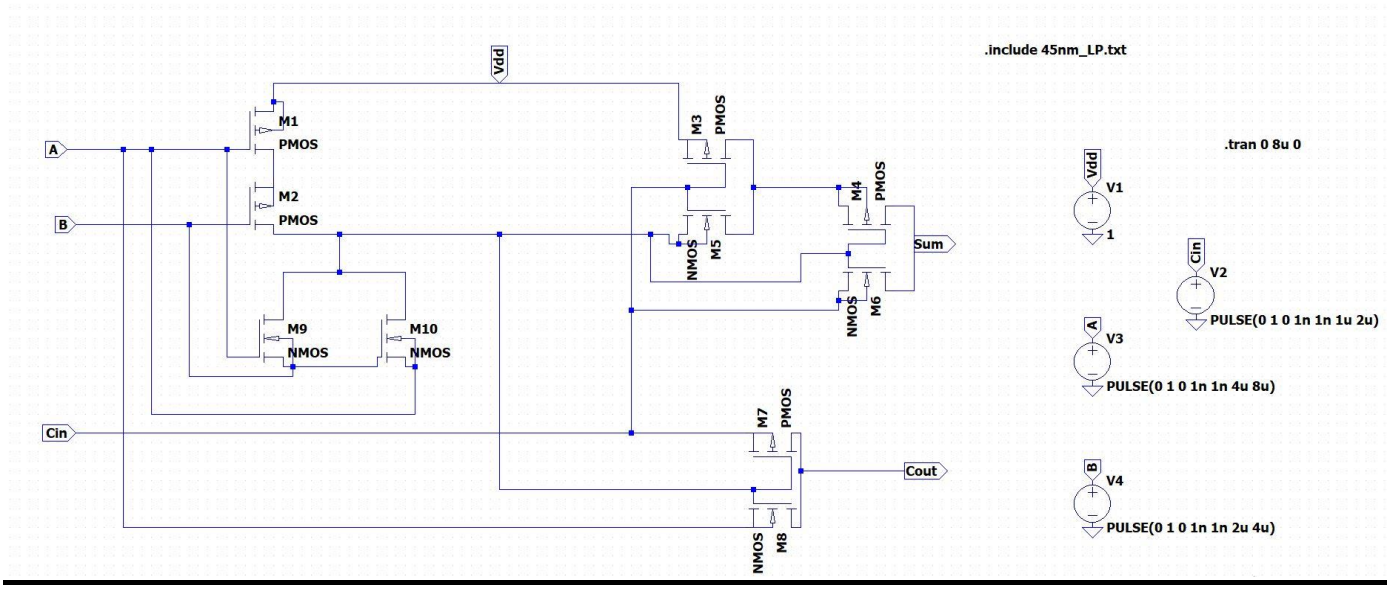

V(a)
1.0V
0.9V
0.8V
0.7V
0.6V
0.5V
0.4V
0.3V
0.2V
0.1V
0.0V
V(b)
1.0V
0.9V
0.8V
0.7V
0.6V
0.5V
0.4V
0.3V
0.2V
0.1V
0.0V
V(sum)
1.4V
1.2V
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
V(cout)
1.0V
0.9V
0.8V
0.7V
0.6V
0.5V
0.4V
0.3V
0.2V
0.1V
0.0V
0.0µs
0.8µs
1.6µs
2.4µs
3.2µs
4.0µs
4.8µs
5.6µs
6.4µs
7.2µs
8.0µs
Activate Windows
Go to Settings to activate Windows.

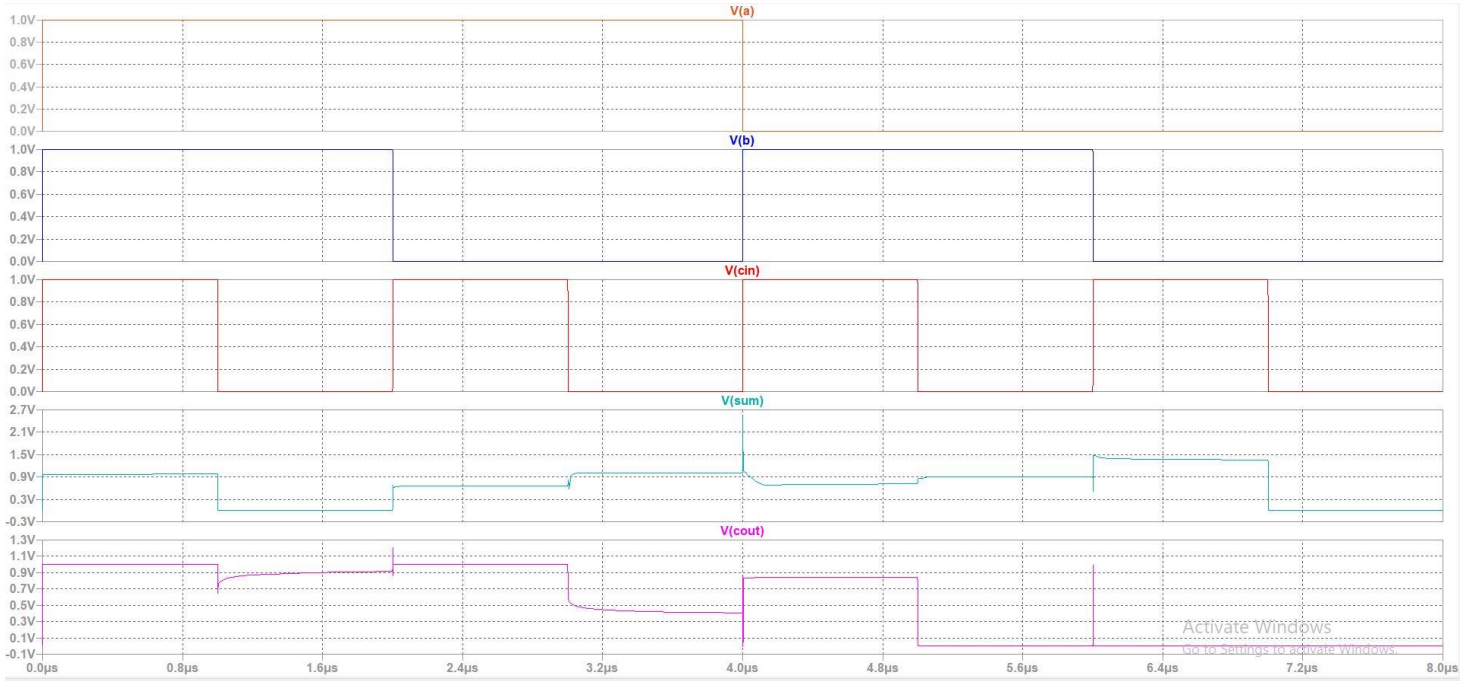
b)


.tran 0 8u 0
VDD
V1
1
A
V2
PULSE(0 1 0 1n 1n 2u 4u)
B
V3
PULSE(0 1 0 1n 1n 2u 4u)
.include 45nm_LP.txt
Cin
V4
PULSE(0 1 0 1n 1n 2u 4u)
M1
PMOS
M2
PMOS
M3
PMOS
M4
PMOS
M5
NMOS
M6
NMOS
M7
NMOS
M8
NMOS
Mp
PMOS
M10
NMOS
Sum
Cout
Activate Windows

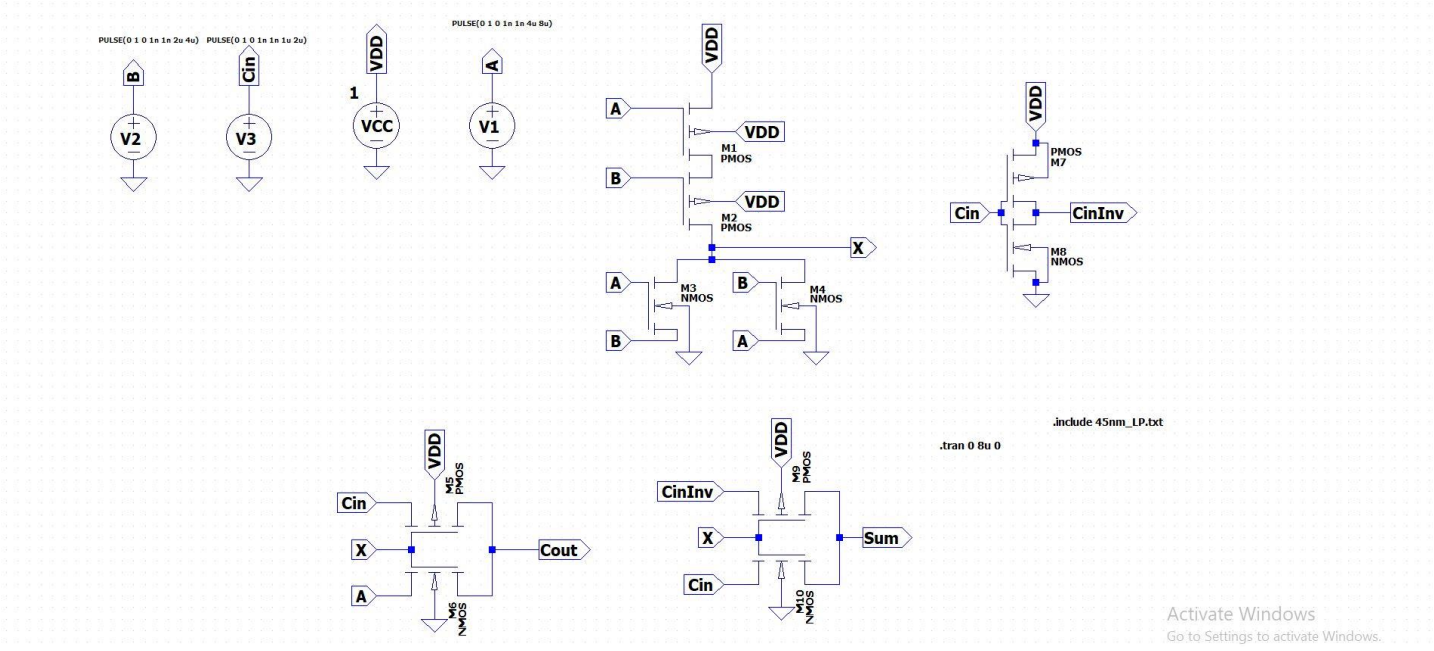

V(a)
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
V(b)
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
V(cout)
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
V(sum)
1.1V
0.9V
0.7V
0.5V
0.3V
0.1V
-0.1V
-0.3V
0.0µs
0.8µs
1.6µs
2.4µs
3.2µs
4.0µs
4.8µs
5.6µs
6.4µs
7.2µs
8.0µs
Activate Windows
Go to Settings to activate Windows.

c)


.include 45nm_LP.txt
.tran 0 8u 0
Vdd
A
B
Cin
Sum
Cout
M1
PMOS
M2
PMOS
M3
PMOS
M4
PMOS
M5
NMOS
M6
NMOS
M7
PMOS
M8
NMOS
M9
NMOS
M10
NMOS
V1
1
V2
PULSE(0 1 0 1n 1n 1u 2u)
V3
PULSE(0 1 0 1n 1n 4u 8u)
V4
PULSE(0 1 0 1n 1n 2u 4u)


V(a)
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
V(b)
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
V(cin)
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
V(sum)
2.7V
2.1V
1.5V
0.9V
0.3V
-0.3V
V(cout)
1.3V
1.1V
0.9V
0.7V
0.5V
0.3V
0.1V
-0.1V
0.0µs
0.8µs
1.6µs
2.4µs
3.2µs
4.0µs
4.8µs
5.6µs
6.4µs
7.2µs
8.0µs
Activate Windows
Go to Settings to activate Windows.

d)


PULSE(0 1 0 1n 1n 2u 4u)
B
V2
PULSE(0 1 0 1n 1n 1u 2u)
Cin
V3
VDD
1
VCC
PULSE(0 1 0 1n 1n 4u 8u)
A
V1
VDD
A
VDD
M1
PMOS
B
VDD
M2
PMOS
X
A
M3
NMOS
B
M4
NMOS
B
A
VDD
PMOS
M7
Cin
CinInv
M8
NMOS
VDD
M5
PMOS
Cin
X
Cout
A
M6
NMOS
.include 45nm_LP.txt
.tran 0 8u 0
VDD
M9
PMOS
CinInv
X
Sum
Cin
M10
NMOS
Activate Windows
Go to Settings to activate Windows.

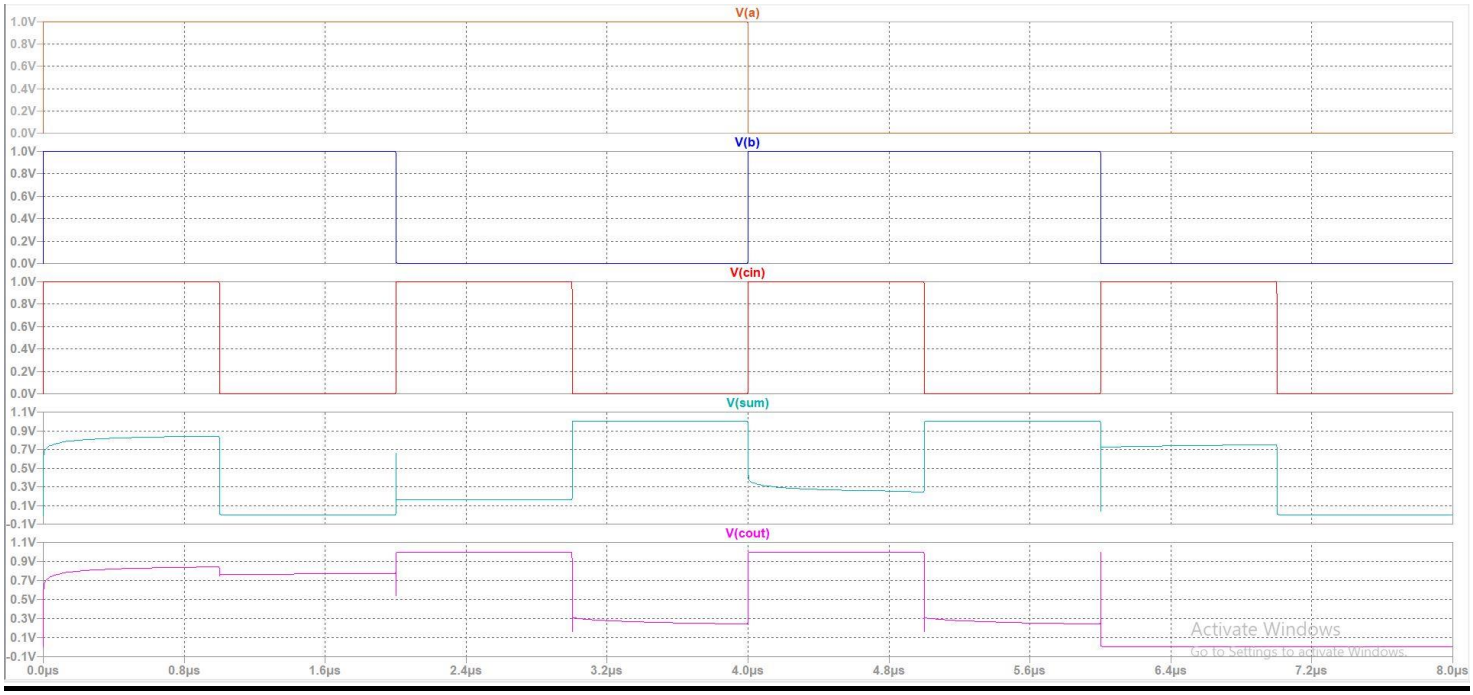
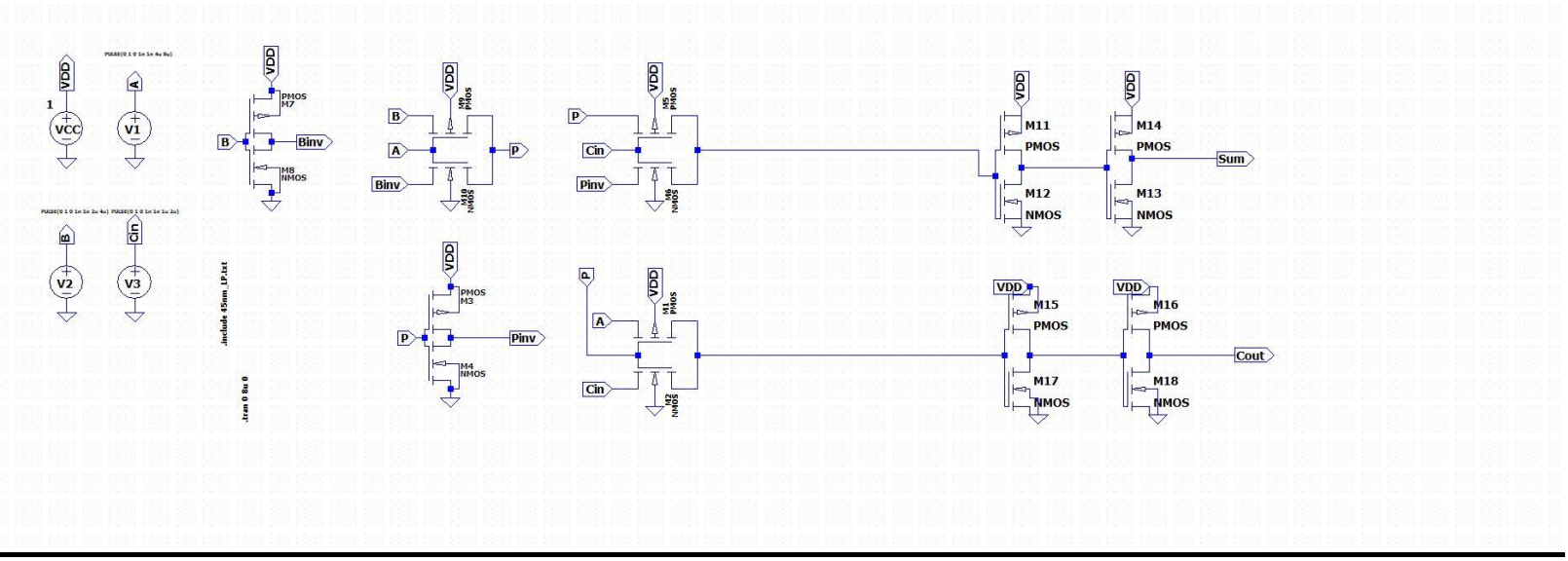
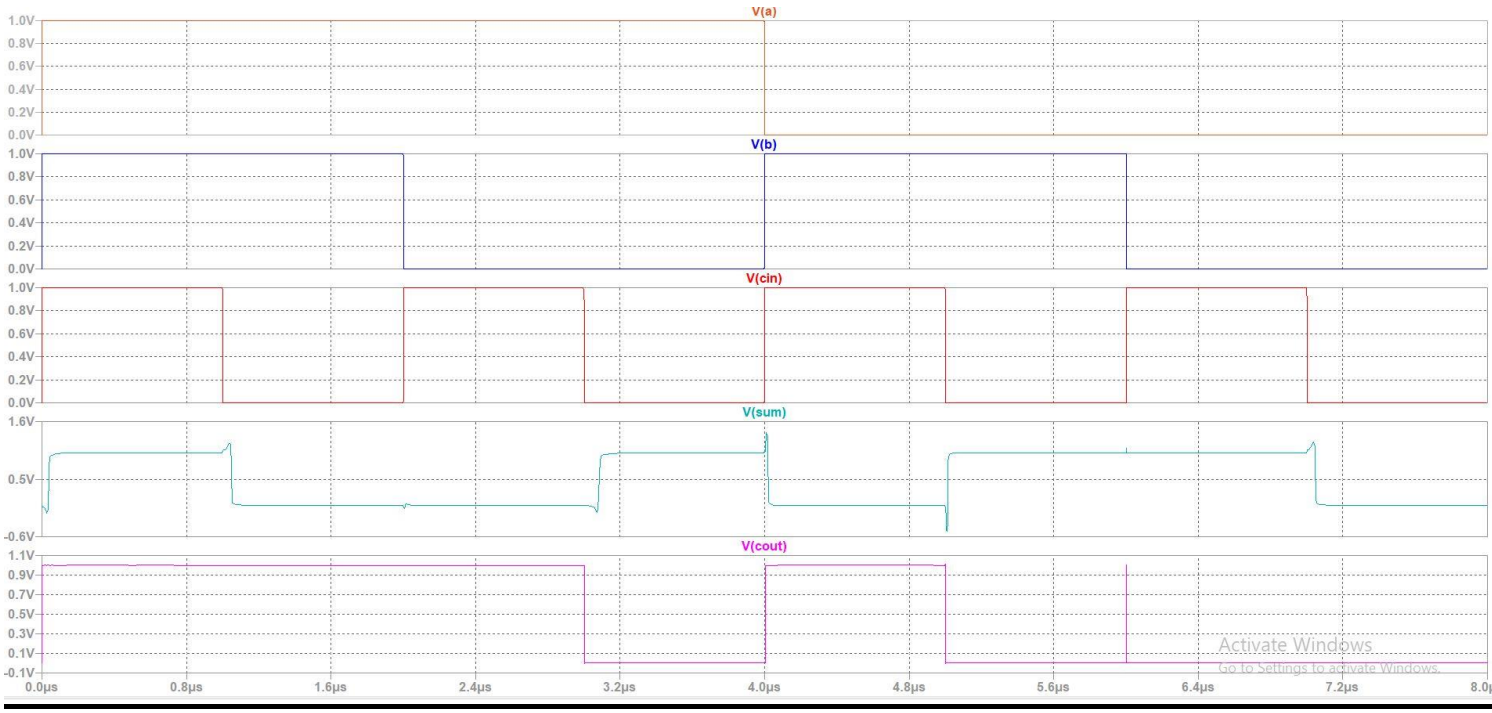

V(a)
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
V(b)
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
V(cin)
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
V(sum)
1.1V
0.9V
0.7V
0.5V
0.3V
0.1V
-0.1V
V(cout)
1.1V
0.9V
0.7V
0.5V
0.3V
0.1V
-0.1V
0.0µs
0.8µs
1.6µs
2.4µs
3.2µs
4.0µs
4.8µs
5.6µs
6.4µs
7.2µs
8.0µs
Activate Windows
Go to Settings to activate Windows.

fig4)


VDD
1
VCC
A
V1
B
V2
Cin
V3
.include 45nm_LP.txt
.tran 0 8u 0 .01r
PMOS
M7
M8
NMOS
Binv
M3
M4
Pinv
M5
M6
P
Cin
Pinv
M1
M2
M11
M12
M13
M14
Sum
M15
M16
M17
M18
Cout



The voltage swing is reduced by the threshold voltage due to the pass transistor configuration, and applying the input to the drain/source terminal of the MOSFET along with the gate terminal. Due to the leakage effect the swing reduction is reduced. The delay of the various full adder configuration shows negligible difference. The delay is approximately few psec for the sum circuit. The full addder in the Fig.4 outperforms the full

adders in the Fig.6 due to the inverter's drain/source terminal is connected to fixed supply and not the input producing full voltage swing. As well as all the circuit nodes are drived by both NMOS and PMOS without liming the voltage swing.