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Design of Low Area and Low Power Systolic Serial Parallel Multiplier using CNTFETs

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***Abstract*—In this paper, we designed a CNTFET based Systolic serial parallel multiplier. This systolic serial parallel multiplier is 100% efficient and operates on selection of either 0, X, 2X, 3X product terms, where X is a serial input to the multiplier. This multiplier design requires modules like 4×1 MUX, 2×1 MUX, OR gate, Full Adder, and Delay elements known as D-Flipflops. In this paper, we have used Gate Diffusion Input (GDI) technique for designing combinational logic gates to reduce the area and power. This multiplier design require more number of D-Flipflops compared to other logic circuits. In this paper we proposed a new D-Flipflop with 10 transistors with a single clock load and a 10T-based full adder design to reduce area and power consumption. The proposed systolic serial parallel multiplier has a saving of 41% of area compared to recent design. Our simulation results shows that proposed systolic serial parallel multiplier design has a reduction in transistor count by 82.65%, a drop in power dissipation by 95.96%, decrease in delay by 98.12% and a decrease in PDP by 99.92% compared to the existing systolic array multiplier.**

***Index Terms*—Carbon NanoTube, Carbon NanoTube Field Effect Transistor (CNTFET), serial parallel multiplier (SPM), systolic serial parallel multiplier (SSPM), Gate Diffusion Input (GDI) technique, flipflop.**

I. Introduction

For the past decade, various researches have been extensively carried out on Carbon NanoTube Field Effect Transistor [1]–[3] (CNTFET) to replace traditional CMOS in nano scale to overcome the scaling down limitations of CMOS circuits. CNTFETs have advantages like higher on-current and lower off-current than that of MOSFETs and also can be operated at low power supplies [4]. In digital devices like Microprocessors, Digital signal Processors etc, having multiplier architectures such as Array multiplier, Baugh-Wooley multiplier, Wallace tree multiplier, Dadda multiplier, Add shift multiplier, etc, to multiply the binary numbers involve complex logic design, high propagation delay, and high power dissipation. These problems increases with an increase in the size of data so that these multiplying architectures are not compatible with large numbers. Serial Parallel Multiplier (SPM) architecture [5] and Systolic Serial Parallel Multiplier (SSPM) [6] are potential alternate architectures to overcome the problems of power dissipation and propagation delay.

In this paper, We have used GDI-based logic gates to design SSPM to reduce power consumption and propagation delay. The SSPM multiplier designed in this paper has a decrease in transistor count by 82.65%, drop in power dissipation by 95.96% and decrease in delay by 98.12% compared to existing systolic array multiplier [7].

We have used single wall CNT Stanford's spice model for CNTFET spice simulation. We have optimised the parameters of CNTFET in such a way to maintain balance between speed and power consumption. Though there were earlier works on the basis of logic design using CNTFETs, we are trying to examine the potential of logic design with GDI technique in a complex multiplier architectures using CNTFETs rather than CMOS. Also, we have proposed novel D-Flipflop with 10 transistors (excluding reset transistor) with a single clock load by concatenating the positive and negative True Single Phase Clock (TSPC) Latches [8], [9] and a 10T-based full adder design to reduce area and power consumption.

The rest of the paper is organized as follows: In sectionIII, we have explained the SSPM algorithm. Section-IV gives details of the design of the GDI-based logic cells and proposed flip-flops using CNTFETs. Section-V discusses the analysis of the simulation results, and finally, Section-VI provides the conclusion.

II. Background

CNTFETs use Carbon NanoTube(CNT) as the channel material, unlike bulk as a channel material in traditional MOSFETs [1]. CNTs are rolled-up sheets of hexagonal structure of graphene [10] along the direction of Chiral Vector. Chiral vector is given by C_h = (n, m). Depending upon the chiral vector, CNT is classified as metallic or semiconducting [1].

In this paper, the logic gates are designed using CNTFETs instead of the CMOS transistors to achieve low power consumption, less propagation delay and less area. To reduce the transistor count, delay and power consumption, we have utilised the Gate Diffusion Input technique (GDI) [11].

TABLE I: Number leaf cells present in different multipliers

N	P	G	Out	Function
$'0'$	B	A	AB	AND
Vdd	B	A	$A+B$	OR
B	A	S	$\overline{S}$A+ SB	$2:1MUX$
$\overline{B}$	B	A	$\overline{A}$B+A$\overline{B}$	$EXOR$
B	$\overline{B}$	A	$A\,\overline{B}+AB$	$EX-NOR$

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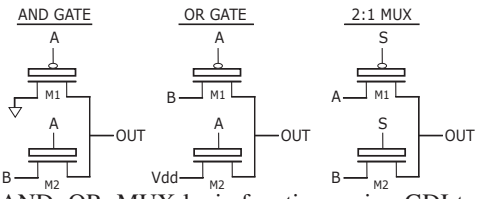

Fig. 1: AND, OR, MUX logic functions using GDI technique

From Fig. 1, it is observed that changing the source/drain and gate terminals produces different logic functions like AND, OR, 2×1 MUX, XOR, and XNOR, as shown in Table-I. The GDI based 4×1 Multiplexer is designed based on the 2×1 Multiplexer.

III. Systolic Serial Parallel Multiplier

The multiplication of two numbers such as A and X are shown in equation (1). The direct implementation of this multiplication based on the equation (1) will take 2N clock cycles to produce the final output and to accept new input data. SPM is also based on the same equation (1) and takes 2N clock cycles and the worst case scenario propagation delay (T_{pmax}) of SPM is through an AND gate and full adder. SPM is only 50% efficient and also it has a disadvantage of broadcasting it's serial input to all multiplier cells which makes SPM unfit for high frequency clock signals, large number multiplication.

$$Y = A.X = (\sum_{i=1}^{n-1} a_i.2^i).X \tag{1}$$

The other alternative to SPM is Systolic Serial Parallel Multiplier (SSPM), which operates with 100% efficiency and a decrease in partial product summands by N/2 based on the equation (2). It has a greatest advantage of computing n-bit multiplication with latency of only N+2 clock cycles. The 16-bit SSPM as shown in Fig. 2 is designed based on 8-bit SSPM proposed in [6] and modeled using CNTFETs. Like SPM, one of the input is directly applied in parallel form to multiplier cells (Combination of full adder and 4:1 MUX) and other input X is fed serially with LSB first.

$$Y = A.X = (\sum_{i=1}^{n-1} a_i.2^i).X = \sum_{j=0}^{n/2-1} (a_{2j} + 2a_{2j+1}).2^{2j}.X \tag{2}$$

This SSPM is based on product $3X$ and 100% efficient which means no zero words are inserted between successive inputs. The product term in equation (2) can take the values from 0, X, 2X, 3X. 2X term is achieved by left shifting input X through a delay element. 3X term is achieved by serial addition of X and 2X terms using a full adder. A 4:1 mux selects either of these terms depending on parallel input 'A' applied to it's select line. Control signal/ initialisation signal 'R' is a key factor in making this multiplier 100% efficient by helping it to download a multiplier cell's sum and carry bit value to the designated register. 'R' is a travelling signal and it is activated to be high at the second zero bit which was sent as a stop bit to isolate multiplier cells [12] sent after n-bit data input. This proposed SSPM has another feature where least significant part of the product is obtained through output line P_L and most significant part of the product is obtained through P_H making it 100% efficient.

IV. CNTFET-based Logic circuits using GDI Technique

GDI primary cell consists of one p-type and one n-type transistor, and it has three inputs i,e., one common gate input, other input to source/drain terminal of pCNTFET (P), and another input to source/drain terminal of nCNTFET (N). Various logic functions can be realized by varying these three inputs to a basic GDI cell, as shown in Table-I.

$$Average\ power = \frac{Energy}{t_1 - t_0} \tag{3}$$

A. Proposed flip flop

The proposed flip flop is as shown in Fig. 3 and it requires only 11 transistors. To eliminate the race conditions, our proposed D-FlipFlop operates on only single phase clock signal without the inverted clock signal. This proposed flip-flop operates on master latch (transistor $M1$ to $M5$) and slave (transistors $M6$ to $M11$) latch configuration. When clk= 1 right before falling edge, master latch is in transparent mode propagating it's output to Node $N3$ while slave latch is in hold mode and vice-versa when clk= 0. when RST =0, no matter the input data 'D', output Q = 0.

In our proposed flipflop design, clock load is only on two transistors, this will lead to less power dissipation. The proposed flip flop has low setup time (t_{Setup}), hold time (t_{hold}), clock to output propagation delay (t_{Pc-q}) compared to other existing flip flops as shown in Table-III

B. Full Adder

The designed full adder shown in Fig. 4 is based on the principle of EXOR and EX-NOR logic. The Node P in the circuit represents XOR output and $\overline{P}$ represents EXNOR output. It is defined that sum is P xor C_{in}. When P =1, C_{out} = C_{in} and when P =0, C_{out} = either A or B.

Though using GDI logic has advantages like less complexity and low power consumption, it suffers from threshold voltage drop across it's cells. It can be clearly seen through the outputs of MUX, OR gate and Full Adder. This problem can be overcome by using proper buffers or restoration logic to achieve full logic swings.

The comparison of average power and the number of the transistors required to design the basic logic gates and GDI based logic gates are as shown in Table-V.

TABLE II: Number leaf cells present in different multipliers

Multiplier Cells	8×8	16×16	24×24	32×32
D-flipflop	27	55	83	111
Full Adder	6	10	14	18
$4 \times 1 Mux$	4	8	12	16
$2 \times 1 Mux$	7	15	23	31
OR Gate	3	7	11	15

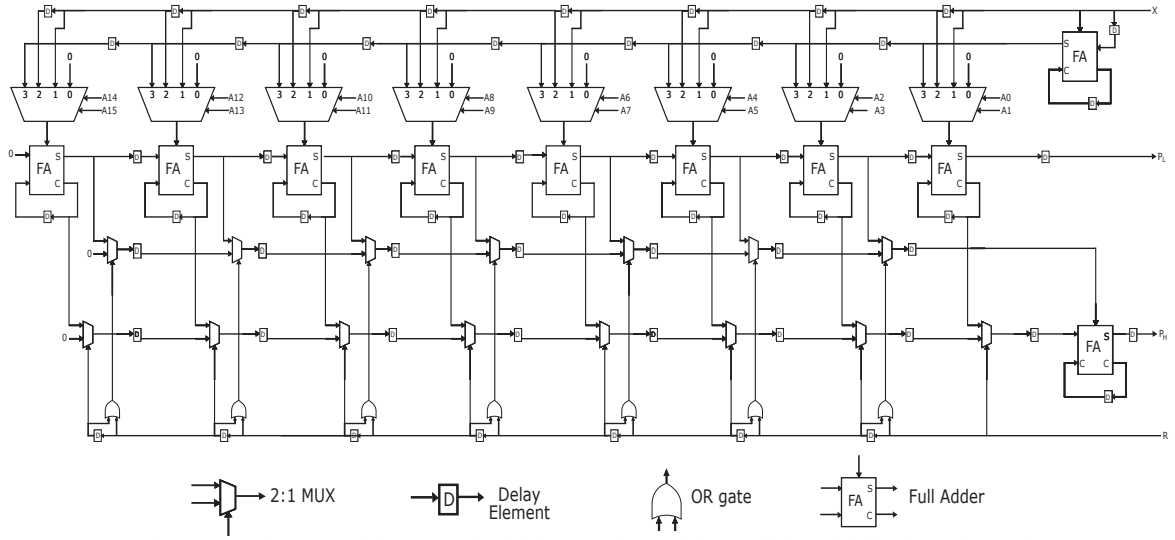

Fig. 2: Hardware Architecture of 16-bit Systolic Serial Parallel Multiplier based on [6]

TABLE III: Comparison of existing Flip-flops with proposed flip-flop

Type	t_{Setup} (ps)	t_{hold} (ps)	t_{Pc-q} (ps)	Clock Load	T_{count}	P_{avg} (μw)	Energy (pJ)
Nand logic [13]	0.4	1.0	1.16	2	26	**161.16**	**16.116**
TG logic Mux [9]	0.6	1.0	0.89	8	22	**26.87**	**2.687**
C^2MOS [14]	46.0	40.0	32.01	4	10	**0.05**	**0.004**
TSPC [8]	0.5	0.1	0.53	4	11	**7.59**	**0.759**
Proposed	0.4	0.1	0.25	2	10	**0.03**	**0.003**

TABLE IV: Comparing systolic serial parallel multiplier results; VDD = 2.5v and 1.5v

Type	Latency	Power dissipation (μW)	Delay (ps)	No. of Transistors	PDP (fJ)	Energy (pJ)
8-bit SSPM (2.5v)	10	850.0	44.7	401	37.9	35.5
8-bit SSPM (1.5v)	10	12.8	44.7	401	0.6	0.6
8-bit SAM (ANx) [7](1.5v)	17	317.8	2390	2312	759.7	-
8-bit SSPM [6]	-	-	-	688	-	-
16-bit SSPM (2.5v)	18	1321.3	80.4	797	106.3	89.8
24-bit SSPM (2.5v)	26	1911.1	116.2	1193	222.1	210.2
32-bit SSPM (2.5v)	34	2584.0	151.9	1589	392.7	361.7

TABLE V: Comparison of Basic logic gates with GDI based logic gates

	GDI based Logic Circuits		CMOS based Logic Circuits	
	Avg. Power (μw)	Total No. of transistors	Avg. Power (μw)	Total No. of transistors
OR Gate	0.0021	2	0.2618	6
AND Gate	0.0027	2	0.0433	6
2×1 Mux	0.0266	2	0.1777	12
Full Adder	0.2831	10	6.0173	28

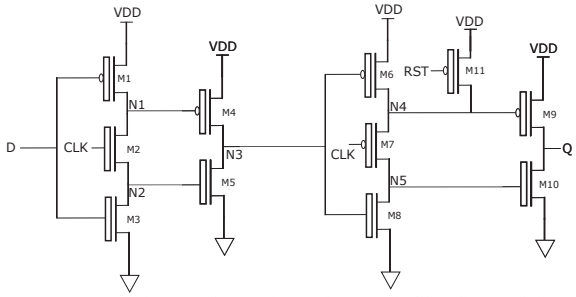

Fig. 3: Proposed negative edge triggered flip flop with reset switch

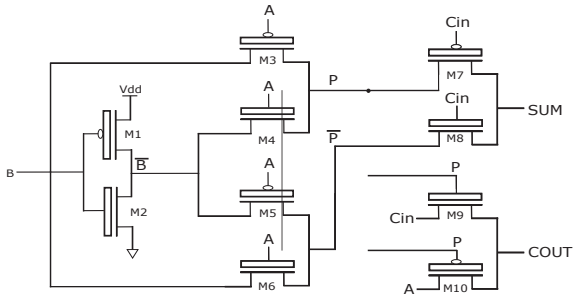

Fig. 4: Full adder design based on EXOR-EXNOR principle using GDI technique

V. Results

In this paper, to achieve energy efficient multiplier design, we have utilised GDI based logic gates and proposed a new D flip-flop. Total number of logic gates required for different bit-size multiplier is as shown in Table-II. Hardware complexity per bit has been reduced from 100 [11] to 61 transistors for an 8-bit systolic serial parallel multiplier. The simulation results of the 16-bit SSPM as shown in Fig. 5. For analysis, we have applied randomly input $X = 1111110000111000$ which is equivalent to 64568 in decimal is fed serially as

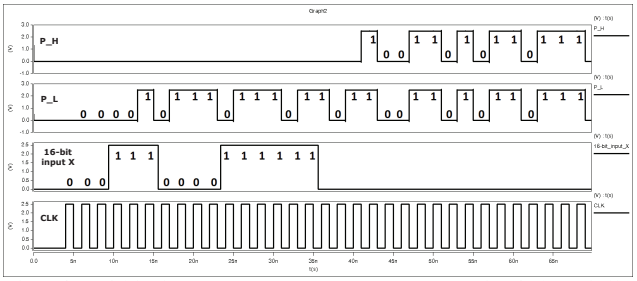

Fig. 5: 16-bit input X =1111110000111000 is fed serially starting with LSB first. Product obtained serially over P_L and P_H starting with LSB first.

shown in Fig. 5 and other input $A = 1111000011110110$ which is equivalent to 61686 in decimal is applied directly to multiplier cells and it produced the Product as $P = 11101101011001101101110111010000$ which is equivalent to 3982941648 in decimal is obtained serially starting with LSB first. Delay elements are added next to right most multiplier cell on product lines P_L and P_H for a nice dynamic response and it is not mandatory to add those. Energy is calculated based on the equation- (3) [15], where t_1,t_0 are the initial and final points of the time period in which both average power and energy of the circuit are calculated respectively.

We have compared our designs with the existing designs as shown in Table-IV. The Table-IV provides comparisons for area (transistor count), latency, delay, power and PDP and Energy consumption. From the Table-IV, we can observe that our proposed design requires 41% less number of transistors compared to the [6]. The other details of [6] are missing and could not be compared for this reason. The proposed design when compared to [7] has savings in area by 82.65%, decrease in power by 95.96%, savings in PDP by 99.92% respectively and other details like energy consumption is missing in [7],and could not be compared for this reason.

VI. Conclusion

In this paper, we have presented a design of Systolic Serial Parallel Multiplier with GDI based logic cells using CNTFETs. Higher order systolic serial parallel multiplier requires large number of D flip-flops. The proposed D flip-flop consumes low power and requires less clock load, and it is faster than the existing flip-flops as shown in Table-III. The GDI based CNTFET logic circuits are compared with CMOS and presented in Table-V. The proposed design of multiplier has less area transistor count, latency, delay, power and PDP values than compared to existing multiplier designs as shown in Table-IV. The simulation results have been carried out in HSPICE. The design of SSPM can be further improved by replacing left far most multiplier cell's full-adder with just an half adder since that multiplier cell does not generate any carry bits, so that area and power dissipation can be further reduced.

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