SYSTEM DESIGN THROUGH VERILOG
(Elective- I)

UNIT-I
INTRODUCTION TO VERILOG:
Verilog as HDL, Levels of design description, concurrency, simulation and synthesis, functional verification, system tasks, programming language interface(PLI), module, simulation and synthesis tools, test benches.
LANGUAGE CONSTRUCTS AND CONVENTIONS:
Introduction, keywords, identifiers, whitespace characters, comments, numbers, strings, logic values, data types, scalars and vectors, parameters, memory, operators, system tasks.

UNIT-II
GATE LEVEL MODELLING:
Introduction, AND gate primitive, module structure, other gate primitives, illustrative examples, tristate gates, array of instances of primitives, design of Flip flops with gate primitives, delays, strengths and contention resolution, net types, design of basic circuits.

UNIT-III
BEHAVIORAL MODELLING:
Introduction, operations and assignments, functional Bifurcation, initial construct, always construct, examples, assignments with delays, wait construct, multiple always blocks, designs at behavioral level, blocking and non-blocking assignments, the case statement, simulation flow, if and if else constructs, assign-De assign construct, repeat construct, FOR loop, the disable construct, While loop, Forever loop, parallel blocks, force-release construct, event.

UNIT-IV
DATAFLOW LEVEL AND SWITCH LEVEL MODELLING:
Introduction, continuous assignment structures, delays and continuous assignments, assignment to vectors, basic transistor switches, CMOS switch, Bidirectional gates and time delays with switch primitives, instantiations with strengths and delays, strength contention with trireg nets.

UNIT-V
SYNTHSIS OF COMBINATIONAL AND SEQUENTIAL LOGIC USING VERILOG: Synthesis of
combinational logic: Net list of structured primitives, a set of continuous assignment statements and level sensitive cyclic behavior with examples, Synthesis of priority structures, Exploiting logic don't care conditions. Synthesis of sequential logic with latches: Accidental synthesis of latches and Intentional synthesis of latches, Synthesis of sequential logic with flip-flops, Synthesis of explicit state machines.

UNIT-VI
VERILOG MODELS:
Static RAM Memory, A simplified 486 Bus Model, Interfacing Memory to a Microprocessor Bus, UART Design and Design of Microcontroller CPU.

TEXT BOOKS:
1. Design through Verilog HDL – T.R. Padmanabhan and B. Bala Tripura Sundari, WSE, IEEE Press, 2004.
2. Advanced Digital Design with Verilog HDL – Michael D. Ciletti, PHI, 2005.

REFERENCES:
1. Fundamentals of Logic Design with Verilog – Stephen. Brown and Zvonko Vranesic, TMH, 2005.
2. A Verilog Primier – J. Bhasker, BSP, 2003.