eSim Semester Long Internship Autumn 2025

On

IC Integration and Subcircuit Creation

Submitted by

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January 17, 2026

Acknowledgment

I would like to express my deepest gratitude to **Prof. Prabhu Ramachandran** for providing me the opportunity to be a part of the FOSSEE internship program and for supporting open-source engineering tool development at IIT Bombay. His guidance and vision have encouraged students and researchers to actively contribute to the open-source ecosystem.

I would also like to acknowledge **Prof. Kannan M. Moudgalya** for his foundational role in establishing and nurturing the FOSSEE initiative. His contributions toward open-source education and the creation of the FOSSEE fellowship framework have directly shaped the platform through which this internship was undertaken.

My sincere appreciation extends to my mentor, **Mr. Sumanto Kar**, for his continual support, technical guidance, and encouragement throughout the duration of this project. His insights and feedback played a key role in refining ideas, overcoming challenges, and ensuring the timely completion of the tasks assigned to me.

I would also like to thank my internal mentors, **Mr. Varad Patil**, **Ms. Shanthi Priya K**, and **Mr. Aditya M**, for their valuable guidance, coordination, and technical inputs during the internship. Their mentorship contributed significantly to the clarity, progress, and successful execution of the work.

This internship has been an enriching learning experience, allowing me to work closely with open-source EDA tools, develop IC subcircuits in eSim, and gain exposure to real-world circuit modeling and simulation workflows. The knowledge acquired during this period will undoubtedly support my future academic and professional pursuits.

I would also like to thank the entire **FOSSEE team** for their coordination, assistance, and timely interactions at various stages of this work. Their collective efforts ensured smooth workflow, resource accessibility, and effective project execution.

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Chapter 1

Introduction

FOSSEE which stands for Free/Libre and Open Source Software for Education is an organization, based at IIT Bombay, as a remarkable initiative aimed at promoting the use of open-source software in education and research. It was established with the mission to reduce the dependency on proprietary software and to encourage the adoption of open-source alternatives. FOSSEE offers a wide range of tools and resources that cater to various academic and professional needs.

It provides comprehensive documentation, tutorials, workshops, and hands-on training sessions, for empowering students, educators, and professionals to leverage open-source software for their projects and coursework. The organization's commitment to fostering a collaborative and inclusive environment has significantly contributed to the democratization of technology and has opened up new avenues for innovation and learning. FOSSEE which stands for Free/Libre and Open Source Software for Education is an organization, based at IIT Bombay, as a remarkable initiative aimed at promoting the use of open-source software in education and research.

1.1 eSim

eSim, created by the FOSSEE project at IIT Bombay, is a versatile open-source software tool for circuit design and simulation. It combines various open-source software packages into one cohesive platform, making it easier to design, simulate, and analyze electronic circuits. This tool is particularly useful for students, educators, and professionals who need an affordable and accessible alternative to proprietary software.

eSim offers features for schematic creation, circuit simulation, PCB design, and includes an extensive library of components.The Subcircuit feature is a significant enhancement, enabling users to design complex circuits by integrating simpler subcircuits. Through eSim, FOSSEE promotes the use of open-source solutions in engineering education and professional fields, encouraging innovation and collaboration.

1.2 NgSpice

NgSpice is the open-source spice simulator for electric and electronic circuits. Such a circuit may comprise JFETs, bipolar and MOS transistors, passive elements like R, L, or C, diodes, transmission lines and other devices, all interconnected in a netlist.

Digital circuits are simulated as well, event-driven and fast, from single gates to complex circuits and the combination of both analog and digital as well as a mixed-signal circuits. NgSpice offers a wealth of device models for active, passive, analog, and digital elements. Model parameters are provided by our collections, by the semiconductor device manufacturers, or from semiconductor foundries. The user adds her circuits as a netlist, and the output is one or more graphs of currents, voltages and other electrical quantities or is saved in a data file.

1.3 Makerchip

Makerchip is a platform that offers convenient and accessible access to various tools for digital circuit design. It provides both browser-based and desktop-based environments for coding, compiling, simulating, and debugging Verilog designs. Makerchip supports a combination of open-source tools and proprietary ones, ensuring a comprehensive range of capabilities.

One can simulate Verilog/SystemVerilog/Transaction-Level Verilog code in Makerchip. eSim is interfaced with Makerchip using a Python based application called Makerchip-App which launches the Makerchip IDE. Makerchip aims to make circuit design easy and enjoyable for users of all skill levels. The platform provides a user-friendly interface, intuitive workflows, and a range of helpful features that simplify the design process and enhance the overall user experience.

The main drawback of these open source tools is that they are not comprehensive. Some of them are capable of PCB design (e.g. KiCad) while some of them are capable of performing simulations (e.g. gEDA). To the best of our knowledge, there is no open source software that can perform circuit design, simulation and layout design together. eSim is capable of doing all of the above.

Chapter 2

Feautures Of eSim

The objective behind the development of eSim is to provide an open source EDA solution for electronics and electrical engineers. The software should be capable of performing schematic creation, PCB design and circuit simulation (analog, digital and mixed-signal). It should provide facilities to create new models and components. Thus, eSim offers the following features -

1. Schematic Creation: eSim provides an easy-to-use graphical interface for drawing circuit schematics, making it accessible for users of all levels. Users can drag and drop components from the library onto the schematic, simplifying the design process. Comprehensive editing tools allow for easy modification of schematics, including moving, rotating, and labeling components.

2. Circuit Simulation: eSim supports SPICE (Simulation Program with Integrated Circuit Emphasis), a standard for simulating analog and digital circuits. Users can perform various types of analysis such as transient, AC, and DC, providing insights into circuit behavior over time and frequency.An integrated waveform viewer helps visualize simulation results, aiding in the analysis and debugging of circuit designs.

3. PCB Design: The PCB layout editor allows users to place components and route traces with precision. eSim includes DRC capabilities to ensure that the PCB design adheres to manufacturing constraints and electrical rules. Users can generate Gerber files, which are standard for PCB fabrication, directly from their designs.

4. Subcircuit Feature: This feature enables users to create complex circuits by integrating smaller, simpler subcircuits, promoting modular and hierarchical design approaches. Subcircuits can be reused in different projects, saving time and effort in redesigning common circuit elements.

5. Open Source Integration: eSim integrates several open-source tools like KiCad, Ngspice, and GHDL, providing a comprehensive suite for electronic design automation. Being open-source, eSim is free to use, making advanced circuit design tools accessible without the need for expensive licenses.

Chapter 3

Problem Statement

To design and develop various Analog and Digital Integrated Circuit Models in the form of sub-circuits using device model files already present in the eSim library. These IC models should be useful in the future for circuit designing purposes by developers and users, once they get successfully integrated into the eSim subcircuit Library.

3.1 Approach

Our approach to implementing the problem statement began with examining datasheets from prominent Integrated Circuit (IC) manufacturers such as Texas Instruments, Analog Devices, and NXP Semiconductors. we selected ICs that offer a diverse range of functionalities, including precision amplifiers, comparators, encoders, and audio amplifiers. After building the subcircuits, we tested them to verify basic circuit configurations using NgSpice simulations. The step-by-step roadmap of this process is outlined below :

1. Analyzing Datasheets : The primary step is to browse through various analog and digital IC datasheets, and hence find suitable circuits to implement in eSim, that are not previously included into the eSim library. Check for the detailed schematic of the IC's and once the component values and the truth table is ascertained, then finalise the IC to be created.

2. Subcircuit Creation : After deciding the IC, we start modeling it as a subcircuit in eSim, using the model files present in the eSim device model library only. The design is strictly according to the information given in the official data-sheets of the ICs.This step also includes building the Symbol/Pin diagram of the IC according to the packaging and pin description given in the data-sheets only.

3. Test Circuit Design : Once the component of the IC is ready, now we can build the test circuits, according to the data-sheets. In this step we build the test cases and test circuits using the component IC.

4. Schematic Testing : Once the test circuits are ready, now it's time to simulate the test circuits so that the output can be obtained in the form of wave-forms and

plots. Here we take help of KiCad to NgSpice conversion and Simulation feature in eSim

If the output of the test circuit is not as per expectation, this implies that the test case has failed, and there is some error in the schematic. In such cases we go back to the design phase of the IC or the test circuits, to look for possible errors and then repeat the testing process again after making required changes.

Once the expected output of the test cases are correct and satisfy the expected results, then in such a case the IC is declared successfully working. The test case has been verified and the designing process is complete.

Chapter 4

Integrated Circuits

4.1 SN54LS373 - OCTAL D-TYPE TRANSPARENT LATCHES

The SN54/74LS373 is an 8-bit D-type transparent latch designed for temporary data storage in digital systems. When the enable (C) input is high, the outputs directly follow the input data, making the latch transparent. When the enable goes low, the data present at the inputs is latched and held at the outputs. The device features 3-state outputs, allowing it to be connected directly to a shared data bus without causing bus contention. An output control (OC) pin places the outputs in a high-impedance state without affecting the stored data. Buffered control inputs improve noise immunity and reliable operation. The LS373 is commonly used in buffer registers, I/O interfacing, and bus-oriented architectures.

4.1.1 IC Layout

This figure represents the Pin Package Diagram of SN54LS373 ic

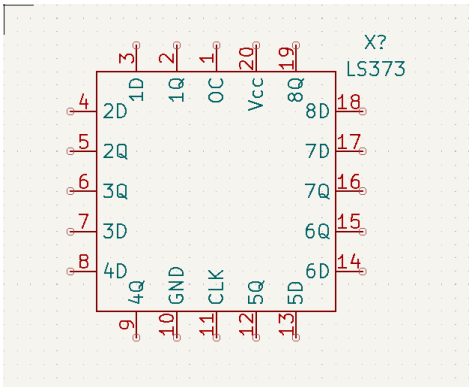

Figure 4.1: Pin diagram of SN54LS373

4.1.2 Subcircuit Schematic Diagram

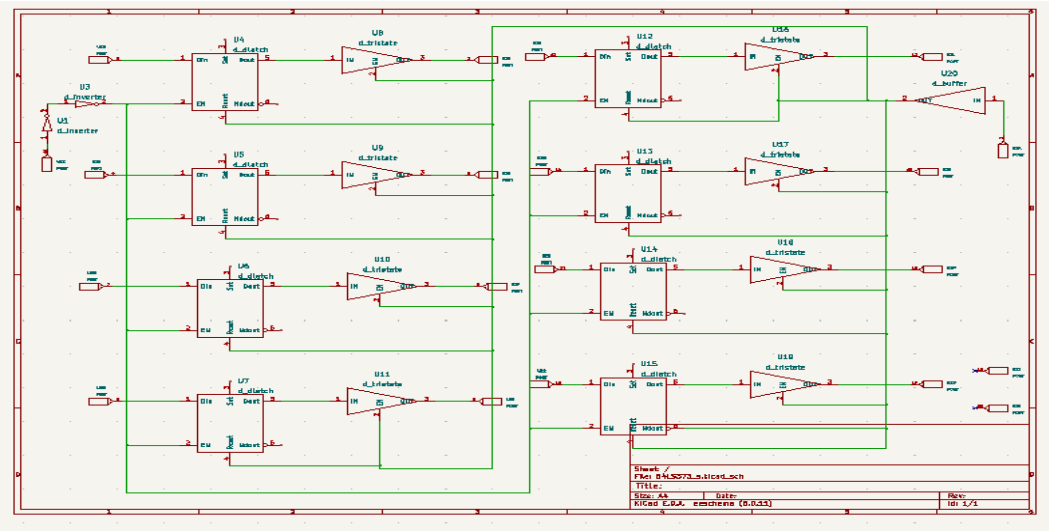

Figure 4.2: Subcircuit Schematic of SN54LS373

4.1.3 Test Circuit

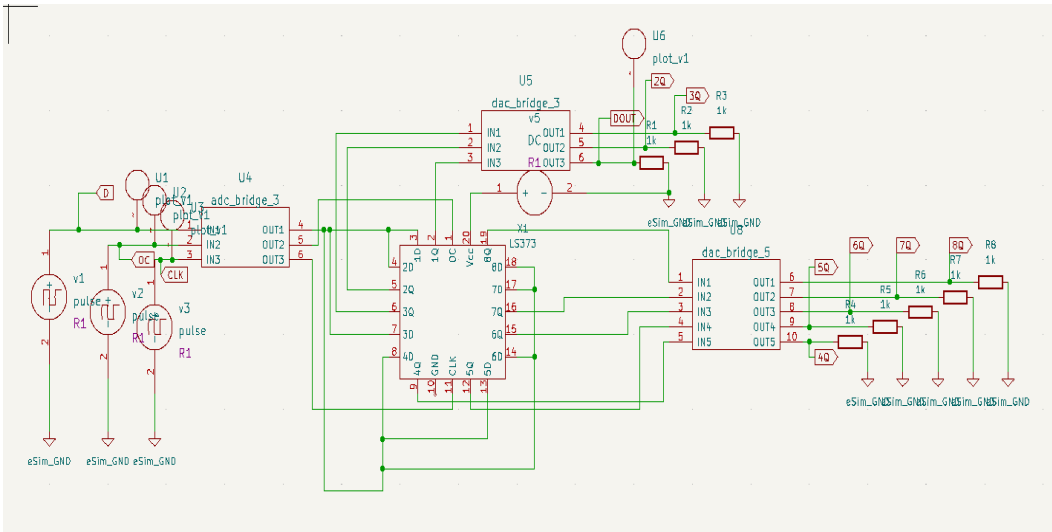

Figure 4.3: Test Circuit of SN54LS373 IC

4.1.4 Input Plots

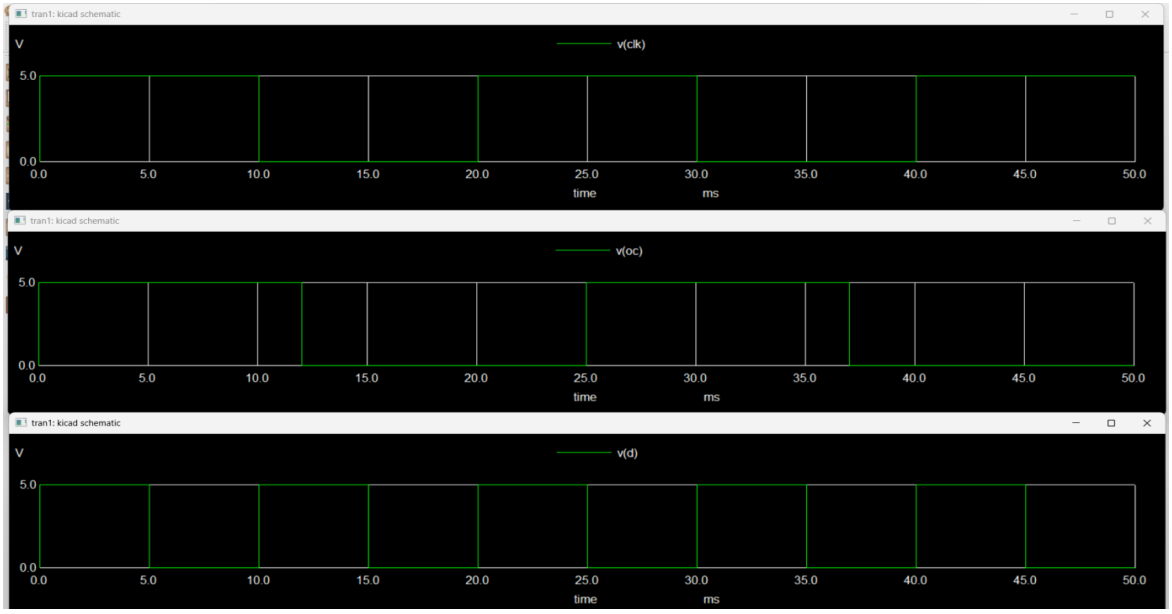

Figure 4.4: Input Voltage Waveform of SN54LS373

4.1.5 Output Plots

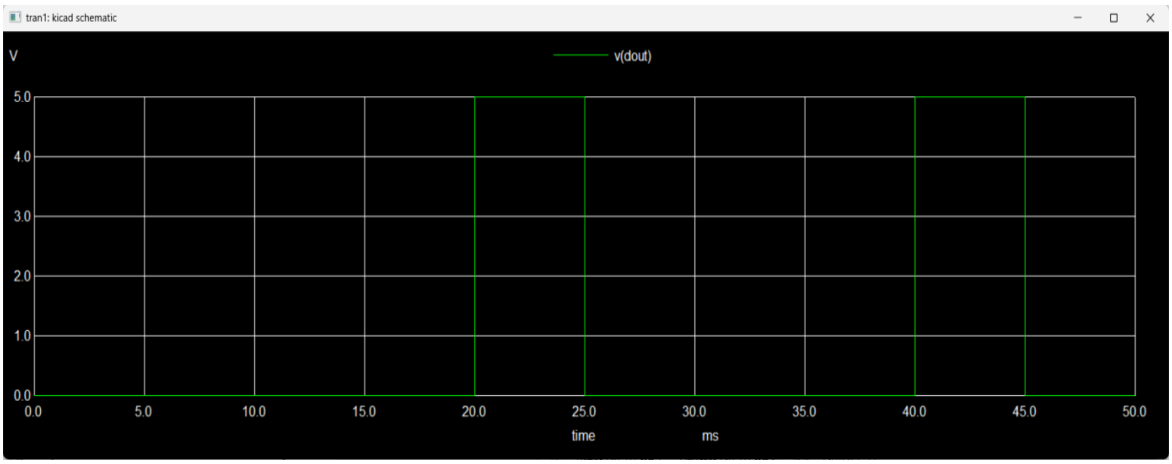

Figure 4.5: Output Voltage Waveform of SN54LS373

4.2 SN54166 - 8 - BIT PARALLEL-LOAD SHIFT REGISTER

The SN54/74LS166A is an 8-bit parallel-load shift register used for efficient data handling in digital systems. It allows parallel data inputs to be loaded simultaneously into the register. Using a shift/load control, the device can switch between loading data and shifting it serially. Data shifting occurs synchronously with the clock input, ensuring controlled timing. A serial output provides parallel-to-serial data conversion for communication purposes. An asynchronous clear input resets all stored data to zero when required. This IC is commonly used in data serialization, registers, and digital communication circuits.

4.2.1 IC Layout

This figure represents the Pin Package Diagram of SN54166

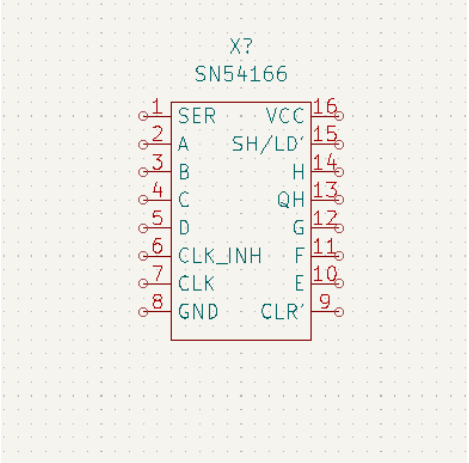

Figure 4.6: Pin diagram of SN54166

4.2.2 Subcircuit Schematic Diagram

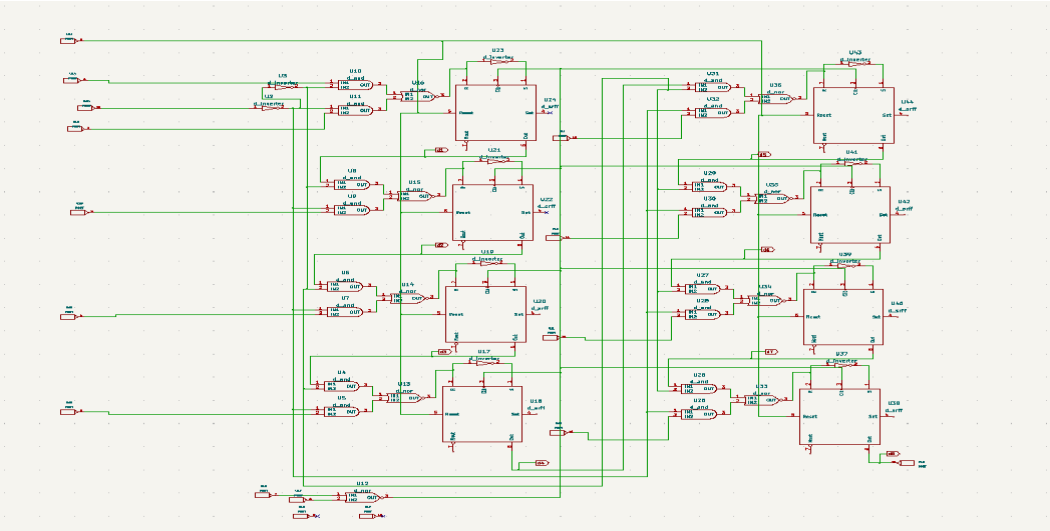

Figure 4.7: Subcircuit Schematic of SN54166

4.2.3 Test Circuit

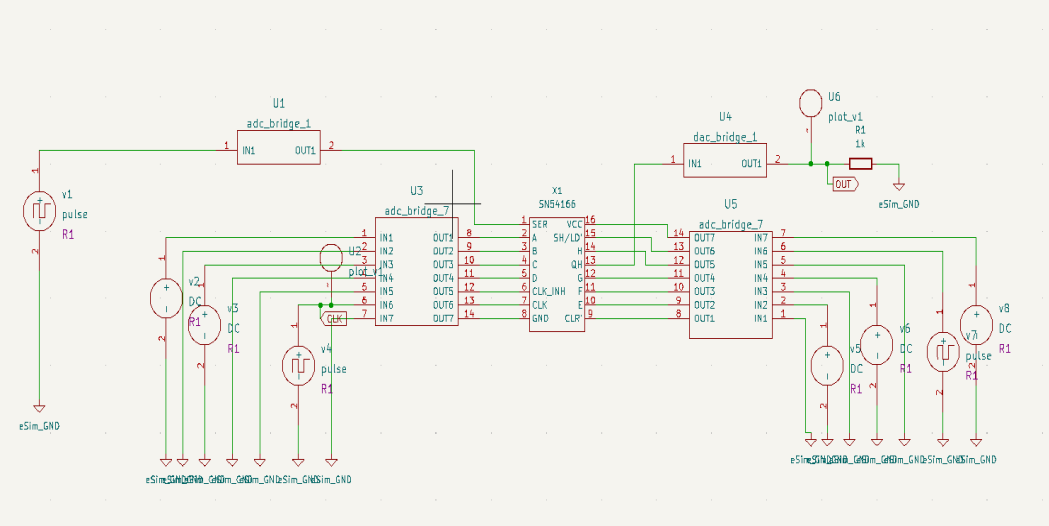

Figure 4.8: Test Circuit of SN54166 IC

4.2.4 Input Plots

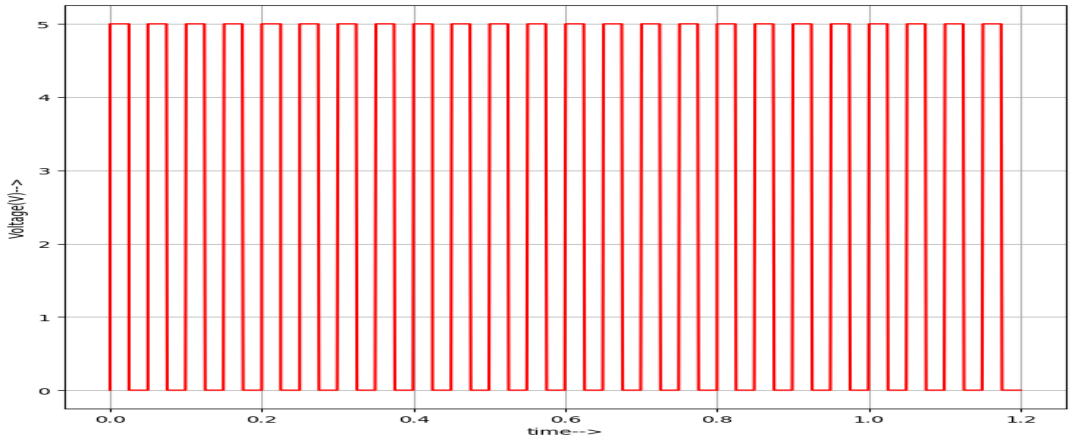

Figure 4.9: Input Voltage Waveform of SN54166

4.2.5 Output Plots

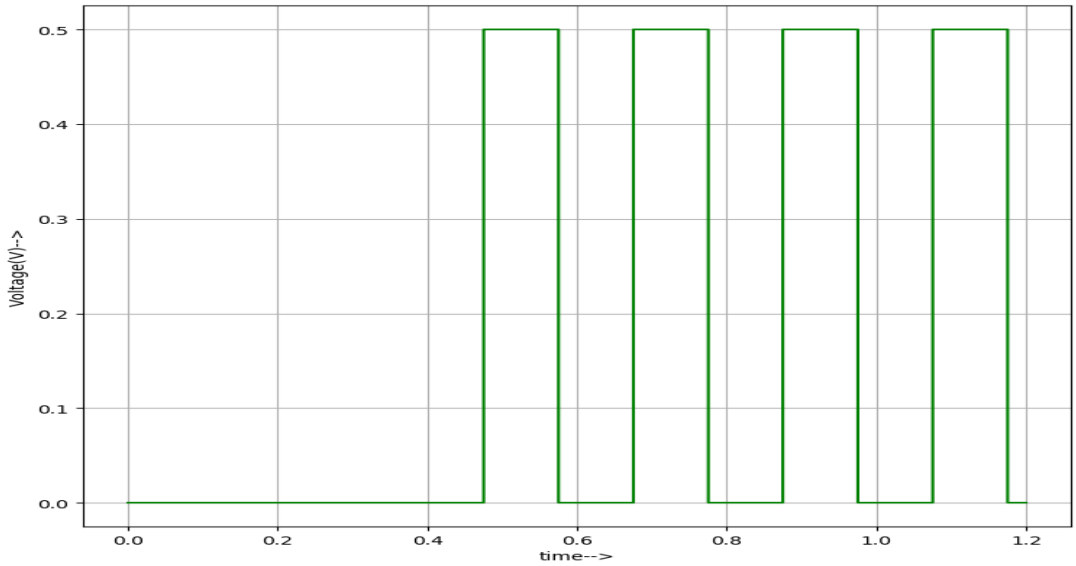

Figure 4.10: Output Voltage Waveform of SN54166

4.3 CD74HC390 - DUAL DECADE RIPPLE COUNTER

The CD74HC390 / CD74HCT390 is a dual 4-bit decade ripple counter designed using high-speed CMOS logic technology. It contains two independent counters in a single package, each capable of operating as a decade or bi-quinary counter. Each counter is internally divided into a divide-by-2 and a divide-by-5 section, enabling flexible frequency division. The device operates with falling-edge triggered clocks, making it suitable for ripple counting applications. Independent asynchronous clear inputs allow each counter to be reset individually. By appropriate interconnection, the IC can be configured for divide-by-2, 4, 5, 10, 20, 25, 50, or 100 operations. The HC version supports wide supply voltage operation, while the HCT version is TTL input compatible. It offers low power consumption compared to traditional TTL counters. The device provides good noise immunity and balanced propagation delays. It is widely used in frequency dividers, digital clocks, counters, and timing circuits.

4.3.1 IC Layout

This figure represents the Pin Package Diagram of CD74HC390

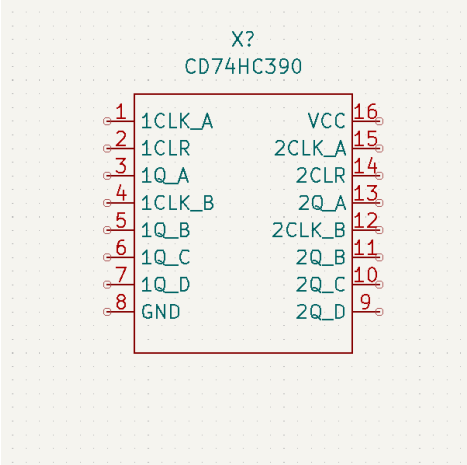

Figure 4.11: Pin diagram of CD74HC390

4.3.2 Subcircuit Schematic Diagram

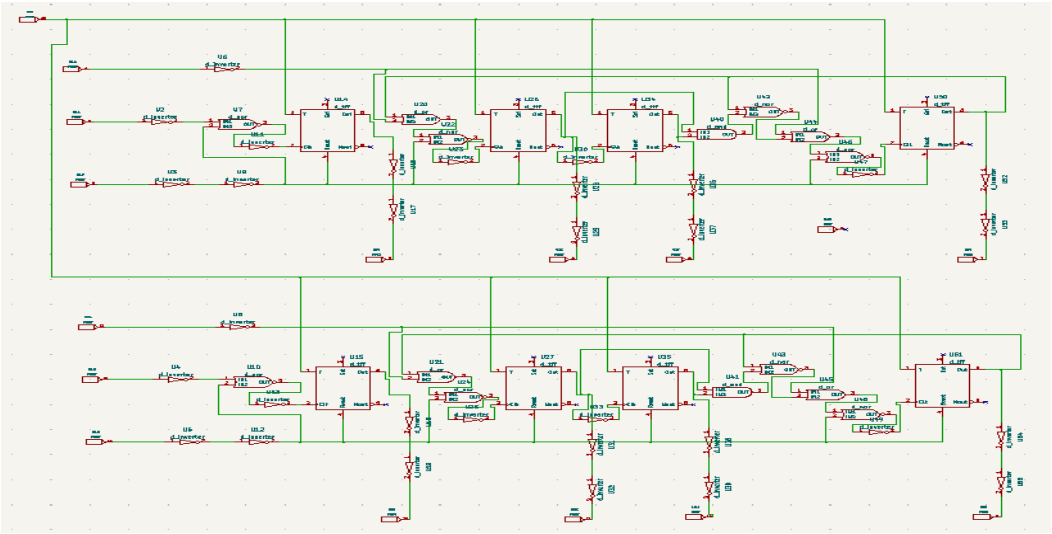

Figure 4.12: Subcircuit Schematic of CD74HC390

4.3.3 Test Circuit

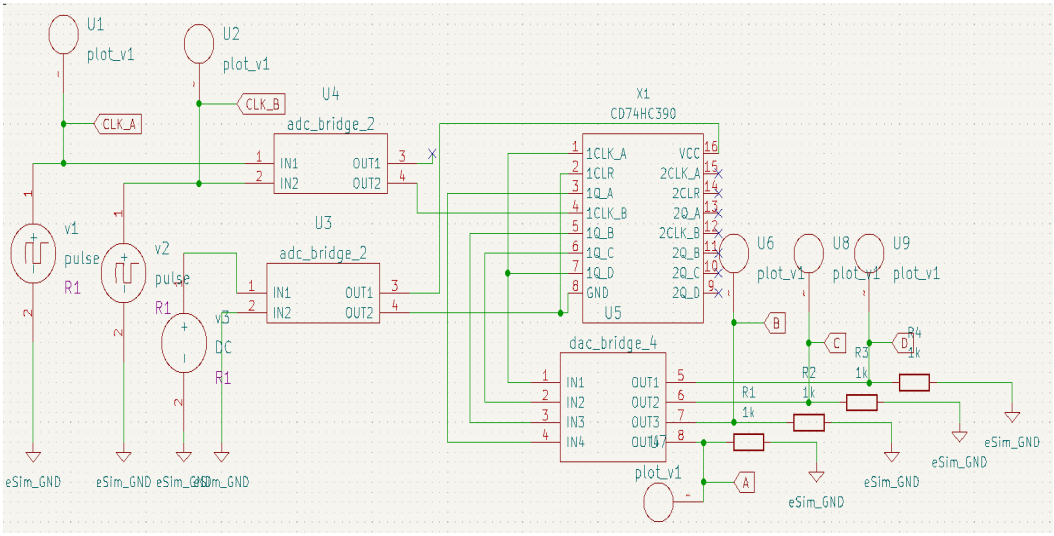

Figure 4.13: Test Circuit of CD74HC390 IC

4.3.4 Input Plots

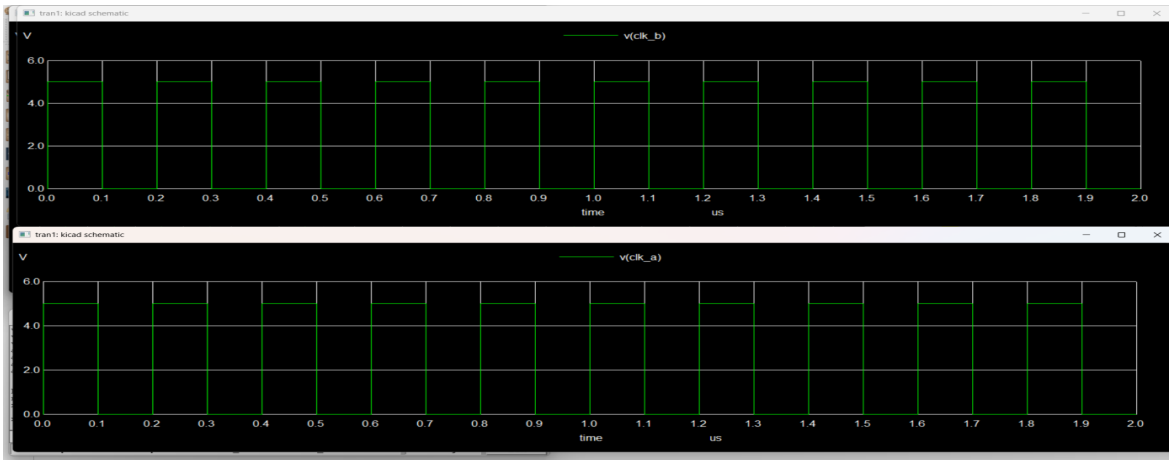

Figure 4.14: Input Voltage Waveform of CD74HC390

4.3.5 Output Plots

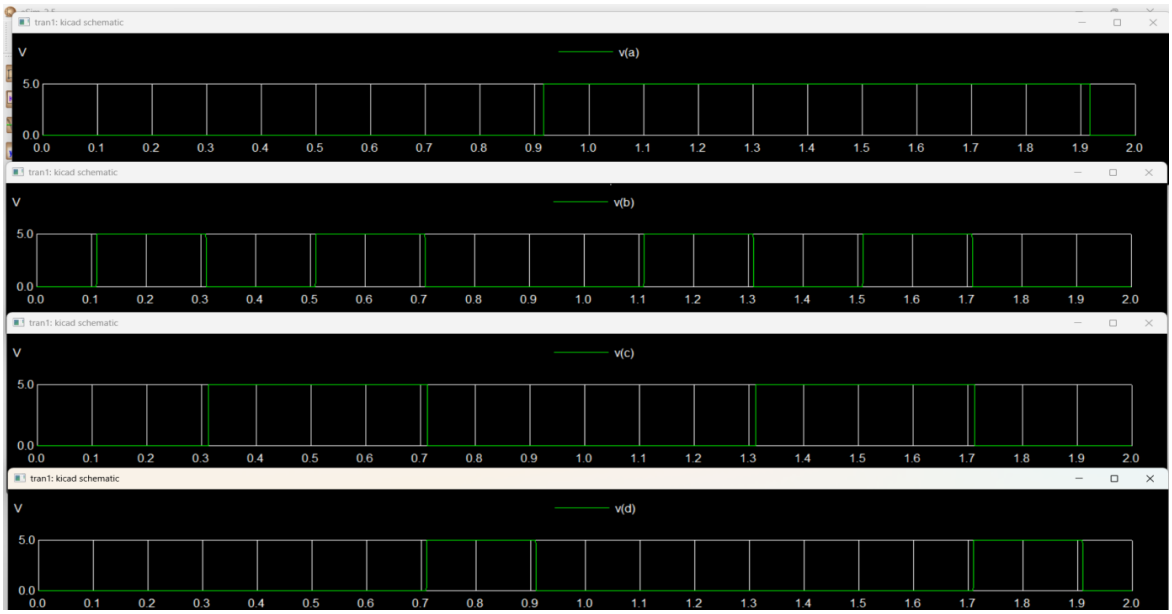

Figure 4.15: Output Voltage Waveform of CD74HC390

4.4 SN74LS299 - 8 BIT SHIFT/STORAGE REGISTER

This device is a digital component designed to perform multiple data-handling operations such as storing, shifting, loading, or transferring information depending on the selected mode. It operates using control inputs that determine whether data is shifted left, shifted right, loaded in parallel, or held constant, while the clock signal ensures synchronized movement of bits inside the register. The internal architecture typically consists of flip-flops arranged in series with multiplexed inputs so that data can flow in different directions based on external control logic. Additional pins like output enable, reset, and serial input allow easy interface with microprocessors, communication circuits, and cascading with other registers to build larger systems. The device ensures flexible data manipulation with reduced pin count, supports expansion through serial chaining, and maintains stable digital storage even at high operating speeds. It is commonly used in systems requiring temporary data buffering, serial-to-parallel or parallel-to-serial conversion, and sequencing applications in embedded and communication hardware. This makes it ideal for efficient data organization, reliable timing-based shifting, and compact digital design implementations in modern electronic circuits.

4.4.1 IC Layout

This figure represents the Pin Package Diagram of SN74LS299

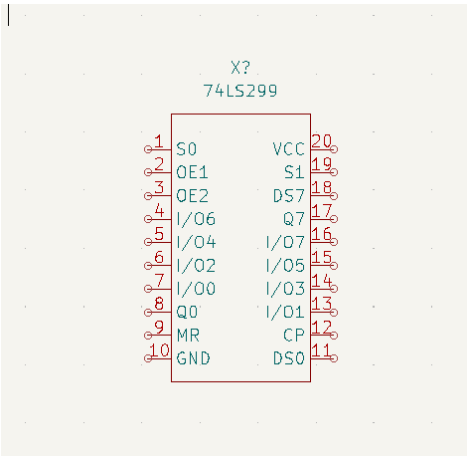

Figure 4.16: Pin diagram of SN74LS299

4.4.2 Subcircuit Schematic Diagram

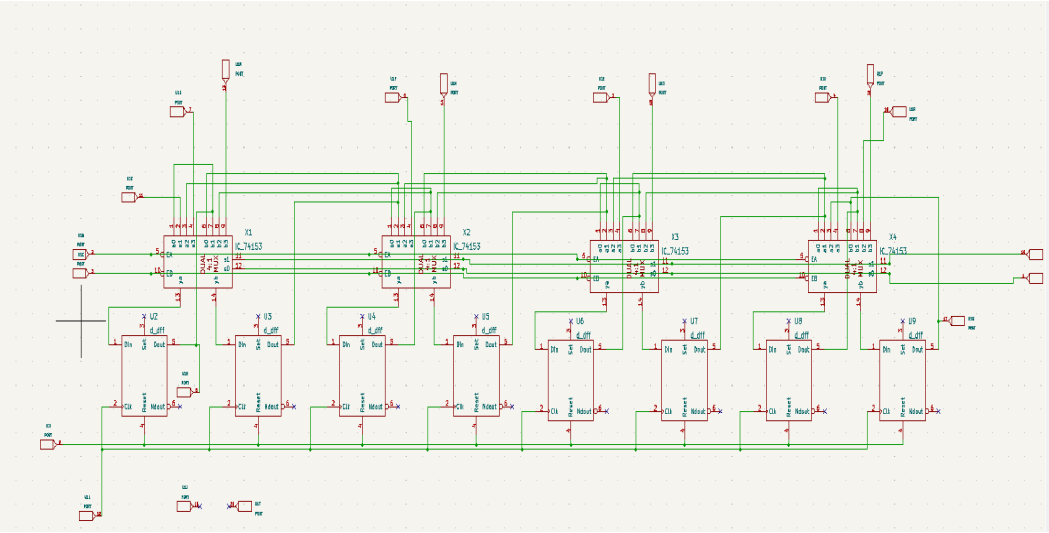

Figure 4.17: Subcircuit Schematic of SN74LS299

4.4.3 Test Circuit

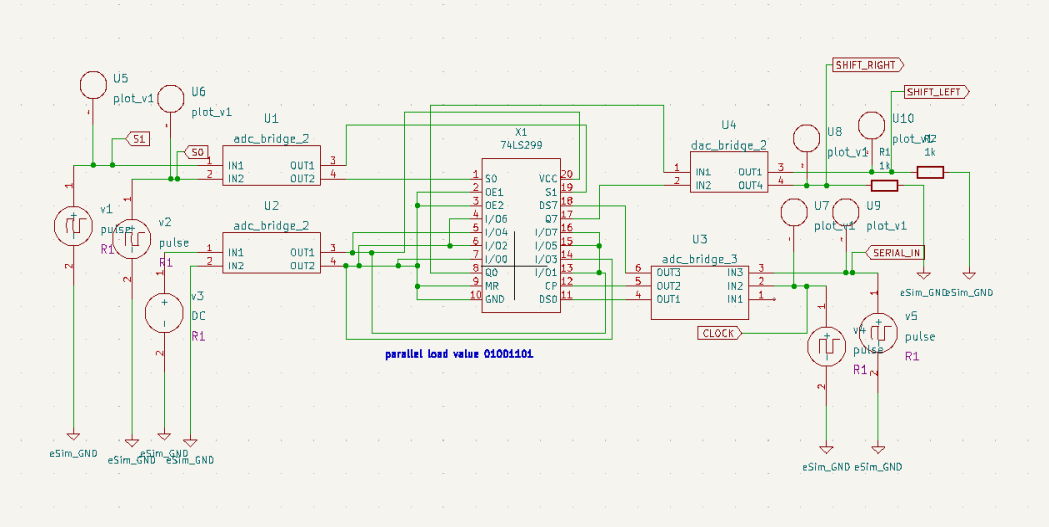

Figure 4.18: Test Circuit of SN74LS299 IC

4.4.4 Input Plots

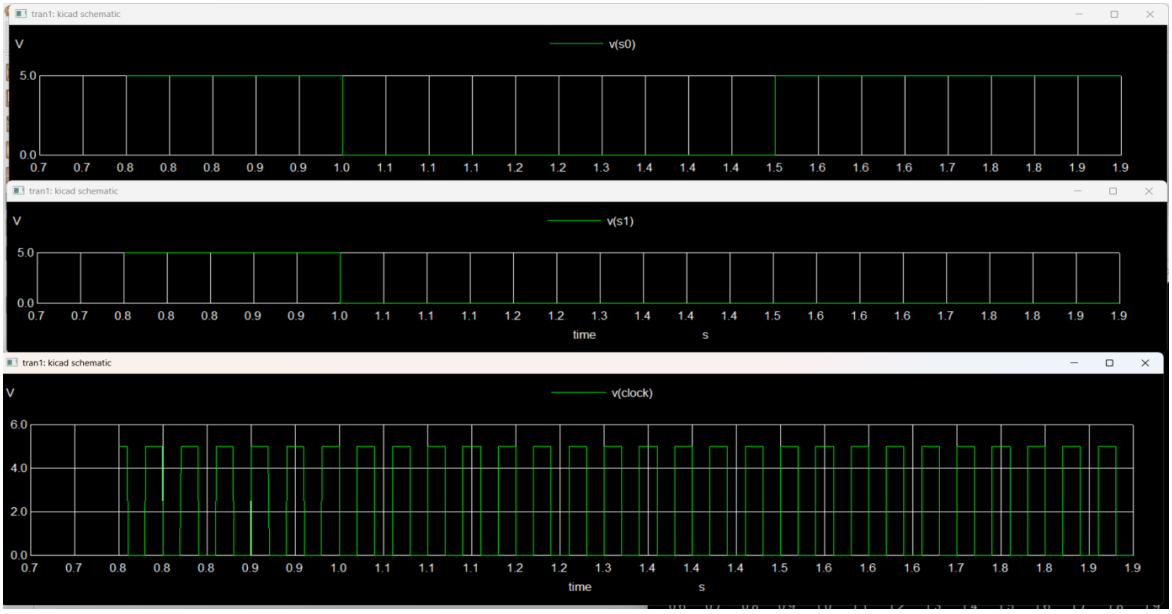

Figure 4.19: Input Voltage Waveform of SN74LS299

4.4.5 Output Plots

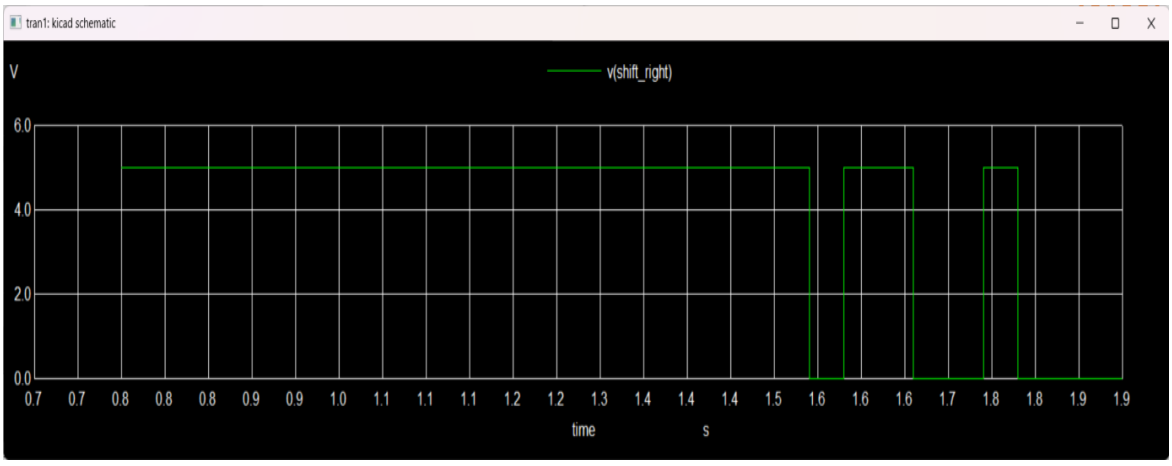

Figure 4.20: Output Voltage Waveform of SN74LS299

4.5 SN54LS290 - DECADE/BI-QUINARY COUNTER

The SN74LS290 is a monolithic decade counter IC that internally consists of four JK master– slave flip-flops and decoding logic to implement a divide-by-10 counting function, while also supporting an alternate bi-quinary (5–2) counting mode depending on how the A and B inputs are connected. It accepts input clock pulses on pin A and uses pin B to extend or modify the count sequence, with the QA output feeding back to B when full decade counting is required. The device includes asynchronous gated reset inputs (R01, R02, R91, R92) which allow it to be reset to a known state immediately, independent of the clock, ensuring predictable startup and stable sequence transitions. The counter outputs QA, QB, QC, and QD generate a binary-coded count that progresses from 0 to 9 in BCD mode, or through the programmed bi-quinary sequence depending on wiring. This IC is widely used in timing circuits, frequency division, digital clocks, event counting, and sequence generation applications, where its stable switching characteristics, reliable TTL compatibility, and ability to cascade with additional counters make it an effective building block in modular digital systems.

4.5.1 IC Layout

This figure represents the Pin Package Diagram of SN54LS290

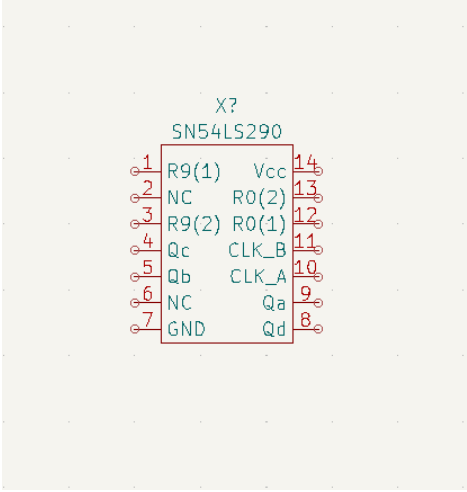

Figure 4.21: Pin diagram of SN54LS290

4.5.2 Subcircuit Schematic Diagram

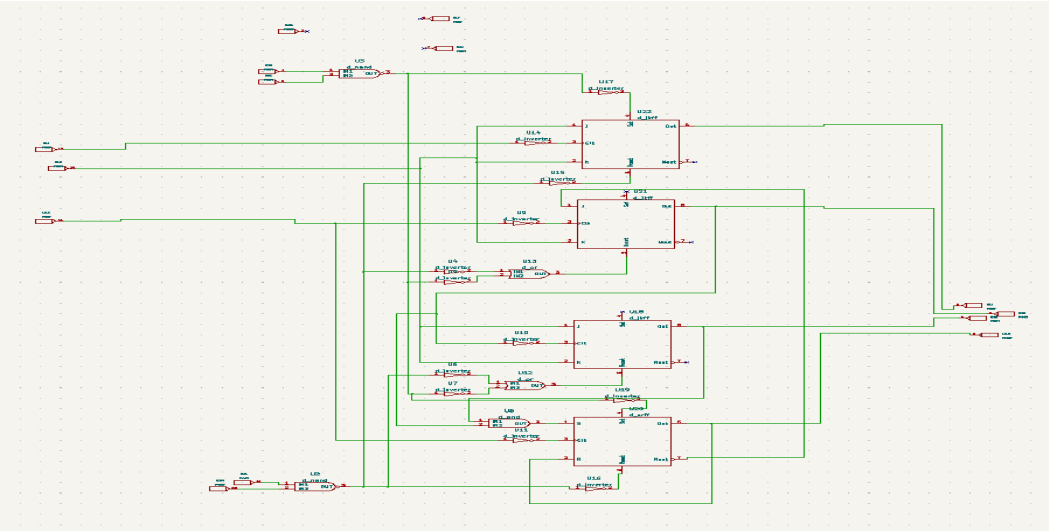

Figure 4.22: Subcircuit Schematic of SN54LS290

4.5.3 Test Circuit

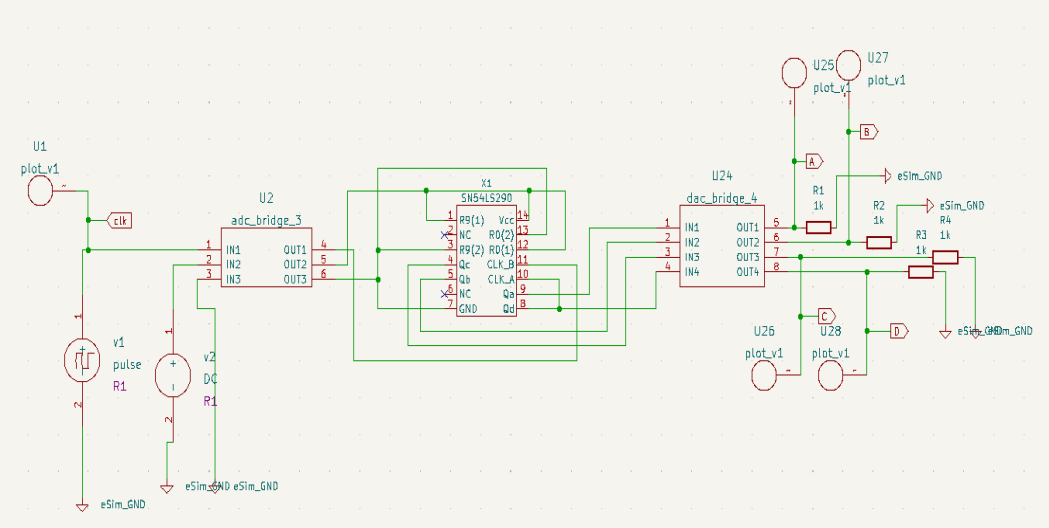

Figure 4.23: Test Circuit of SN54LS290 IC

4.5.4 Input Plots

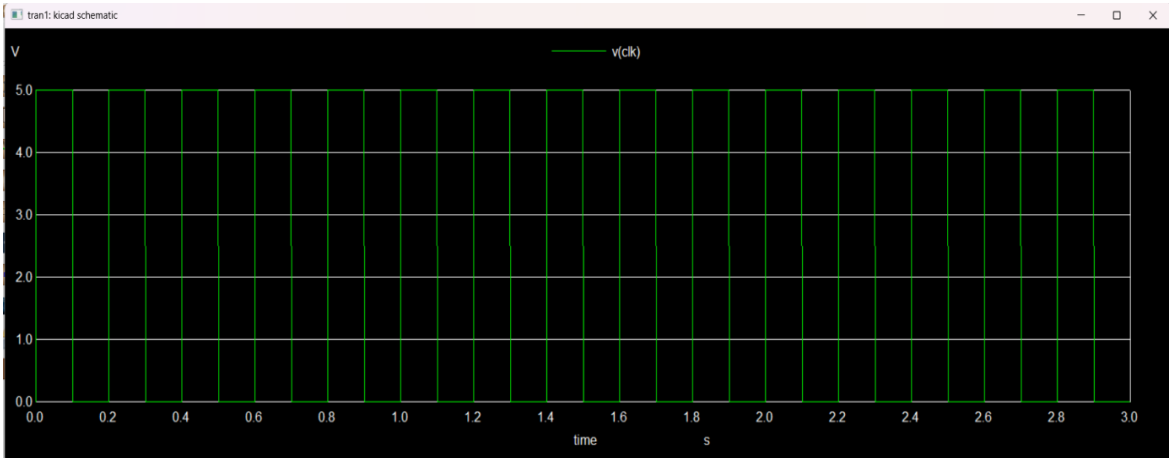

Figure 4.24: Input Voltage Waveform of SN54LS290

4.5.5 Output Plots

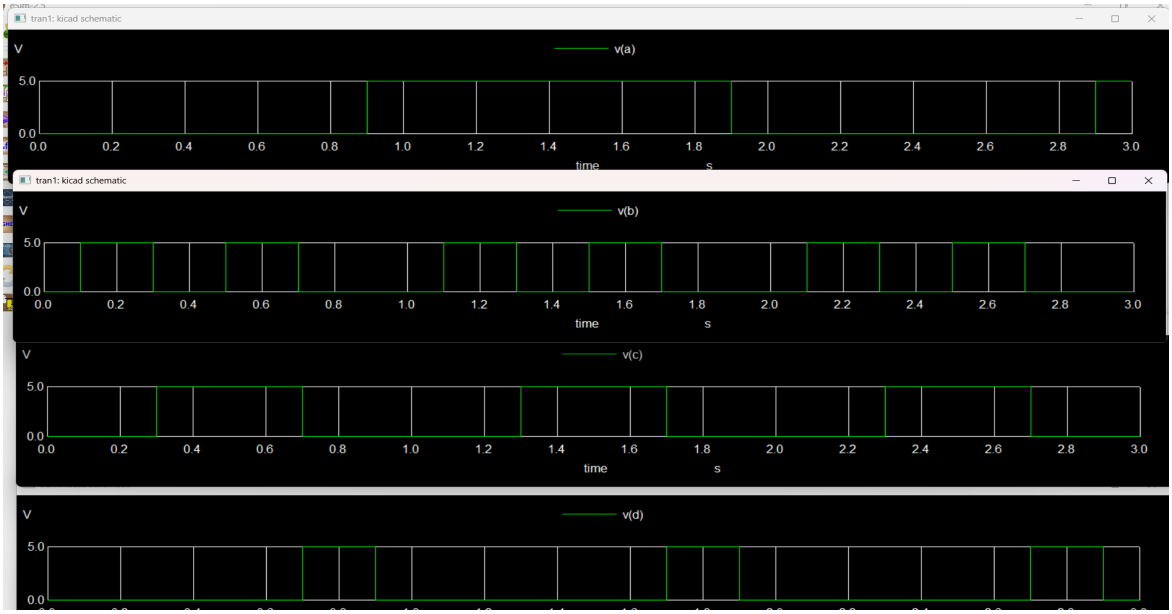

Figure 4.25: Output Voltage Waveform of SN54LS290

4.6 SN54LS293 - 4 BIT BINARY COUNTER

The SN74LS293 is a 4-bit binary counter IC that consists of four JK master–slave flip-flops arranged to generate a fully synchronous divide-by-16 counting sequence, with two separate clock inputs allowing independent divide-by-2 and divide-by-8 stages that combine to produce the complete 4-bit binary output. Input clocks applied at CKA increment QA and then ripple through to QB, QC, and QD based on the internal gating structure, while the second clock input CKB controls the higher-order three-bit section for flexible timing arrangements. The device includes gated asynchronous reset controls (R01, R02) that immediately clear all outputs to zero regardless of clock activity, ensuring proper initialization during power-up or control events. Its outputs (QA, QB, QC, QD) follow a binary progression from 0000 to 1111, making the LS293 suitable for frequency division, digital timing, event counting, sequence generation, and as a cascade element in larger counting chains for complex timing systems. With reliable TTL input/output compatibility, predictable switching delays, and the ability to easily cascade for higher-order counts, the LS293 provides robust performance in counters, timers, digital clocks, and control logic applications.

4.6.1 IC Layout

This figure represents the Pin Package Diagram of SN54LS293

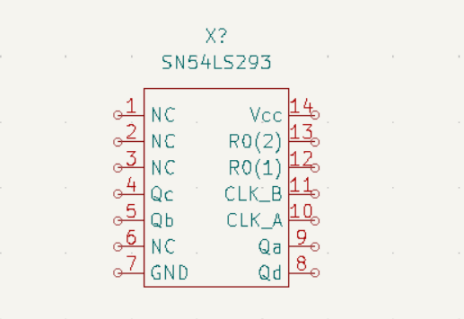

Figure 4.26: Pin diagram of SN54LS293

4.6.2 Subcircuit Schematic Diagram

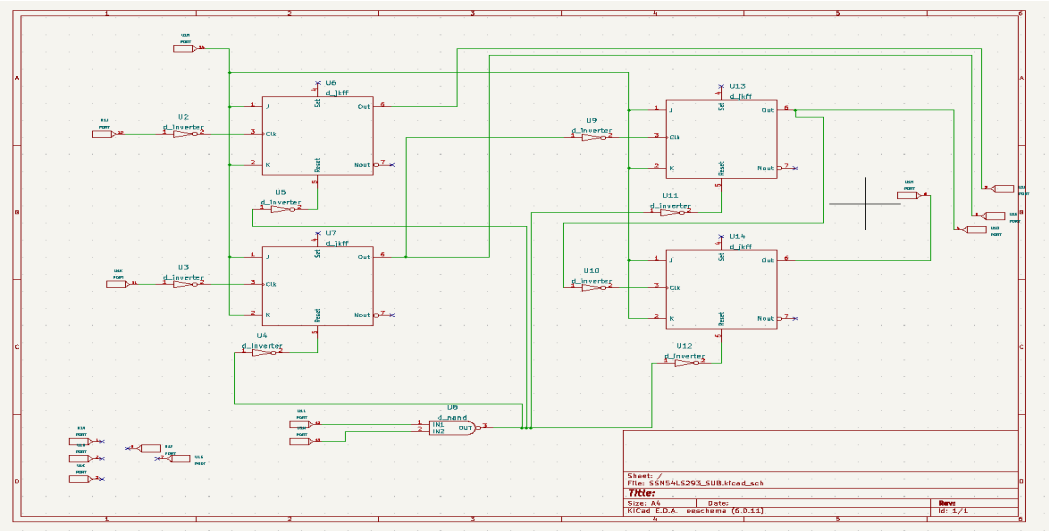

Figure 4.27: Subcircuit Schematic of SN54LS293

4.6.3 Test Circuit

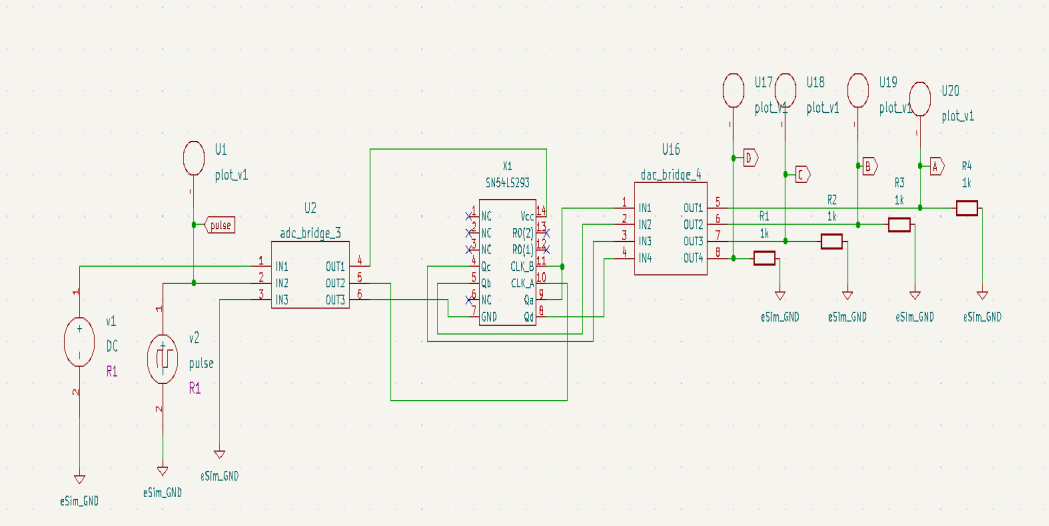

Figure 4.28: Test Circuit of SN54LS293 IC

4.6.4 Input Plots

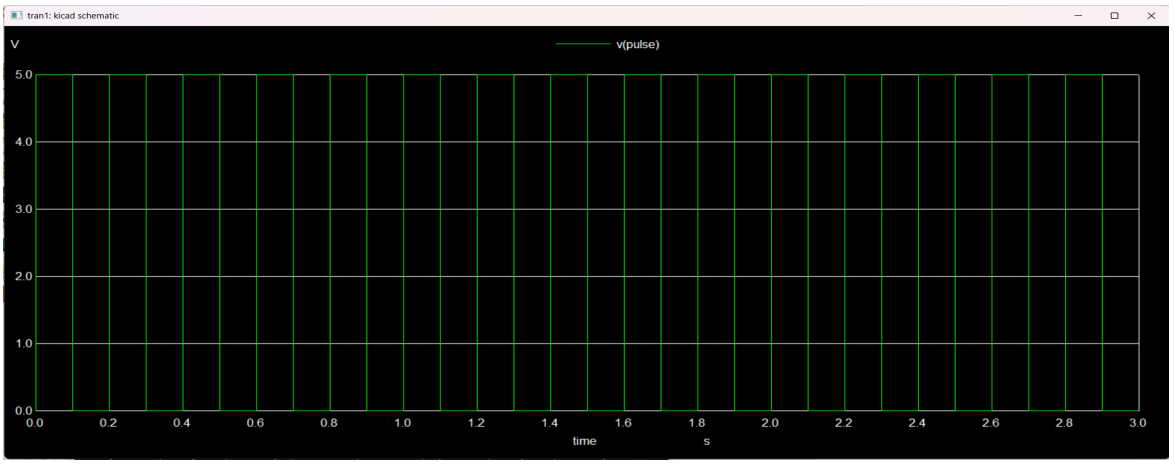

Figure 4.29: Input Voltage Waveform of SN54LS293

4.6.5 Output Plots

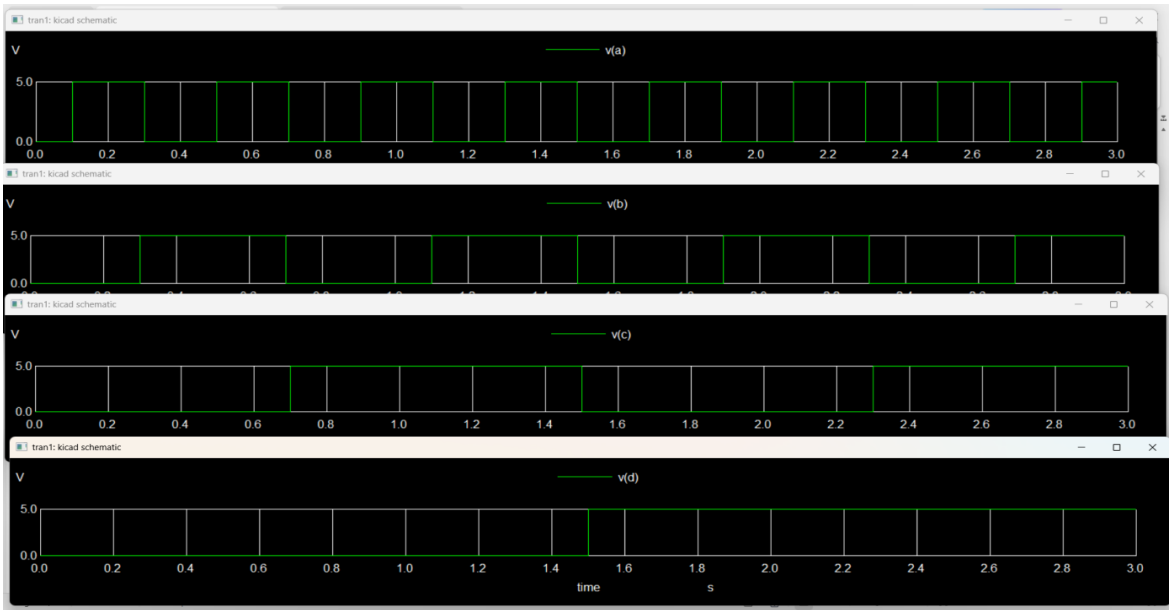

Figure 4.30: Output Voltage Waveform of SN54LS293

4.7 DS2004 - HIGH CURRENT DRIVERS

The shown circuit is a discrete implementation of a 7-channel high-current Darlington driver,functionally similar to the DS2004 device, built using pairs of NPN transistors configured in Darlington topology, with input resistors, base-bias resistors, and fly-back diodes for each channel. Each input signal passes through a 10.5 k resistor before driving the first NPN transistor, which then drives a second NPN to form a high-gain Darlington pair capable of sinking large currents at the output ports. The 7.2 k and 3.4 k resistors provide proper biasing to prevent leakage and ensure clean switching, while the series diodes connected from each output line to the supply rail act as inductive kickback clamps, protecting the transistors when driving solenoids, relays, or motors. The outputs are open-collector,meaning they can directly sink high loads and multiple channels can be paralleled when higher current capability is needed, while sharing a common ground return path. Overall, the circuit serves as an efficient interface between low-power logic-level inputs and high-power external loads, providing isolation, amplification, and protection exactly like a Darlington driver IC but implemented with discrete components for visibility and customization.

4.7.1 IC Layout

This figure represents the Pin Package Diagram of DS2004

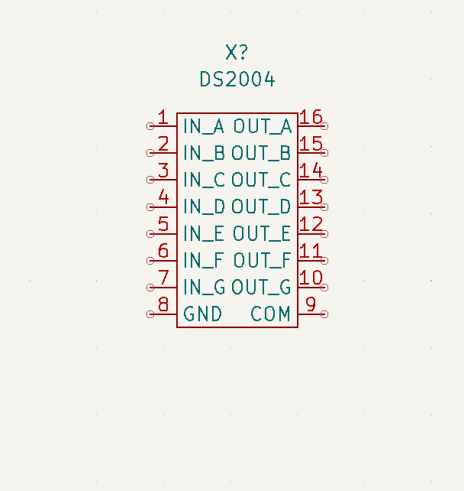

Figure 4.31: Pin diagram of DS2004

4.7.2 Subcircuit Schematic Diagram

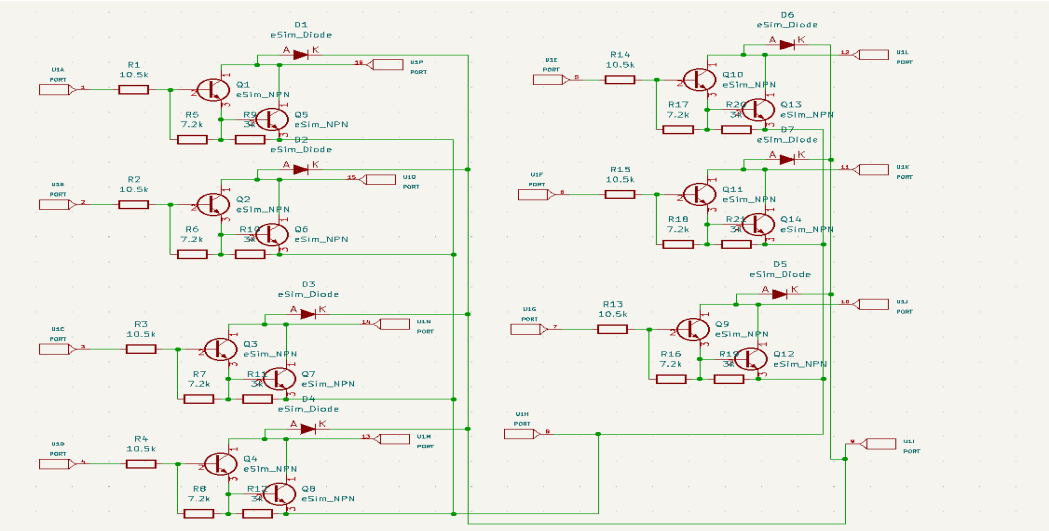

Figure 4.32: Subcircuit Schematic of DS2004

4.7.3 Test Circuit

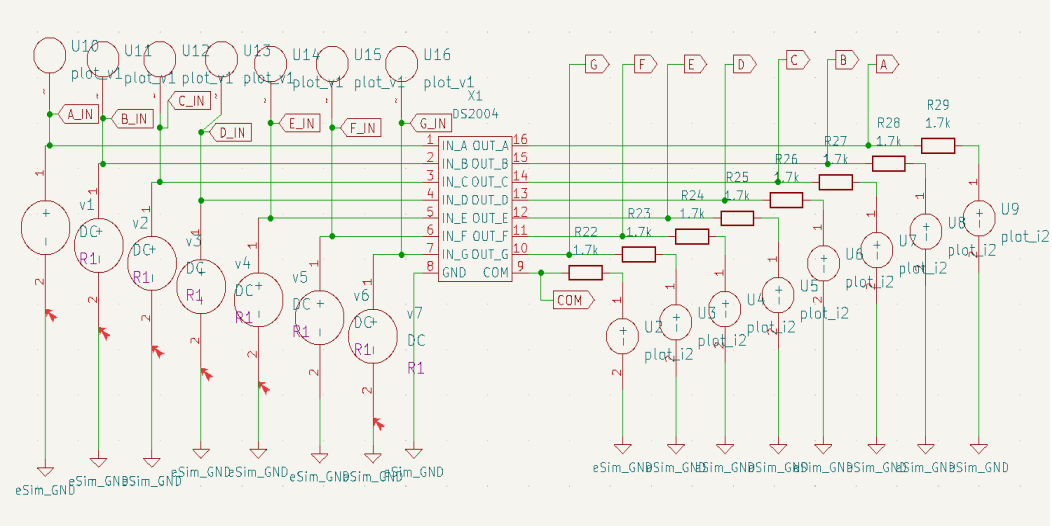

Figure 4.33: Test Circuit of DS2004 IC

4.7.4 Input Plots

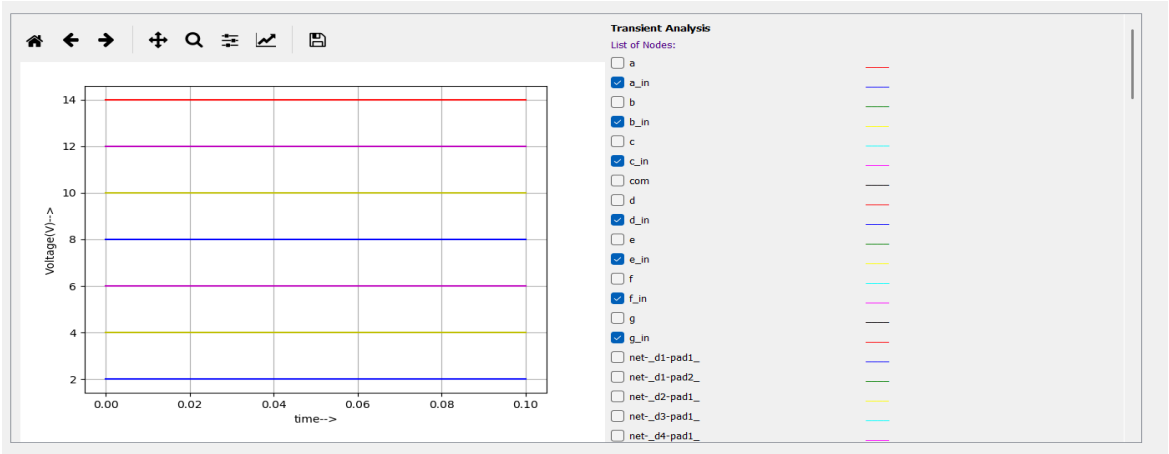

Figure 4.34: Input Voltage Waveform of DS2004

4.7.5 Output Plots

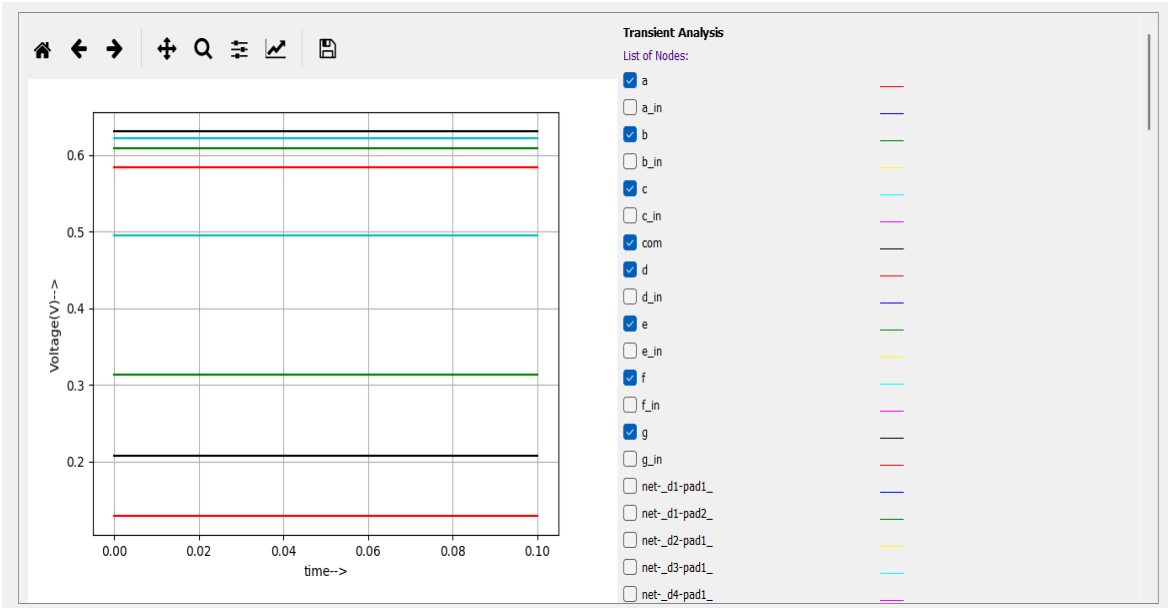

Figure 4.35: Output Voltage Waveform of DS2004

4.8 HEF4539 - DUAL 4 INPUT MULTIPLEXER

The HEF4539B is a dual 4-input multiplexer IC that integrates two independent multiplexers sharing common select logic, each offering four data inputs (I0–I3), an active-LOW enable pin,and a single output, enabling efficient routing of digital signals in medium-scale integration applications. When the enable input is LOW, the two select lines S0 and S1 determine which of the four input channels is passed to the corresponding output, allowing flexible data selection from multiple sources. When the enable pin is HIGH, the output is forced LOW regardless of the input or select conditions, providing a clean and predictable disable state for both multiplexer sections. The device supports standard CMOS logic levels, making it ideal for digital switching, signal routing, data steering, and building modular control logic circuits. Its symmetrical internal design ensures consistent propagation and stable logic behavior, allowing the HEF4539B to function reliably in timing, control, communication, and selection systems where multiple signal paths must be compactly managed.

4.8.1 IC Layout

This figure represents the Pin Package Diagram of HEF4539

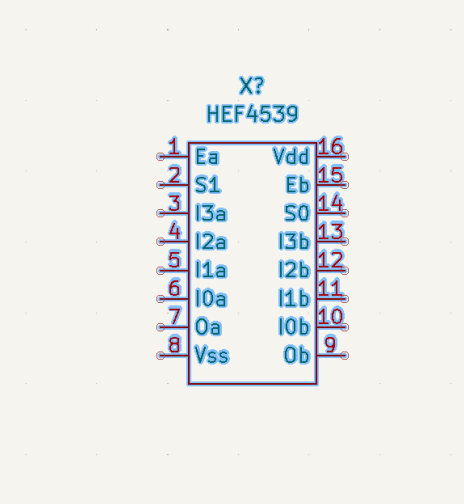

Figure 4.36: Pin diagram of HEF4539

4.8.2 Subcircuit Schematic Diagram

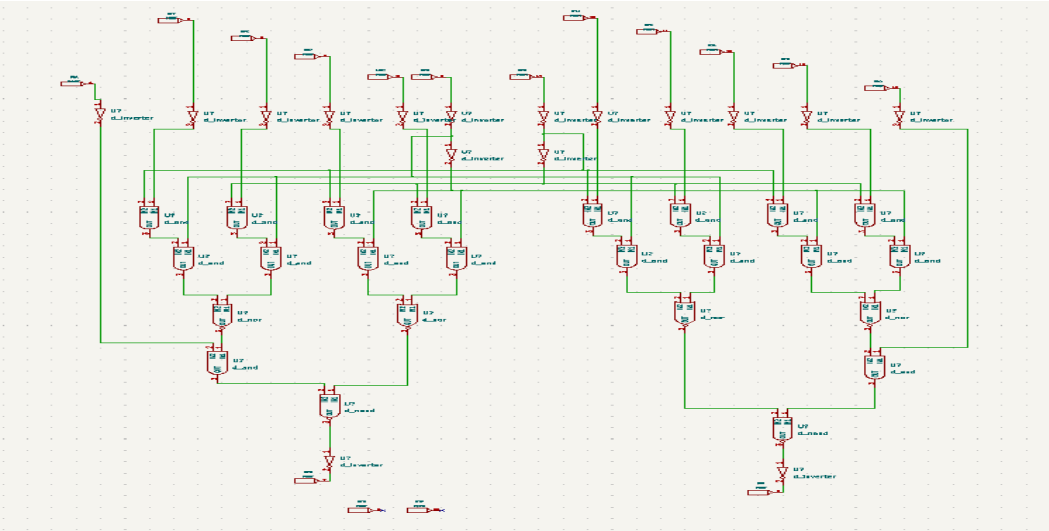

Figure 4.37: Subcircuit Schematic of HEF4539

4.8.3 Test Circuit

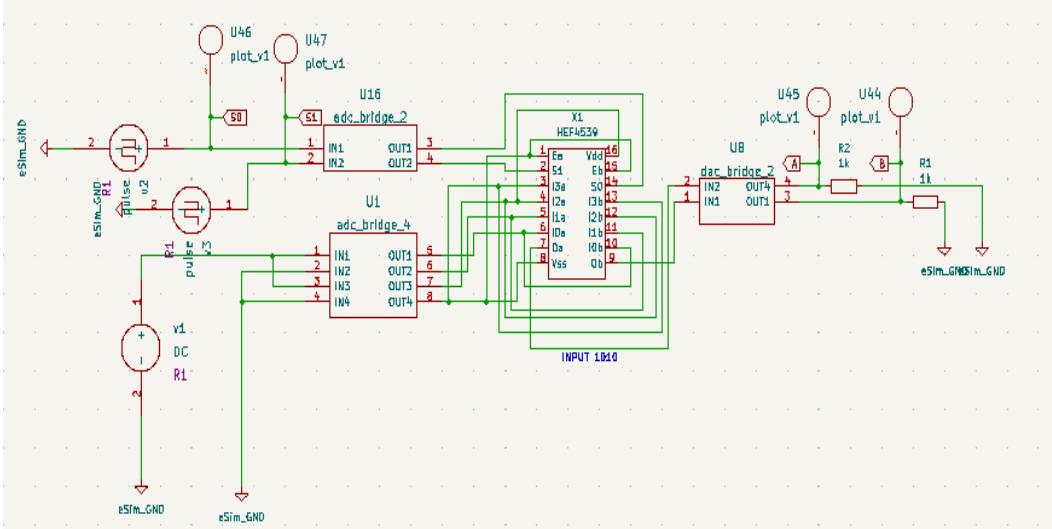

Figure 4.38: Test Circuit of HEF4539 IC

4.8.4 Input Plots

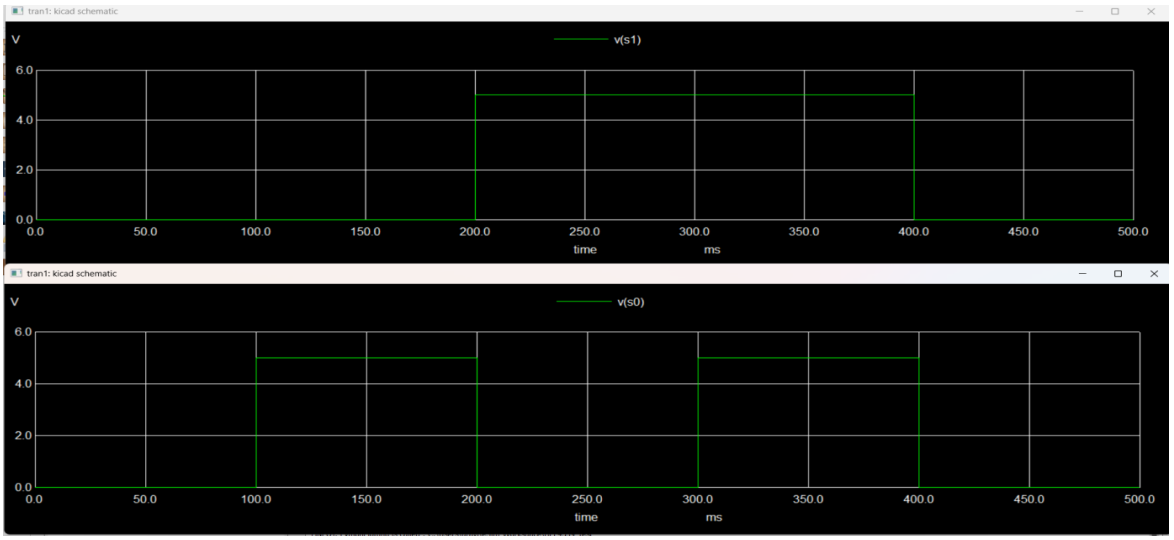

Figure 4.39: Input Voltage Waveform of HEF4539

4.8.5 Output Plots

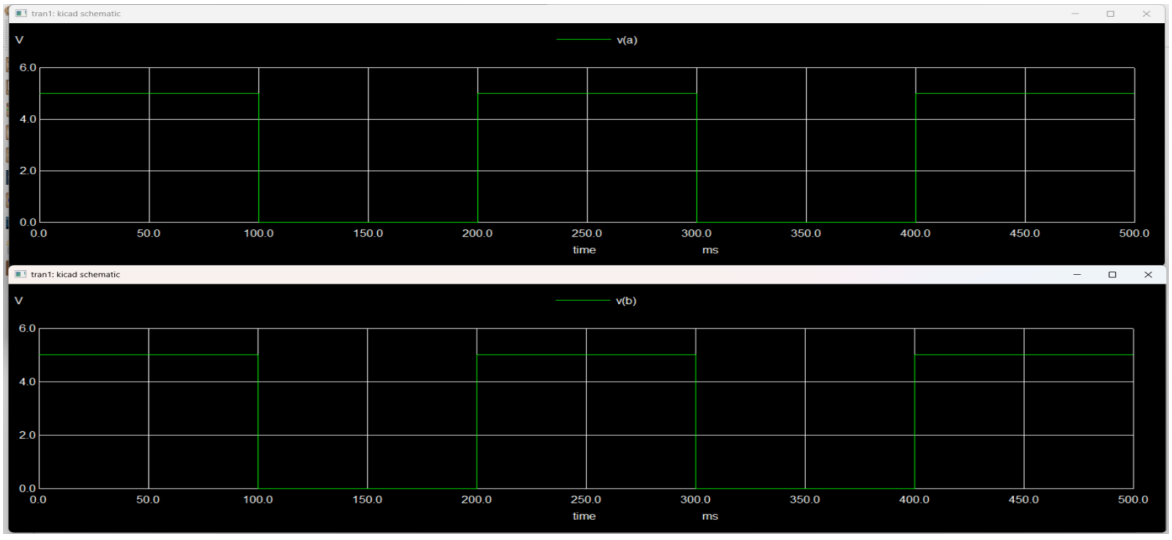

Figure 4.40: Output Voltage Waveform of LM341

4.9 CD40107B - DUAL 2 INPUT NAND BUFFER

The CD40107B is a dual 2-input NAND buffer/driver that integrates two independent high-current NAND stages with open-drain N-channel transistor outputs, providing wired-OR capability and allowing it to directly sink large currents up to 136 mA typical at VDD = 10 V,making it suitable for driving relays, lamps, LED arrays, and other heavy loads. Each section accepts two logic inputs and produces an inverted output, but instead of a standard CMOS push-pull stage, it uses a single N-channel transistor output that requires an external pull-up resistor, enabling flexible interfacing across voltage domains. The device maintains stable operation over a wide supply range and supports TTL/CMOS compatibility, with propagation delays and switching characteristics designed for robust buffer/driver applications. Its open-drain structure also allows multiple outputs to be tied together for wired-logic functions without additional components, making the CD40107B an effective interface element where high current drive, level shifting, or logical AND-wired OR operations are required.

4.9.1 IC Layout

This figure represents the Pin Package Diagram of CD40107B

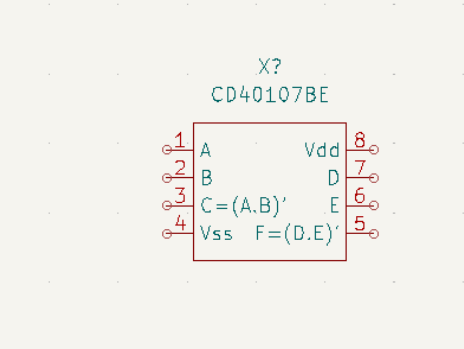

Figure 4.41: Pin diagram of CD40107B

4.9.2 Subcircuit Schematic Diagram

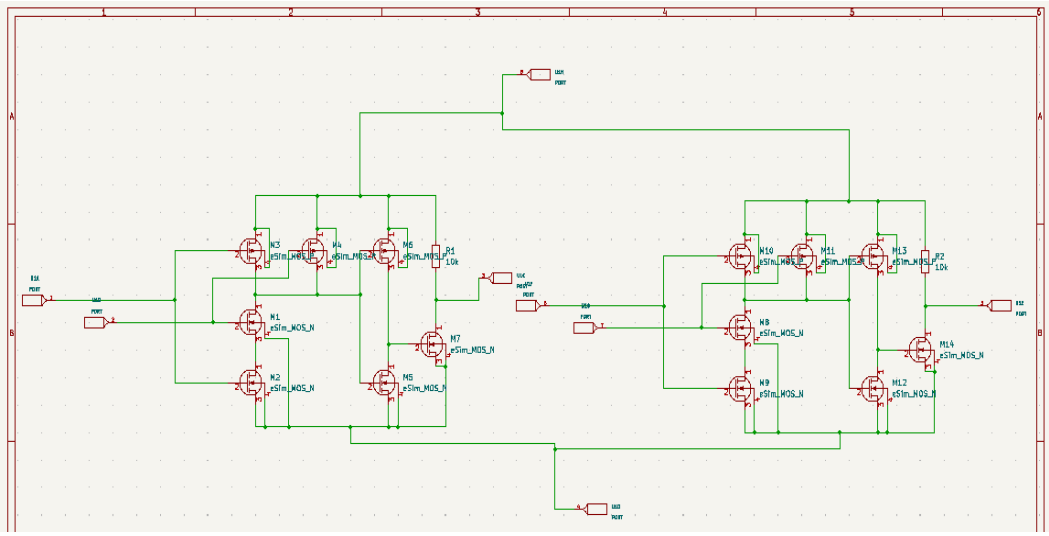

Figure 4.42: Subcircuit Schematic of CD40107B

4.9.3 Test Circuit

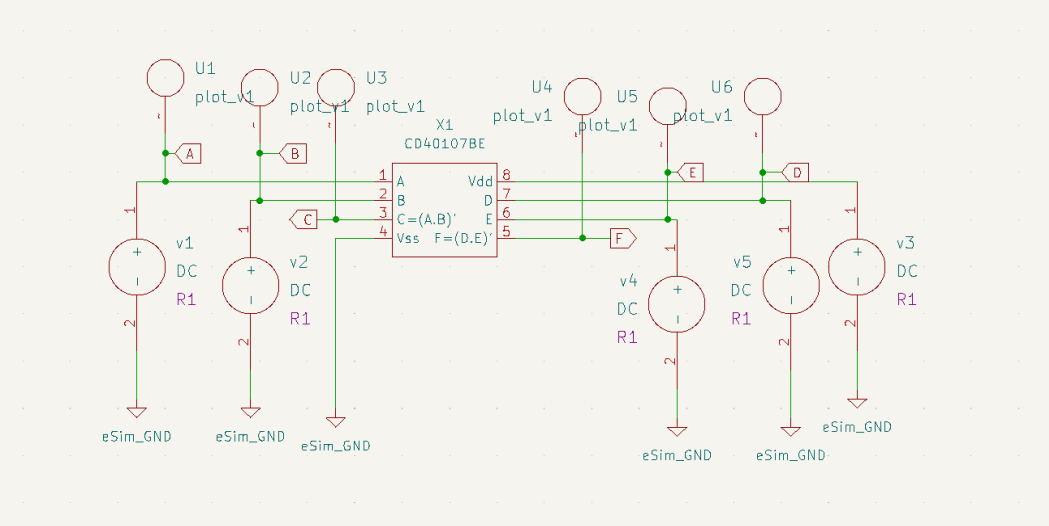

Figure 4.43: Test Circuit of CD40107B IC

4.9.4 Input Plots

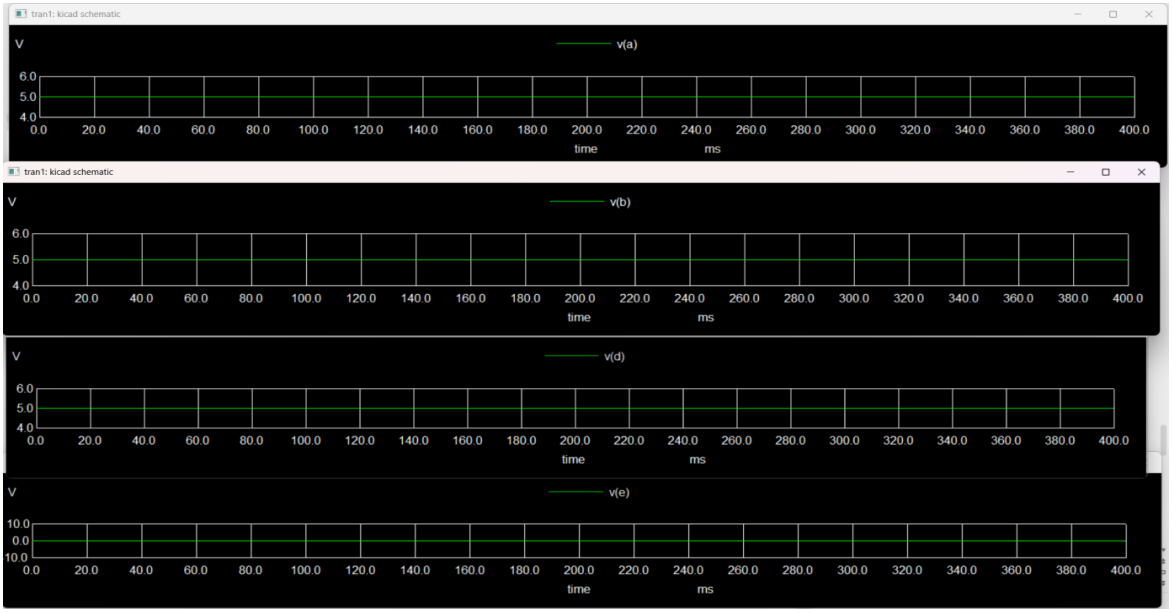

Figure 4.44: Input Voltage Waveform of CD40107B

4.9.5 Output Plots

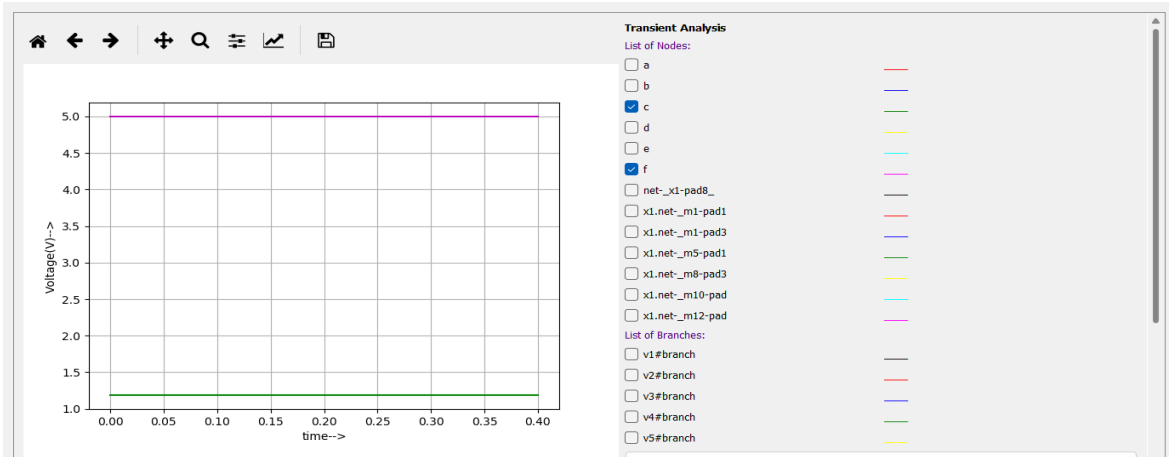

Figure 4.45: Output Voltage Waveform of CD40107B

4.10 SN54LS374 - OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

The SN74LS374 is an octal edge-triggered D-type flip-flop register featuring eight parallel inputs, eight 3-state outputs, and a common clock and output-control pin, designed for direct interfacing to bus-organized digital systems. Data present at the D inputs is transferred to the Q outputs only on the positive edge of the clock, ensuring precise and synchronous data capture, while the separate output-control input allows the eight outputs to be placed in a high-impedance state independently of the internal storage operation. This enables the device to act as a bidirectional bus driver or output buffer without loading the bus when inactive. Its buffered and hysteresis-enhanced control inputs provide improved noise immunity, and its ability to drive highly capacitive or low-impedance loads makes it suitable for use as an I/O latch, register, or data-holding element in microprocessor-based designs requiring stable, clock-synchronized 8-bit data transfer.

4.10.1 IC Layout

This figure represents the Pin Package Diagram of SN54LS374

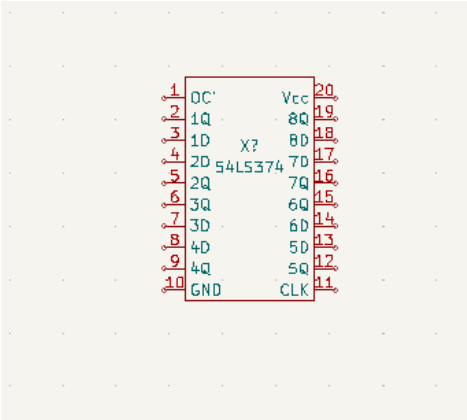

Figure 4.46: Pin diagram of SN54LS374

4.10.2 Subcircuit Schematic Diagram

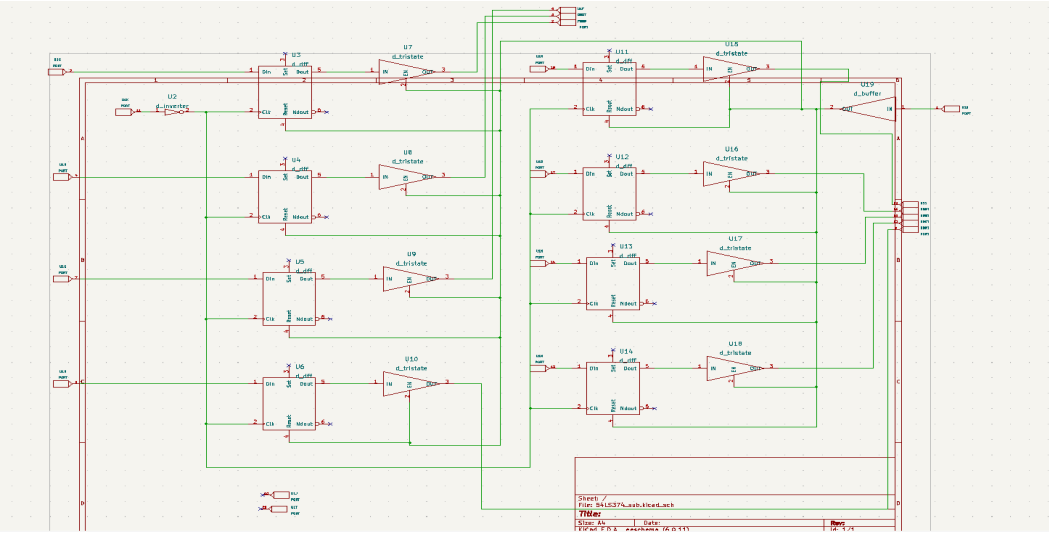

Figure 4.47: Subcircuit Schematic of SN54LS374

4.10.3 Test Circuit

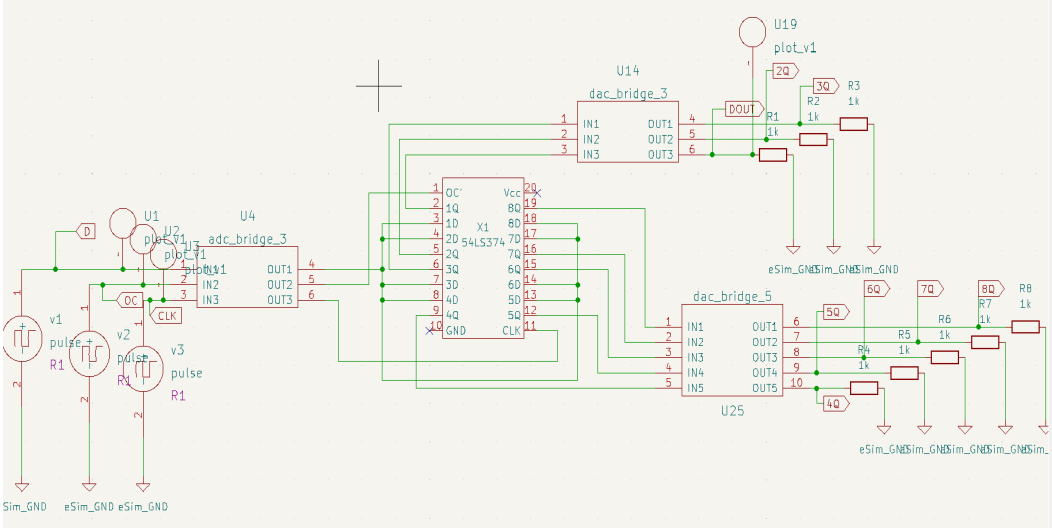

Figure 4.48: Test Circuit of SN54LS374B IC

4.10.4 Input Plots

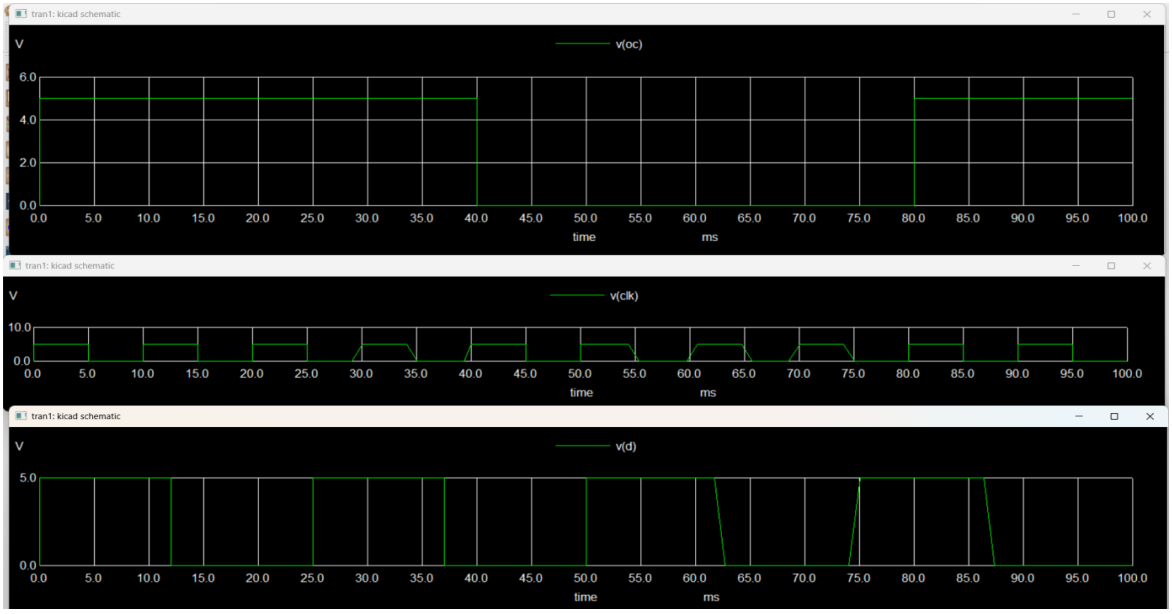

Figure 4.49: Input Voltage Waveform of SN54LS374

4.10.5 Output Plots

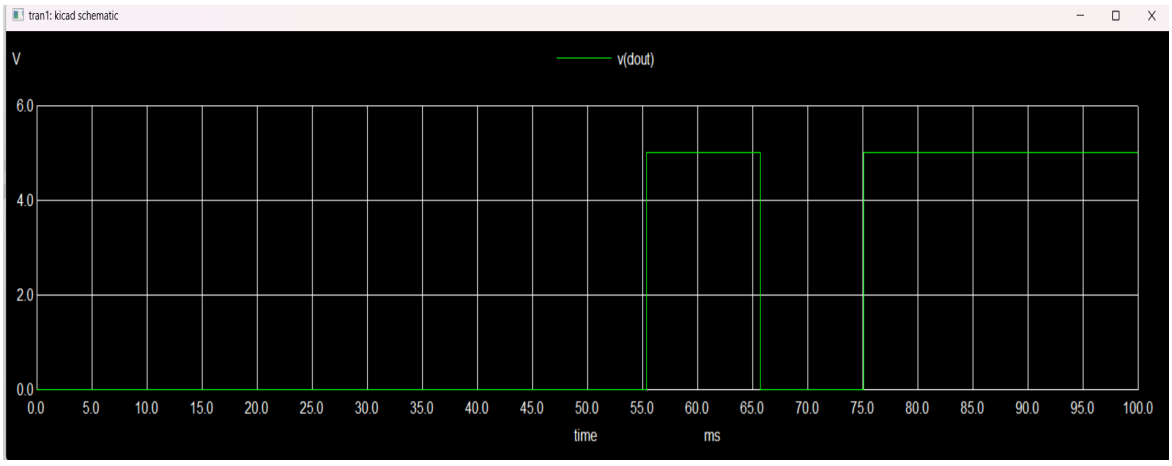

Figure 4.50: Output Voltage Waveform of SN54LS374

4.11 MC14040B - 12 BIT BINARY COUNTER

The MC14040B is a 12-stage ripple-carry binary counter built using CMOS P-channel and N-channel enhancement devices, featuring a built-in input wave-shaping circuit that ensures reliable triggering on the negative-going edge of the clock pulse. It provides 12 binary-divided outputs (Q1 to Q12), each representing successive divide-by-2 stages, allowing frequency division from 2 up to 4096 with a single chip, and includes a common asynchronous reset input that forces all outputs LOW regardless of clock activity. Operating over a wide supply range of 3 V to 18 V, the counter supports fully static operation and includes input diode protection, enabling compatibility with both CMOS and low-power TTL logic families. With low quiescent current, high noise immunity, and the ability to directly drive two low-power TTL loads, the MC14040B is well suited for timing chains, frequency synthesizers, time-delay generators, event counters, and clock-division systems where stable and predictable binary sequencing is required.

4.11.1 IC Layout

This figure represents the Pin Package Diagram of MC14040B

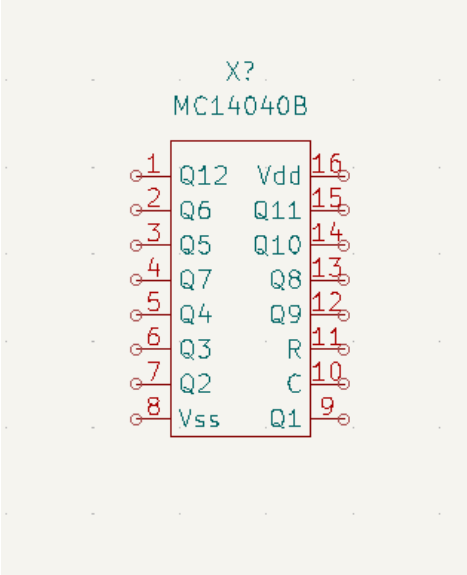

Figure 4.51: Pin diagram of MC14040B

4.11.2 Subcircuit Schematic Diagram

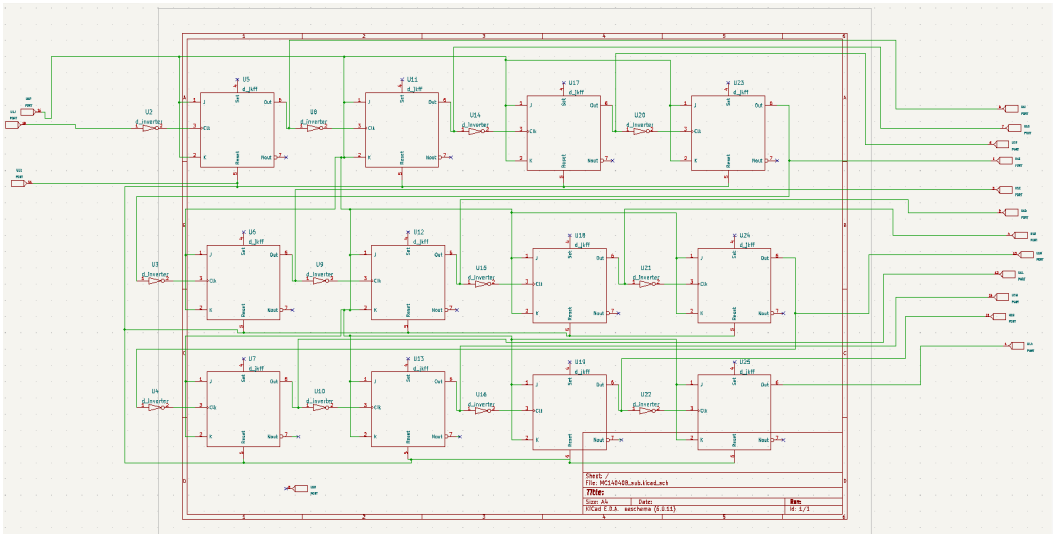

Figure 4.52: Subcircuit Schematic of MC14040B

4.11.3 Test Circuit

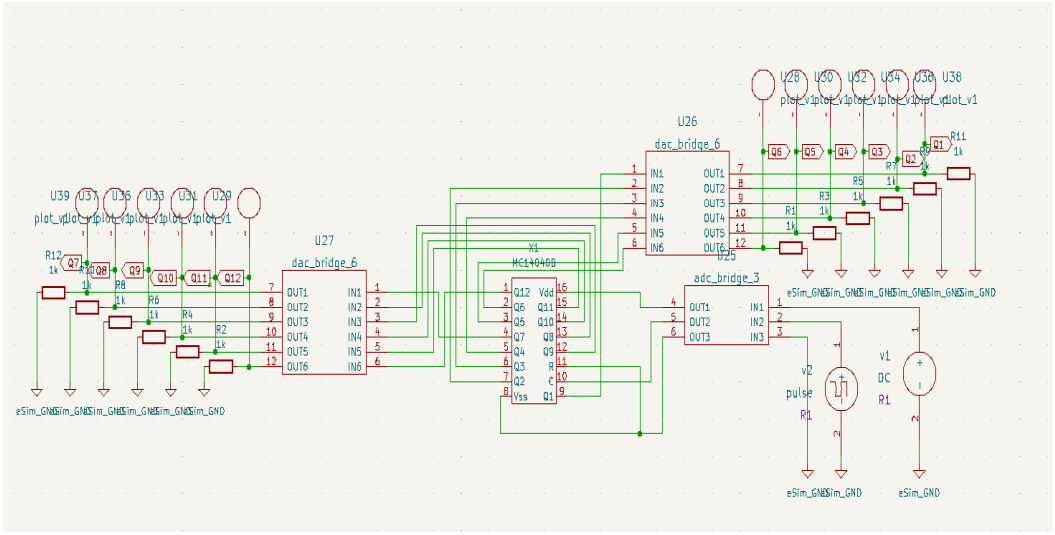

Figure 4.53: Test Circuit of MC14040B IC

4.11.4 Input Plots

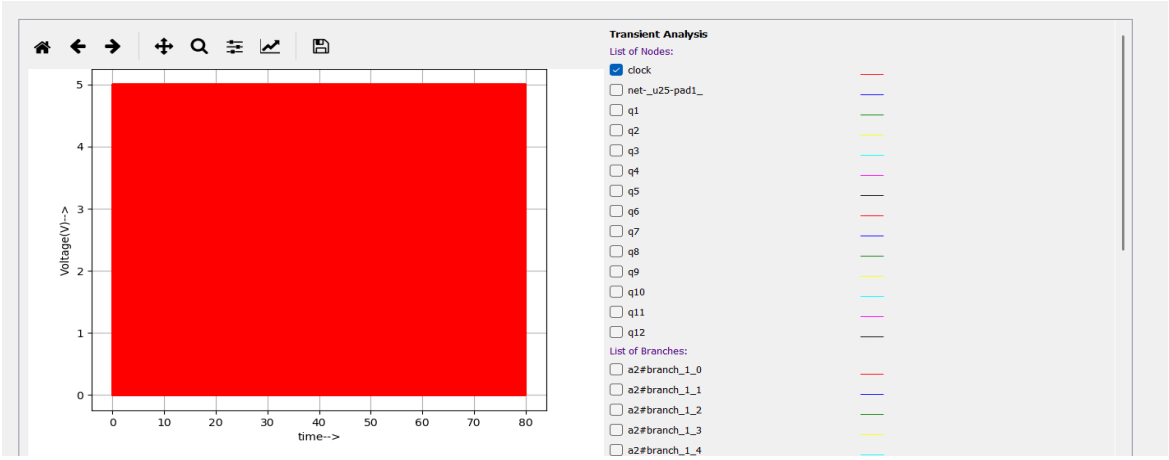

Figure 4.54: Input Voltage Waveform of MC14040B

4.11.5 Output Plots

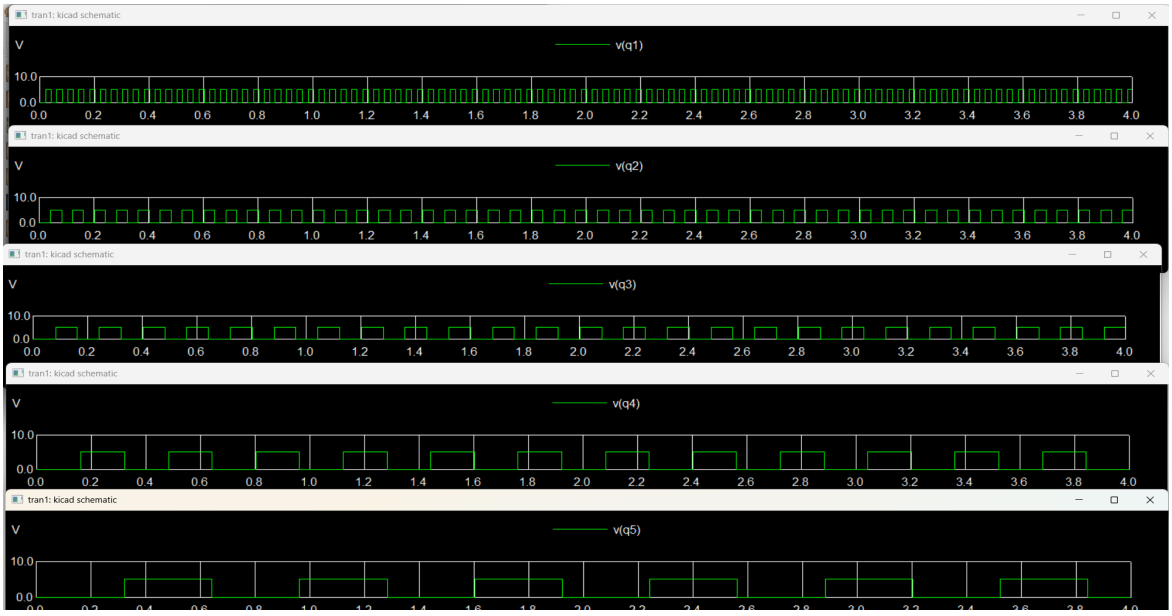

Figure 4.55: Output Voltage Waveform of MC14040B

Chapter 5

Failed Circuits

5.1 Overview

In this section, we discuss circuits that did not perform as expected during testing.Understanding the reasons for these failures helps in diagnosing issues and improving circuit design. Each failed circuit is analyzed to identify the potential causes of failure and to suggest corrective measures.

5.2 Failed Circuit 1: BA10339 IC

5.2.1 Circuit Diagram

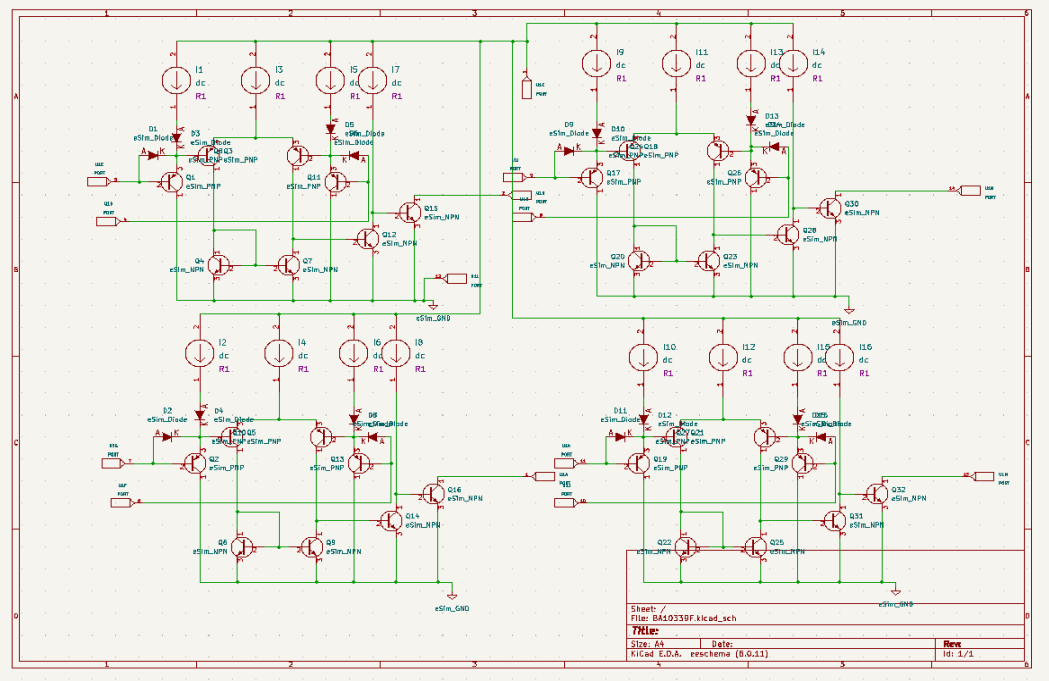

Figure 5.1: Subcircuit Schematic diagram of the BA10339 IC

5.2.2 Test Circuit

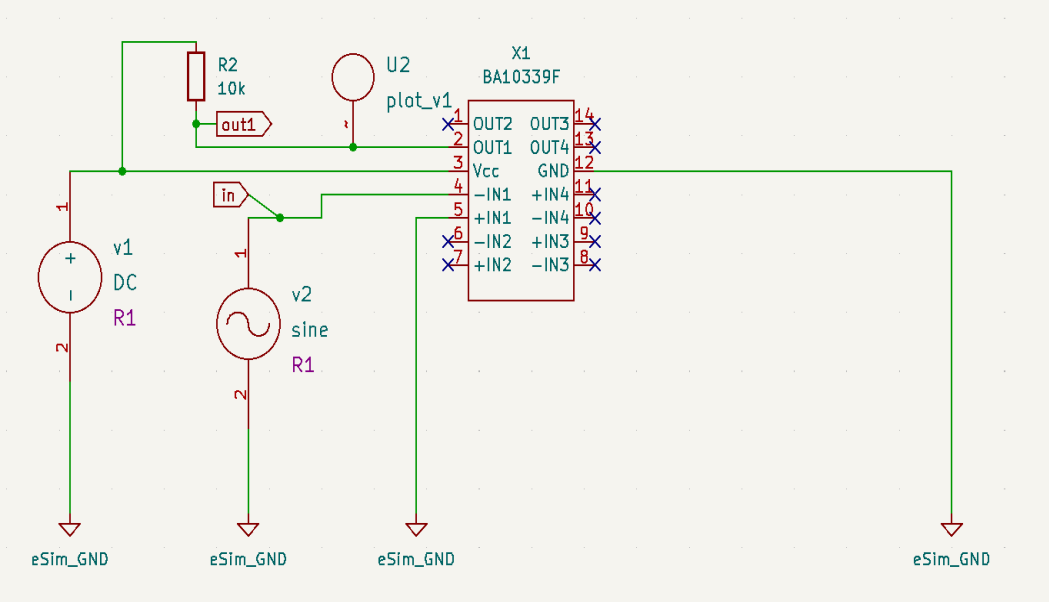

Figure 5.2: Test circuit of the BA10339 IC

5.2.3 Issue Description

The BA10339 quad comparator exhibits several operational issues primarily due to improper biasing across its input and output stages. The most common problem stems from improper input biasing where differential input pairs lack proper common-mode biasing within the specified 0 to (Vcc-1.5V) range, causing outputs to remain stuck in saturation and fail to respond to input changes. Reference voltage biasing errors on the inverting (-) inputs shift the comparison threshold outside the signal swing range, preventing correct switching behavior.Output stage biasing issues arise from missing or incorrect pull-up resistors on the open-collector outputs, resulting in undefined logic levels instead of proper high/low states. Supply voltage biasing problems occur when Vcc falls outside the 3V-36V operating range,destabilizing internal reference circuits essential for comparator functionality. Finally, input overbiasing beyond the common-mode limit triggers phase reversal in the internal transistor differential pairs.

5.3 Failed Circuit 2: CD4095 IC

5.3.1 Circuit Diagram

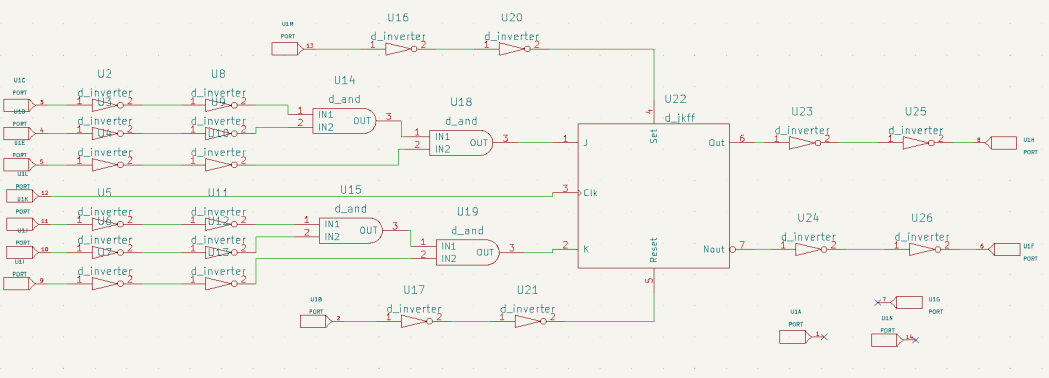

Figure 5.3: Subcircuit Schematic diagram of the CD4095 IC

5.3.2 Test Circuit

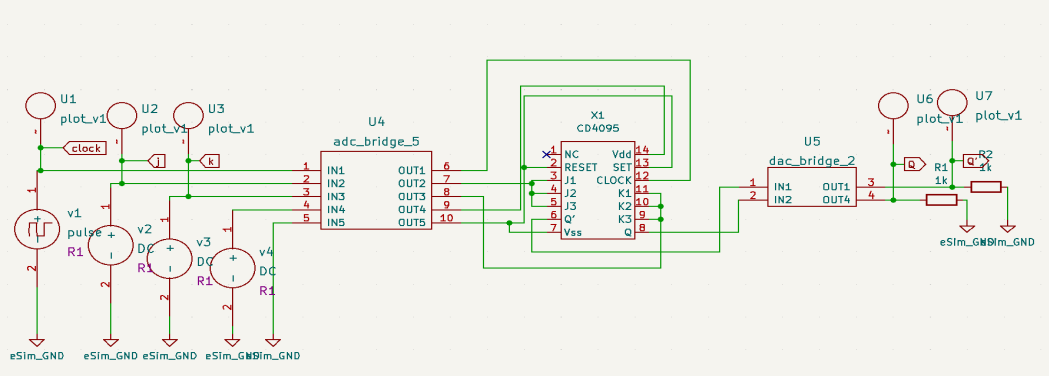

Figure 5.4: Test Circuit of the CD4095 IC

5.3.3 Issue Description

The simulation failure of the KiCad schematic in eSim occurs due to malformed XSPICE digital model parameter expansion where two .model statements on original lines 8 and 19 contain unmatched "Closing not found" braces, causing ngspice's numparam processor to generate invalid placeholder model names like numparm. This results in 66 copies with 131 evaluations but 2 critical errors that prevent proper model instantiation.When the user answers "y" to bypass numparam expansion errors, ngspice still cannot locate the undefined model definition for analog instance a2, leading to an immediate MIF-ERROR and simulation interruption. The absence of PSPICE compatibility mode exacerbates the parameter parsing issue, but the core problem remains the syntactically broken digital gate/flip-flop model definitions that fail during the initial netlist preprocessing stage.

Chapter 6

Conclusion

In conclusion, the studied device plays a vital role as a fundamental building block in digital and electronic systems by providing reliable, efficient, and predictable operation under a wide range of conditions. Its functional characteristics—such as stable logic behavior, low power consumption, compatibility with standard logic levels, and dependable switching performance—enable it to integrate seamlessly into larger circuits. Whether used for data processing, control, timing, or driving applications, the device consistently supports system-level reliability and simplifies design requirements. Overall, its architecture, electrical specifications, and functional versatility make it a robust choice for educational experiments,prototyping, and industrial-level electronic designs.

Looking ahead, the functionality of such devices can be extended by combining them with microcontrollers, programmable logic devices, or sensor interfaces to create more intelligent and automated systems. With advancements in embedded technology and IoT, these components can be integrated into smart applications requiring improved accuracy, real-time monitoring, and automated decision-making. Further development may include cascading multiple units for higher functionality, optimizing power consumption for battery-based designs, or integrating additional protection, filtering, and signal-conditioning circuits for enhanced robustness. As technology evolves, these devices will continue to remain relevant as dependable elements in timing, control, interfacing, and signal-processing applications.

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[6] URL:https://www.ti.com/

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