Assignment : 01A Gate Level Modeling

- Half Adder (using xor and and primitives).
- Full Adder (using two Half Adders + OR gate).
- 4-bit Ripple Carry Adder (cascading Full Adders).
- 4:1 MUX (using only NAND gates).
- 1:4 DEMUX (gate-level)
- 2:4 Decoder (using only NAND gates)
- **2-to-1 Multiplexer (Tri-State Style) ,** Use **two bufif gates** to select between inputs I0 and I1 with control S. Ensure only one path is active at a time.