Assignment-03: Structural Modelling

- Design 4:1 using 2:1 multiplexer

- Design 8:1 using 2:1 multiplexer

- Design 1:2 demultiplexer,

- Design 1:8 demux using 1:2 demux

- Design 5:1 Mux using 2:1 multiplexer using structural design

- Design Adder cum Subtractor using structural design (4-bit)
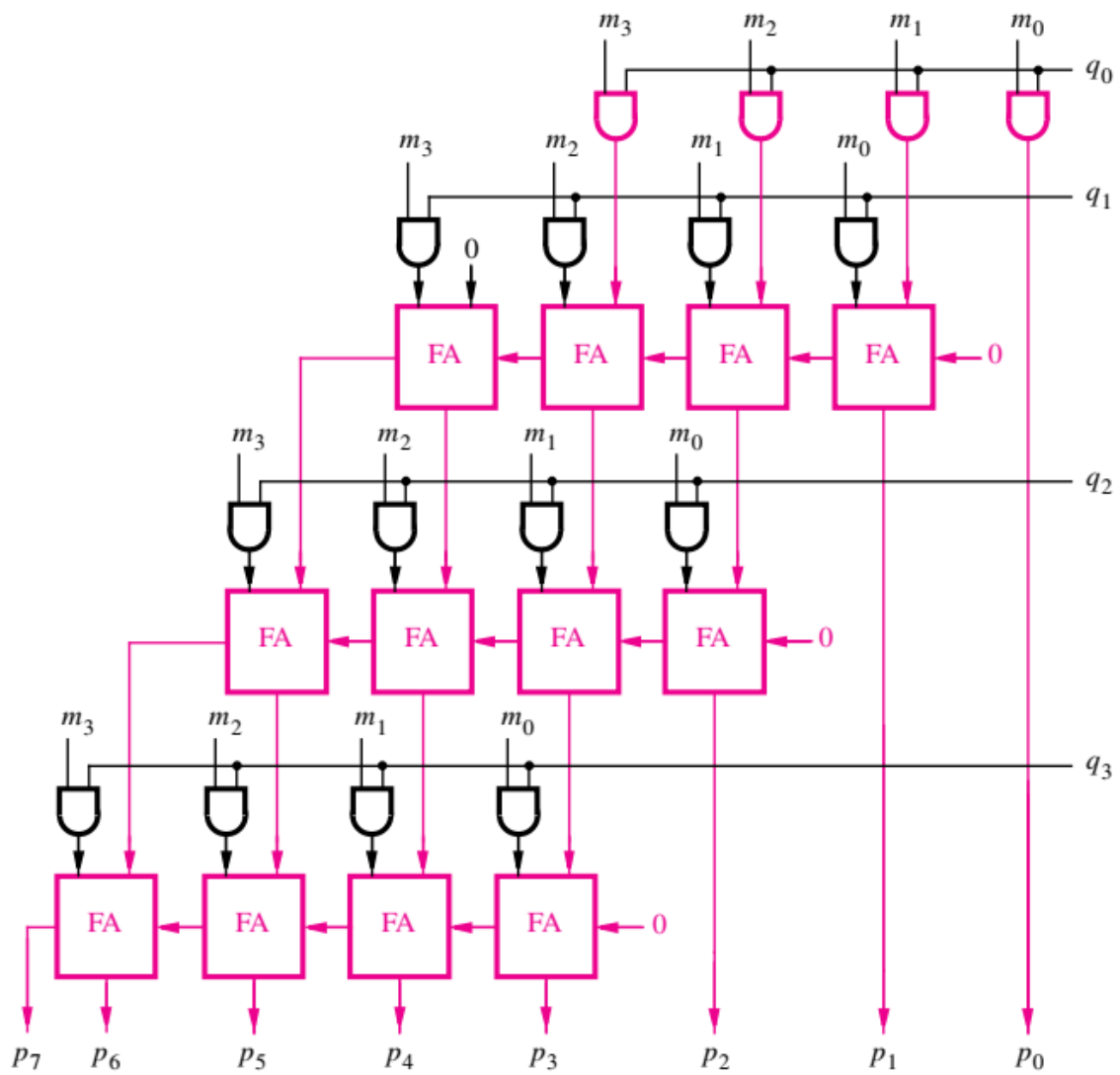
- Design 4-bit Multiplier circuits as below

(a) Multiplication by hand

(b) Using multiple adders

(c) Hardware implementation

Hardware implementation of four-bit multiplier

Write Verilog description for following BCD adder circuit and verify the results
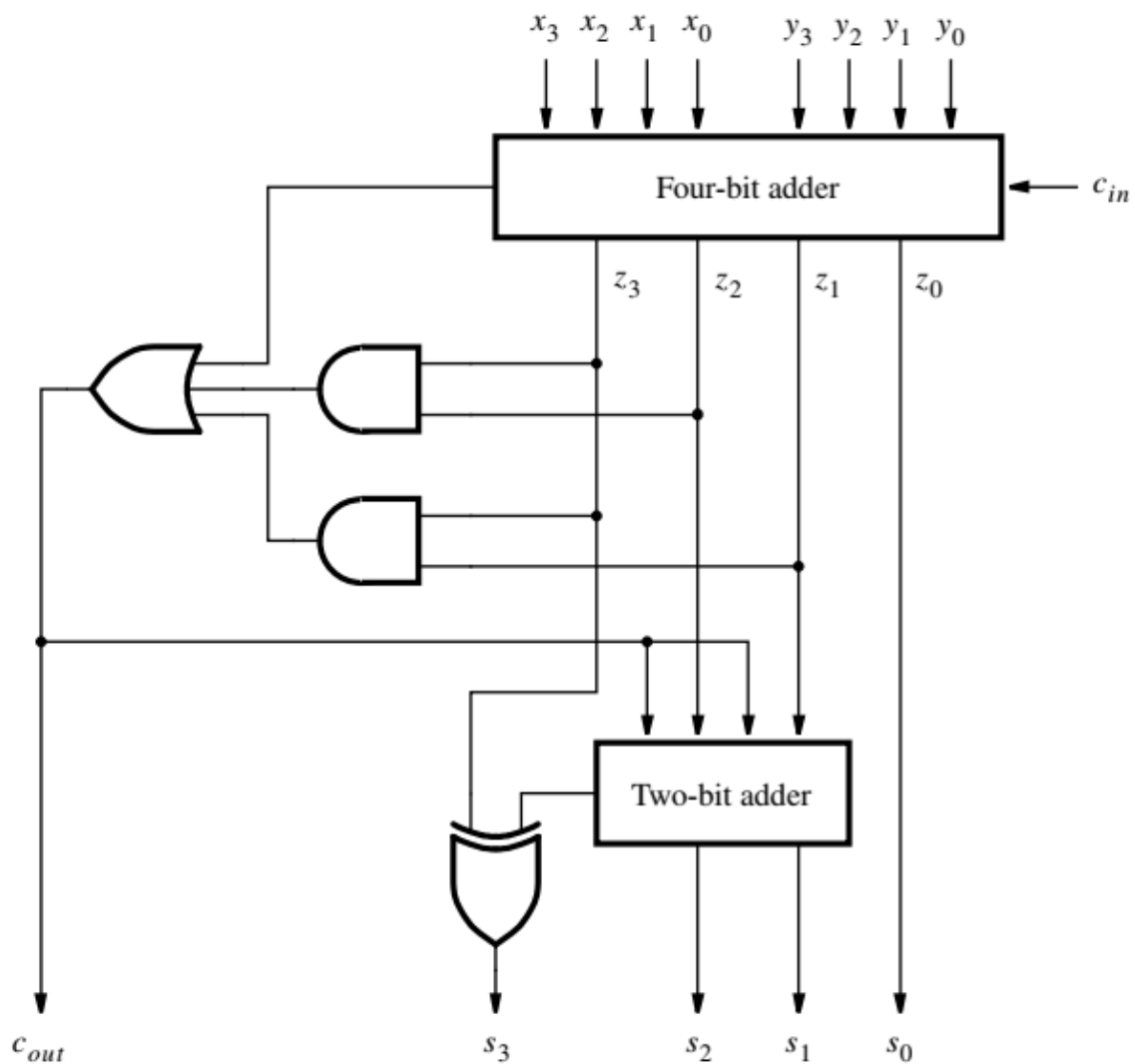
Explanation for the above circuit

When X + Y ≤ 9:

- The addition is the same as adding two 4-bit unsigned binary numbers.

When X + Y > 9:

- The result exceeds the valid range of BCD (which can only represent values 0-9).
- The sum will require two BCD digits.
- The initial 4-bit sum from the adder may be **incorrect** and needs correction.
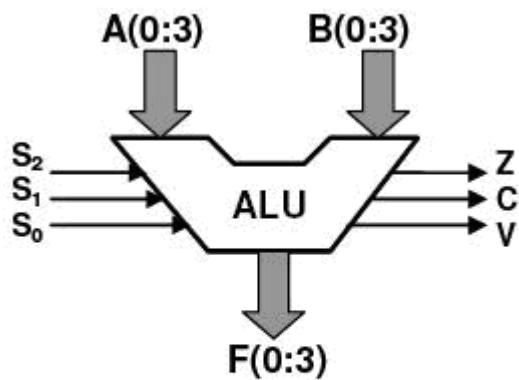
 Correction Needed: If the sum exceeds 9, an adjustment is required to ensure the result is a valid BCD representation.

$$\text{Adjust} = \text{Carry-out} + z_3(z_2 + z_1)$$

$$
\begin{array}{rrr}
X & 0\,1\,1\,1 & 7 \\
+\,Y & +\,0\,1\,0\,1 & +\,5 \\
\hline
Z & 1\,1\,0\,0 & 12 \\
& +\,0\,1\,1\,0 & \\
\hline
\text{carry} \longrightarrow & 1\,0\,0\,1\,0 & \\
& \underbrace{} & \\
& S = 2 &
\end{array}
$$

$$
\begin{array}{rrr}
X & 1\,0\,0\,0 & 8 \\
+\,Y & +\,1\,0\,0\,1 & +\,9 \\
\hline
Z & 1\,0\,0\,0\,1 & 17 \\
& +\,0\,1\,1\,0 & \\
\hline
\text{carry} \longrightarrow & 1\,0\,1\,1\,1 & \\
& \underbrace{} & \\
& S = 7 &
\end{array}
$$

Design Four-bit ALU

Z, C and V are status flags
$Z = 1$ if $F=0$
C = Carry or Borrow
V = Overflow

S_2	S_1	S_0	Function (F)
0	0	0	A+B
0	0	1	A-B
0	1	0	A-1
0	1	1	A+1
1	0	0	A $\wedge$ B
1	0	1	A $\vee$ B
1	1	0	NOT A
1	1	1	A $\oplus$ B