

### Assignment-03: Structural Modelling

- Design 4:1 using 2:1 multiplexer
- Design 8:1 using 2:1 multiplexer
- Design 1:2 demultiplexer,
- Design 1:8 demux using 1:2 demux
- Design 5:1 Mux using 2:1 multiplexer using structural design
- Design Adder cum Subtractor using structural design ( 4-bit)
- Design 4-bit Multiplier circuits as below

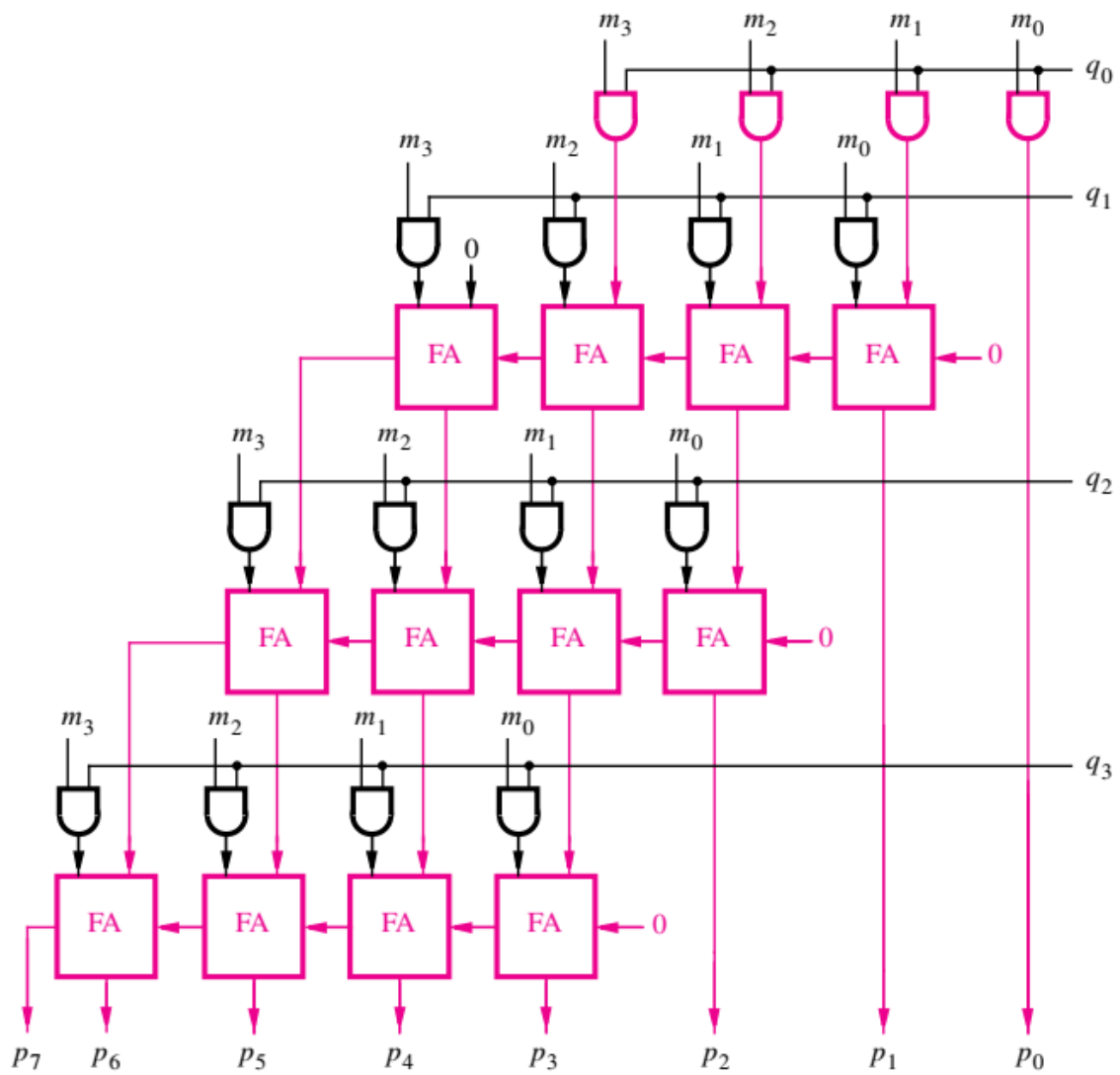
Multiplicand M	(14)	1 1 1 0	Multiplicand M	(14)	1 1 1 0
Multiplier Q	(11)	× 1 0 1 1	Multiplier Q	(11)	× 1 0 1 1
		1 1 1 0	Partial product 0		1 1 1 0
		1 1 1 0			+ 1 1 1 0
		0 0 0 0	Partial product 1		1 0 1 0 1
		1 1 1 0			+ 0 0 0 0
Product P	(154)	1 0 0 1 1 0 1 0	Partial product 2		0 1 0 1 0
					+ 1 1 1 0
			Product P	(154)	1 0 0 1 1 0 1 0

(a) Multiplication by hand

(b) Using multiple adders

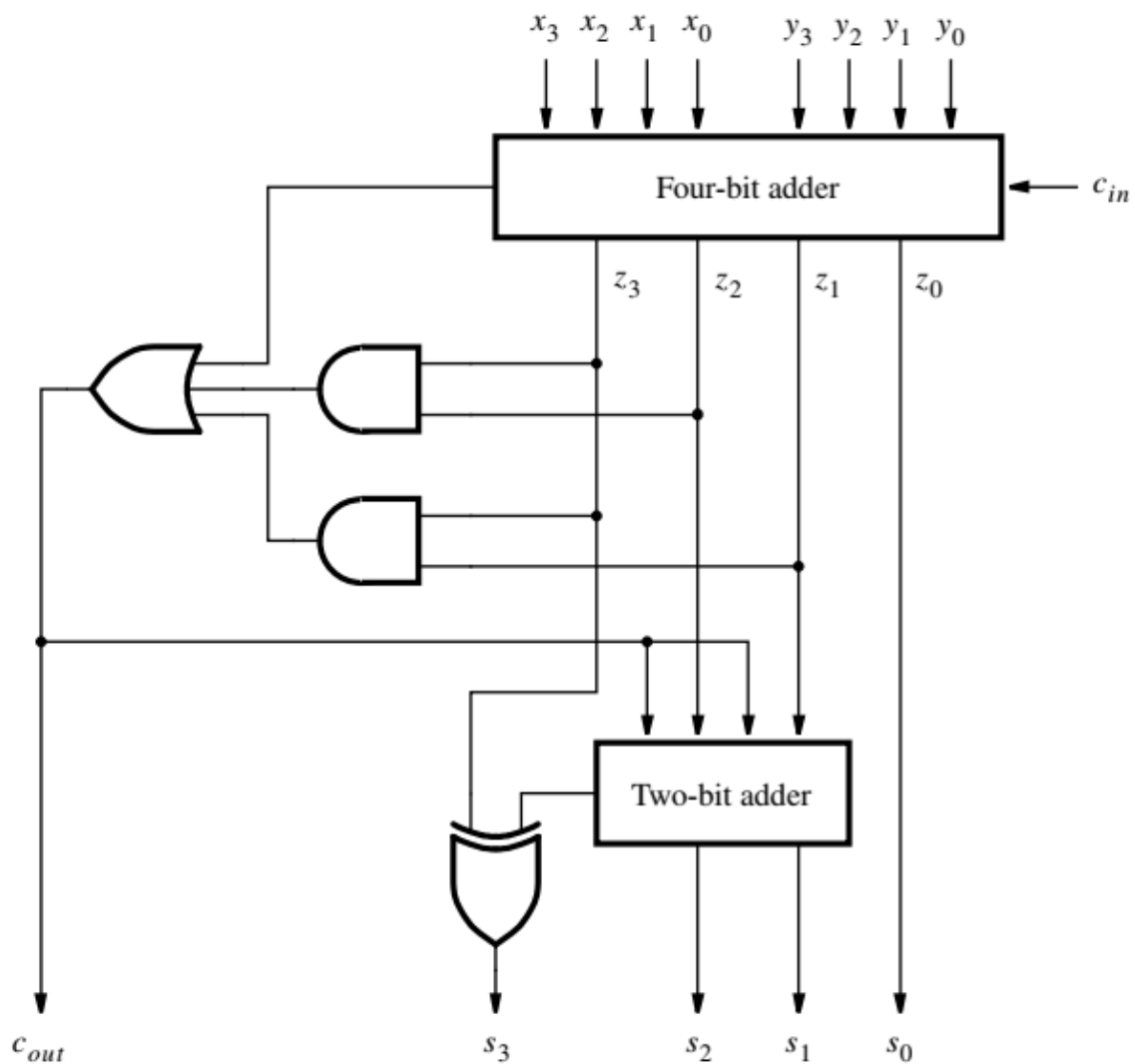
				$m_3$	$m_2$	$m_1$	$m_0$
				$\times \quad q_3$	$q_2$	$q_1$	$q_0$
Partial product 0					$m_3q_0$	$m_2q_0$	$m_1q_0$
					$+ \quad m_3q_1$	$m_2q_1$	$m_1q_1$
Partial product 1							$m_0q_1$
Partial product 2							
Product P	$p_7$	$p_6$	$p_5$	$p_4$	$p_3$	$p_2$	$p_1$

(c) Hardware implementation



Hardware implementation of four-bit multiplier

Write Verilog description for following BCD adder circuit and verify the results



Explanation for the above circuit

**When  $X + Y \leq 9$ :**

- The addition is the same as adding two 4-bit unsigned binary numbers.

**When  $X + Y > 9$ :**

- The result exceeds the valid range of BCD (which can only represent values 0-9).
- The sum will require two BCD digits.
- The initial 4-bit sum from the adder may be **incorrect** and needs correction.

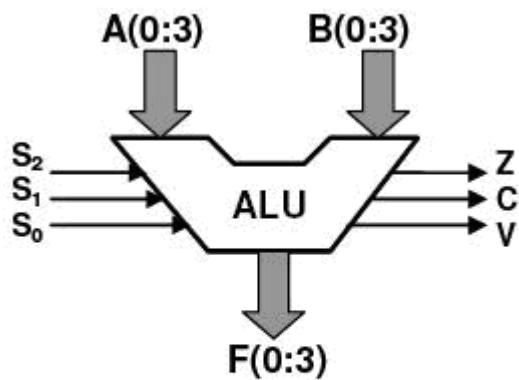
**Correction Needed:** If the sum exceeds 9, an adjustment is required to ensure the result is a valid BCD representation.

$$\text{Adjust} = \text{Carry-out} + z_3(z_2 + z_1)$$

$$\begin{array}{r}
 X \quad \quad 0111 \quad \quad 7 \\
 + Y \quad + 0101 \quad + 5 \\
 \hline
 Z \quad \quad 1100 \quad \quad 12 \\
 \quad \quad + 0110 \\
 \hline
 \text{carry} \rightarrow 10010 \\
 \quad \quad \quad \underbrace{\quad \quad \quad} \\
 \quad \quad \quad S = 2
 \end{array}$$

$$\begin{array}{r}
 X \quad \quad 1000 \quad \quad 8 \\
 + Y \quad + 1001 \quad + 9 \\
 \hline
 Z \quad \quad 10001 \quad \quad 17 \\
 \quad \quad + 0110 \\
 \hline
 \text{carry} \rightarrow 10111 \\
 \quad \quad \quad \underbrace{\quad \quad \quad} \\
 \quad \quad \quad S = 7
 \end{array}$$

Design Four-bit ALU



Z, C and V are status flags  
 Z = 1 if F=0  
 C = Carry or Borrow  
 V = Overflow

S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>	Function (F)
0	0	0	A+B
0	0	1	A-B
0	1	0	A-1
0	1	1	A+1
1	0	0	$A \wedge B$
1	0	1	$A \vee B$
1	1	0	NOT A
1	1	1	$A \oplus B$