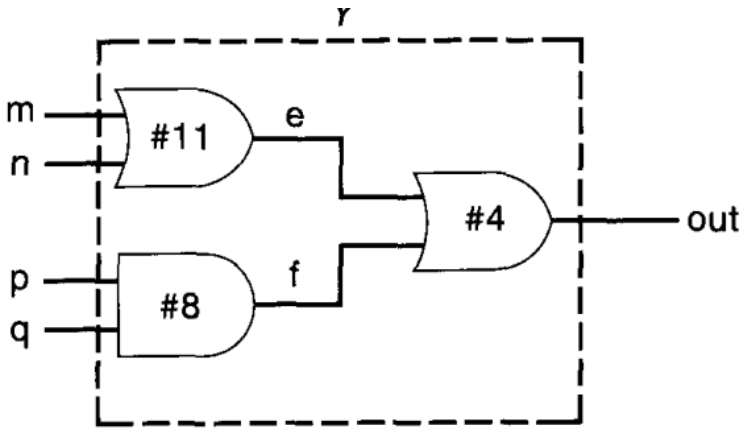
Assignment #13

Timing and Delays

Lumped Delay

1. What type of delay model is used in the following circuit? Write the Verilog description for the module Y.



2. For Exercise-1, use the largest delay in the module to convert the circuit to lumped delay model. using lumped delay model write the verilog description for module
3. Inverter with Lumped Delay : Use assign #2 out = in; Vary delay and observe waveform.
4. 2-input AND Gate with Lumped Delay : assign #3 out = a & b;
5. 2-input OR Gate with Different Lumped Delays , Use different delays for each gate in a chain.
6. Combinational Block (e.g., Half Adder) with Lumped Delay, Add # delays to all output assignments.
7. MUX with Lumped Delay : Implement 2:1 MUX using continuous assignment and delays

Distributed Delay

1. Inverter with Delay in Always Block, Use #2 inside always block:,
   always @(in) out = #2 in;
2. Half Adder Using Always Block and Distributed Delay :Insert delay before sum and carry assignment.
3. Full Adder with Delayed Assignments : Delay each internal wire and output

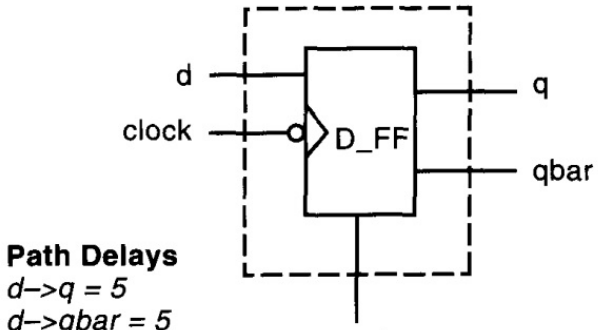
Pin-to-Pin Delay

1. Basic Gate with Pin-to-Pin Delay : Use gate instantiation with delays:
   and #(2,3) g1 (out, a, b); // rise = 2, fall = 3

2. 2-input NAND Gate with Unequal Pin-to-Pin Delay
   nand #(1:2:3, 3:2:1)

3. XOR Gate Using Pin-to-Pin Delay : Apply rise/fall delay on output.

4. Consider the negative edge-triggered with the asynchronous reset D-flipflop shown in the figure below. Write the Verilog description for the module D-FF. Show only the I/O ports and path delay specification. Describe path delays, using parallel connection.



Path Delays
d–>q = 5
d–>qbar = 5
clock–>q = 6
clock–> qbar = 7
reset–>q = 2
reset–>qbar = 3

5. 4-bit Comparator Using Pin-to-Pin Delay : Model per-bit comparison with delays.