VadaTech AMC502

FPGA Reference Design Manual

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vadatech inc

THE POWER OF VISION

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Revision History

Doc Rev	Description of Change	Revision Date
1.0.0	Document created	3/9/2015
1.0.1	Corrected FPGA RS-232 port references	3/18/2015
1.1.0	Added amc502_xxx_212_xxx XAUI+PCIe project.	1/19/2016
1.2.0	Updated to Vivado 2015.4. Added amc502_xxx_223_xxx PCIe x8 project.	5/20/2016
1.2.1	Added a project: amc502_xxx_210_xxx	7/13/2018

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Tables

1 Document Overview

This document describes the AMC502 FPGA reference designs available. These reference designs facilitate factory testing, customer acceptance testing, hardware debugging, and act as references for further customer development. FPGA/software development is expected to be performed at the customer's site to add any additional application-specific functionality to the AMC502 board.

1.1 Applicable Products

- VadaTech AMC502 (Kintex-7)

1.2 Document References

- VadaTech AMC502 Datasheet (http://www.vadatech.com)
- VadaTech FMCs User Manual
- PICMG® AMC.0 AdvancedMC Mezzanine Module (http://www.picmg.org)
- PICMG® AMC.1 AdvancedMC PCI Express and AS (http://www.picmg.org)
- PICMG® AMC.2 AdvancedMC Ethernet (http://www.picmg.org)
- PICMG® AMC.4 AdvancedMC Serial RapidIO (http://www.picmg.org)
- Xilinx Kintex-7 Datasheets and User's Guides
- Xilinx Vivado and IP Documentation
- ANSI/VITA 57.1 FPGA Mezzanine Card (FMC) Standard (http://www.vita.com)

1.3 Acronyms Used in this Document

Acronym	Description
AMC	Advanced Mezzanine Card
BAR	Base Address Register
BIST	Built-In Self Test
BSP	Board Support Package
C2M	Carrier-to-Mezzanine (signal)
CGND	Chassis Ground
CLK	Clock
CPU	Central Processing Unit
DIP	Dual In-line Package
FMC	FPGA Mezzanine Card
FPGA	Field Programmable Gate Array
FRU	Field Replaceable Unit
GbE	Gigabit Ethernet

GND	Signal Ground
GTX	Kintex-7 Multi-Gigabit Transceiver
HPC	High Pin Count (FMC connector)
IP	Intellectual Property
IPMI	Intelligent Platform Management Interface
JSM	JTAG Switch Module
JTAG	Joint Test Action Group
LED	Light Emitting Diode
LPC	Low Pin Count (FMC connector)
LVCMOS	Low-Voltage Complementary Metal Oxide Semiconductor
LVDS	Low Voltage Differential Signaling
M2C	Mezzanine-to-Carrier (signal)
MAC	Media Access Controller
MB	Megabyte (2^20 bytes)
M-LVDS	Multi-point Low Voltage Differential Signaling
MMC	Module Management Controller (IPMI controller of AMC)
n.c.	No connection
PCI	Peripheral Component Interconnect
PCIe	Peripheral Component Interconnect Express
PHY	Physical Layer Device
PICMG	PCI Industrial Computer Manufacturer's Group
PLL	Phase Locked Loop
SERDES	Serializer/Deserializer
SRIO	Serial RapidIO
TCLK	Telephony Clock
VADJ	Adjustable Voltage (power rail)
VIO	I/O Voltage (power rail)
VREF	Reference Voltage (power rail)
XAUI	Ten Gigabit Attachment Unit Interface

Table 1: Acronyms

2 FPGA Reference Design Mapping to Ordering Options

The AMC502 FPGA reference designs are broken up into various different VHDL projects/images. They are broken up to facilitate testing of the common board functionality vs. functionality that varies based on ordering options or FMC board attached.

Each reference design focuses on a specific hardware configuration and is identified by a combination of ordering options and possible suffixes to indicate additional functionality. Here are the ordering options from the AMC502 datasheet:

ORDERING OPTIONS **COMMON CONFIGURATIONS**

AMC502 – A0C – DEF – G0J

A = I/O Clock Signal Routing
0 = Standard routing
1 = CMS routing

C = Front Panel
1 = Reserved
2 = Mid-size
3 = Full-size
4 = Reserved
5 = Mid-size, MTCA.1 (captive screw)
6 = Full-size, MTCA.1 (captive screw)

D = FPGA
0 = Reserved
1 = Reserved
2 = XC7K420T

E = FPGA Speed
1 = Low (min buy required**)
2 = High
3 = Highest (min buy required**)

F = PCIe Option
0 = None
1 = PCIe on Ports 4-7
2 = PCIe on Ports 8-11
3 = PCIe on Ports 4-11

G = Clock Holdover Stability
0 = Standard (XO)
1 = Stratum-3 (TCXO)

J = Temperature Range and Coating
0 = Commercial (–5° to +55° C), No coating
1 = Commercial (–5° to +55° C), Humiseal 1A33 Polyurethane
2 = Commercial (–5° to +55° C),Humiseal 1B31 Acrylic
3 = Industrial (–20° to +70° C), No coating
4 = Industrial (–20° to +70° C), Humiseal 1A33 Polyurethane
5 = Industrial (–20° to +70° C), Humiseal 1B31 Acrylic
6 = Military (–40° to +85° C), Humiseal 1A33 Polyurethane*
7 = Military (–40° to +85° C), Humiseal 1B31 Acrylic*

*Edge of module for conduction-cooled boards
** Contact Sales for details

Certain ordering options have no direct impact on the FPGA portion of the board such as options C, G, and J. Therefore it is options A, D, E, and F that affect the FPGA projects/images.

When an ordering option value is specified in a project/image name, it indicates that this specific hardware variation is tested by the image. Please do not attempt to use an image on a board that has different options as this will result in a mismatch between the actual hardware on the board and the image.

When an ordering option value is not specified then it means that the image does not test that hardware. For example ‘AMC502-XXX-21X-XXX’ means that the image tests the density XC7K420T part (D=2) with speed grade 1 (E=1). Due to the way that speed grades are specified by the FPGA vendor, it is possible to use an E=1 image on E=2 and E=3 boards. Therefore the E option listed indicates a **minimum** speed grade for that image.

Certain projects/images will make use of standard features of the board and others will not. Since there is no convenient way to name projects based on the standard feature usage this usage is simply described in the documentation section for each image.

Each project/image uses the front panel U0, U1, U2, U3 LEDs in unique ways. Therefore, when interpreting these LEDs, make sure that you are aware of which FPGA image is actually loaded at the time.

The FPGA QSPI flash on the board is loaded with the default FPGA image that tests the standard baseboard functionality by default. The customer can overwrite the image with another image of their own choosing.

The projects/images are released in one top level zip file that is sequentially numbered such as 'release 1', 'release 2', etc. Each project/image within the top level zip file is individually versioned such as '1.0.1 R0', '1.2.0 R1', etc and this version number only changes when that particular project changes. This numbering scheme follows a 'Major.Minor.Patch Revision' scheme.

The currently supported reference designs are documented in the following sections. If the hardware features you are interested in verifying are not represented in the current set of reference designs please contact VadaTech.

3 FPGA Reference Design Projects

The following reference design projects are provided. Each highlights and tests specific combinations of hardware functionality available on the AMC502 board. Additional images will be provided as new configurations come on-line.

Speed Grade	Name	Primary Hardware Tested
1 (or faster)	AMC502-XXX-21X-XXX	AMC Backplane 1000Base-X (AMC Ports 0 & 1) Quad-PLL/M-LVDS CBS Clocks [default image]
1 (or faster)	AMC502-XXX-210-XXX	AMC backplane XAUI (AMC Ports 4-7) AMC backplane XAUI (AMC Ports 8-11)
1 (or faster)	AMC502-XXX-211-XXX	AMC backplane PCIe Gen2 x4 (AMC Ports 4-7), AMC backplane XAUI (AMC Ports 8-11)
1 (or faster)	AMC502-XXX-212-XXX	AMC backplane XAUI (AMC Ports 4-7), AMC backplane PCIe Gen2 x4 (AMC Ports 8-11)
2 (or faster)	AMC502-XXX-223-XXX	AMC backplane PCIe Gen2 x8 (AMC Ports 4-11)

Table 2: FPGA Reference Design Projects

3.1 Building the Reference Designs

The designs are built using **Vivado 2015.4** and **SDK 2015.4.** The pre-compiled images make use of hardware evaluation licenses where necessary rather than paid licenses. Because of this some of the IP cores may stop functioning after a number of hours of up-time. Simply reload the image if this occurs to continue testing or compile the image with full paid licenses. VadaTech does not provide licenses for the Vivado tool nor the IP cores from Xilinx. Please contact Xilinx directly for licensing, IP core, or Kintex-7 device-specific support.

NOTE: When building the images make sure to build the out-of-context runs first before performing the main run, otherwise the required sub-components won't be available on your machine and the main run will fail.

LEGAL NOTICE: The VadaTech custom VHDL code included in this reference design is the intellectual property of VadaTech Incorporated. Permission is granted to use the VadaTech custom VHDL code royalty-free in customer designs targeting the VadaTech AMC502 card only. Redistribution to third parties or use of this code for any other purpose is strictly prohibited.

3.2 Reference Design Common LEDs

Each image uses the front panel FPGA LEDs in different ways.

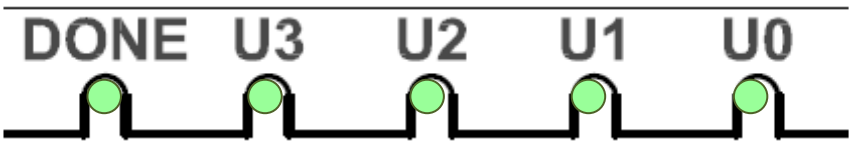


Figure 1: AMC502 Front Panel FPGA-controlled LEDs

The DONE LED always indicates whether the FPGA is configured or not configured. The four User LEDs are controlled by each image uniquely to reflect relevant status for that particular image.

3.3 AMC502-XXX-21X-XXX (Common Parts/Default Image)

This project two 1000Base-X ports to AMC Ports 0 and 1 for link up status checking (no packet data). This image is also used for clock testing of the Quad PLL/M-LVDS Crossbar Switch (CBS). Refer to the Clock Testing section for details.

An RS-232 serial console is provided on the FPGA RS-232 port to communicate with the soft-core MicroBlaze CPU in this image which controls the M-LVDS CBS /Quad PLL chips via I2C.

3.3.1 LEDs

LED	Test Coverage	Blinking	On	Off
U0	Configuration	n/a	FPGA powered/configured	n/a
U1	100MHz Clock 1	4 Hz	n/a	n/a
U2	AMC Port 0	n/a	1000Base-X Port 0 Linked	1000Base-X Port 0 NOT Linked
U3	AMC Port 1	n/a	1000Base-X Port 1 Linked	1000Base-X Port 1 NOT Linked

Table 3: AMC502-XXX-21X-XXX User LEDs

3.3.2 Troubleshooting

U0 doesn't turn on:
Check the payload power/reset and FPGA QSPI chip/image.

U1 doesn't blink:
Check the 100MHz clock 1.

U2 doesn't turn on:
Check the payload power/reset, 100MHz clock 1, 125MHz refclock, AMC Port 0.

U3 doesn't blink:
Check the payload power/reset, 100MHz clock 1, 125MHz refclock, AMC Port 1.

3.3.3 Structure

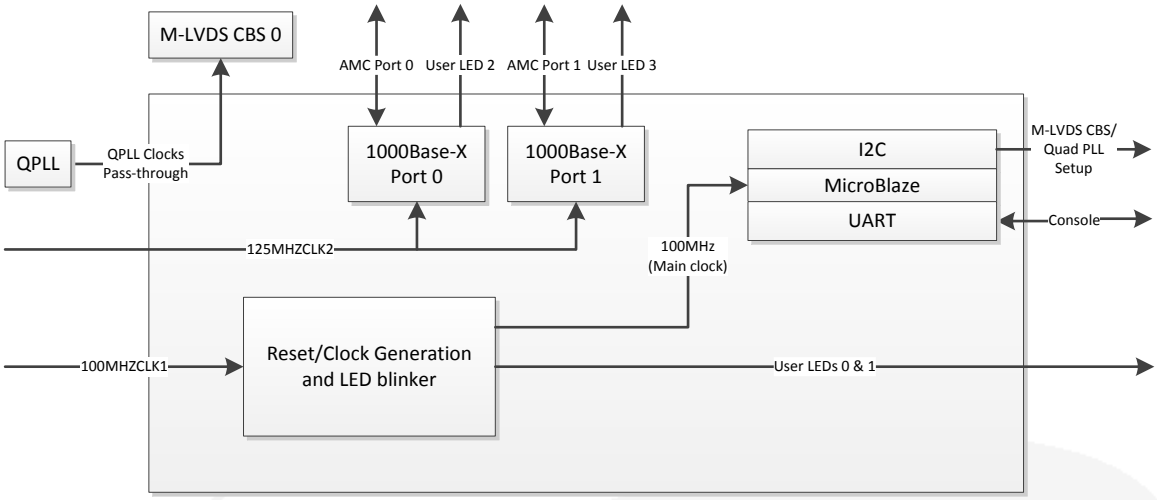


Figure 2: AMC502-XXX-21X-XXX Structure

3.4 AMC502-XXX-211-XXX (AMC PCIe Gen2 x4 AMC Ports 4-7 + XAUI AMC Ports 8-11)

This project implements a PCIe Gen2 x4 port on backplane AMC ports 4-7 for link establishment/enumeration only plus XAUI on AMC Ports 8-11 for link establishment only.

3.4.1 LEDs

LED	Test Coverage	Blinking	On	Off
U0	PCIe AMC Ports 4-7	n/a	App Ready	Not Ready
U1	XAUI AMC Ports 8-11	n/a	TX Ready	Not Ready
U2	PCIe AMC Ports 4-7	Link Up but not x4 or not Gen 2	Link Up x4 Gen 2	Not Linked
U3	XAUI AMC Ports 8-11	n/a	RX Link	Not Linked

Table 4: AMC502-XXX-211-XXX User LEDs

3.4.2 Checking PCIe link at the Far Side

To test the PCIe, you can use the **`pcie`** command on MCH 1 to see the link status, lane width, and speed at the PCIe switch fabric of the MCH for the slot that contains the AMC502.

Then you can test the PCIe enumeration using a PrAMC which implements a PCIe root complex. Make sure that the PrAMC boots up AFTER the AMC502 FPGA image is loaded (you may need to reboot the PrAMC to ensure this sequencing during development). Using the **`lspci`** command on a Linux PrAMC will show the enumeration results. The Vendor ID should appear as 0xABCD (VadaTech Incorporated) and the Device ID should appear as 0x4502 (AMC502).

3.4.3 Checking the XAUI Transmitters at the Far Side

To test the XAUI transmitters it is necessary to check the XAUI link status at the 10GbE Switch on the second MCH. The axel_l1stat all command should be run at least twice or the axel_l1stat <phys_port> repeat command run to ensure that the XAUI signals that are being transmitted by the FPGA are being received by each MCH. The ports should report LINK, ALIGN, SYNC3, SYNC2, SYNC1, SYNC0 steadily without any sporadic asterisk prefixes. It is normal to see the asterisks on the first status read however.

3.4.4 Troubleshooting

U0 doesn't turn on:
Check the 100MHz Clock 1 and FCLKA (100MHz) from the backplane.

U1 doesn't turn on:
Check the 100MHz Clock 1 and 156.25MHz Clock 1 generation on the board.

U2 doesn't turn on:
Check that a PCIe MCH is in the first MCH slot. Check the AMC lanes 4-7.

U3 doesn't turn on:
Check that a 10G MCH is in the second MCH slot. Check the AMC lanes 8-11.

3.4.5 Structure

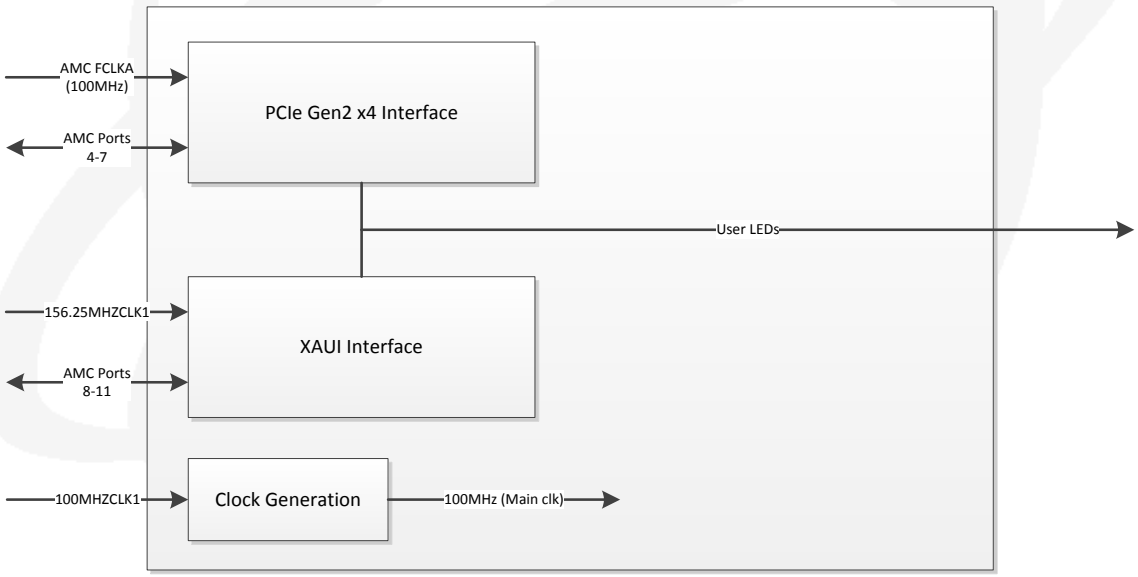


Figure 3: AMC502-XXX-211-XXX Structure

3.5 AMC502-XXX-212-XXX (AMC XAUI AMC Ports 4-7 + PCIe Gen2 x4 AMC Ports 8-11)

This project implements XAUI on AMC Ports 4-7 for link establishment only plus a PCIe Gen2 x4 port on backplane AMC ports 8-11 for link establishment/enumeration only.

3.5.1 LEDs

LED	Test Coverage	Blinking	On	Off
U0	XAUI AMC Ports 4-7	n/a	TX Ready	Not Ready
U1	PCIe AMC Ports 8-11	n/a	App Ready	Not Ready
U2	XAUI AMC Ports 4-7	n/a	RX Link	Not Linked
U3	PCIe AMC Ports 8-11	Link Up but not x4 or not Gen 2	Link Up x4 Gen 2	Not Linked

Table 5: AMC502-XXX-212-XXX User LEDs

3.5.2 Checking PCIe link at the Far Side

To test the PCIe, you can use the **`pcie`** command on MCH 2 to see the link status, lane width, and speed at the PCIe switch fabric of the MCH for the slot that contains the AMC502.

Then you can test the PCIe enumeration using a PrAMC which implements a PCIe root complex. Make sure that the PrAMC boots up AFTER the AMC502 FPGA image is loaded (you may need to reboot the PrAMC to ensure this sequencing during development). Using the **`lspci`** command on a Linux PrAMC will show the enumeration results. The Vendor ID should appear as 0xABCD (VadaTech Incorporated) and the Device ID should appear as 0x4502 (AMC502).

NOTE: Due to the MCH 1 slot being used for XAUI typically you will not be able to expect an FCLKA 100MHz PCIe clock distributed on the backplane (synchronous PCIe clocking). This image uses asynchronous PCIe clocking by utilizing an on-board 100MHz clock source. The PrAMC should similarly be configured.

3.5.3 Checking the XAUI Transmitters at the Far Side

To test the XAUI transmitters it is necessary to check the XAUI link status at the 10GbE Switch on the first MCH. The axel_l1stat all command should be run at least twice or the axel_l1stat <phys_port> repeat command run to ensure that the XAUI signals that are being transmitted by the FPGA are being received by each MCH. The ports should report LINK, ALIGN, SYNC3, SYNC2, SYNC1, SYNC0 steadily without any sporadic asterisk prefixes. It is normal to see the asterisks on the first status read however.

3.5.4 Troubleshooting

U0 doesn't turn on:
Check the 100MHz Clock 1 and 156.25MHz Clock 2 generation on the board.

U1 doesn't turn on:
Check the 100MHz Clock 1 and 100MHz Clock 0 generation on the board.

U2 doesn't turn on:
Check that a 10G MCH is in the first MCH slot. Check the AMC lanes 4-7.

U3 doesn't turn on:
Check that a PCIe MCH is in the second MCH slot. Check the AMC lanes 8-11.

3.5.5 Structure

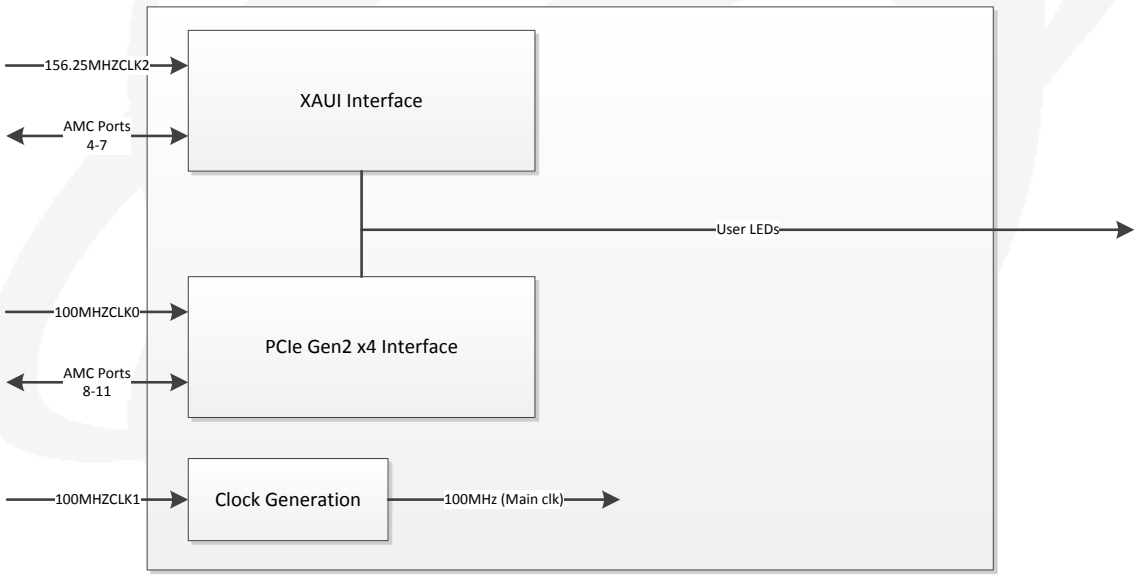


Figure 4: AMC502-XXX-212-XXX Structure

3.6 AMC502-XXX-223-XXX (AMC PCIe Gen2 x8 AMC Ports 4-11)

This project implements a PCIe Gen2 x8 port on backplane AMC ports 4-11 for link establishment/enumeration only.

NOTE: This image is compatible with E=2 or E=3 boards, not E=1 boards due to the chip's requirement of speed grade -2 or higher to do Gen2 speed for x8 links.

3.6.1 LEDs

LED	Test Coverage	Blinking	On	Off
U0	PCIe AMC Ports 4-11	n/a	App Ready	Not Ready
U1		n/a	Link Up	Not Linked
U2		Not x8 width	x8 width	n/a
U3		Not Gen2 speed	Gen2 speed	n/a

Table 6: AMC502-XXX-223-XXX User LEDs

3.6.2 Checking PCIe link at the Far Side

A PCIe x8 chassis configuration should be used. To test the PCIe, you can use the **`pcie`** command on MCH 1 to see the link status, lane width, and speed at the PCIe switch fabric of the MCH for the slot that contains the AMC502.

Then you can test the PCIe enumeration using a PrAMC which implements a PCIe root complex. Make sure that the PrAMC boots up AFTER the AMC502 FPGA image is loaded (you may need to reboot the PrAMC to ensure this sequencing during development). Using the **`lspci`** command on a Linux PrAMC will show the enumeration results. The Vendor ID should appear as 0xABCD (VadaTech Incorporated) and the Device ID should appear as 0x4502 (AMC502).

3.6.3 Troubleshooting

U0 doesn't turn on:
Check the 100MHz Clock 1 and FCLKA (100MHz) from the backplane.

U1 doesn't turn on:
Check the 100MHz Clock 1 and FCLKA (100MHz) from the backplane as well as AMC Ports 4-11.

U2 blinks:
Check that a x8 chassis/MCH is used. Check AMC Ports 4-11.

U3 blinks:
Check that a Gen2 or higher MCH is used. Check AMC Ports 4-11.

3.6.4 Structure

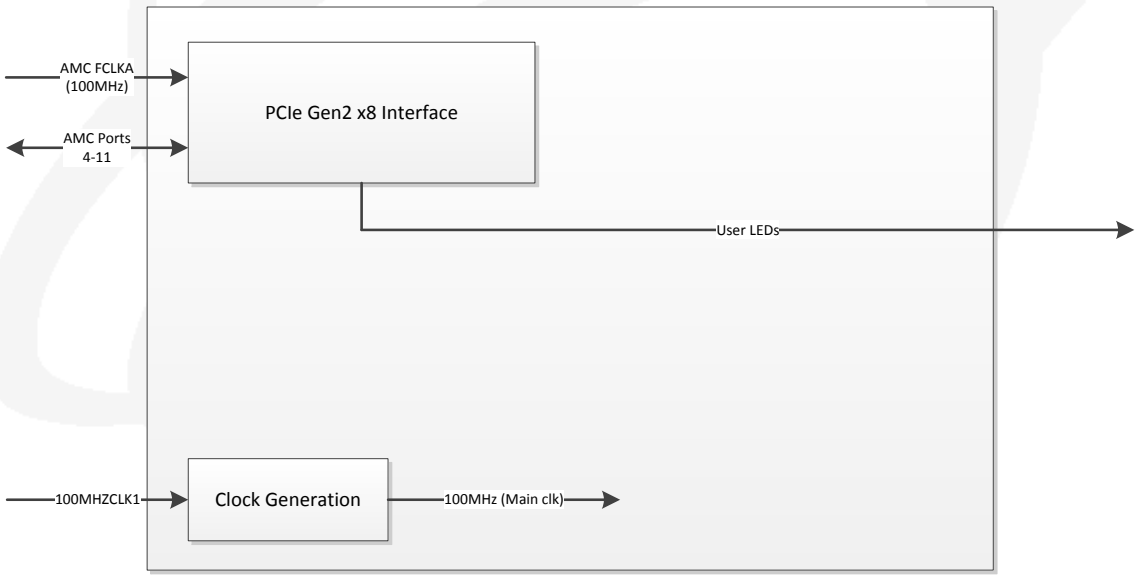


Figure 5: AMC502-XXX-223-XXX Structure

3.7 AMC502-XXX-210-XXX (2 XAUI Interfaces ON AMC Ports 4-7 and Ports 8-11)

This project implements 2 XAUI Interfaces on backplane AMC ports 4-7 and Ports 8-11 for link establishment only.

3.7.1 LEDs

LED	Test Coverage	Blinking	On	Off
U0	XAUI Tx on AMC Ports 4-7	Not Ready	TX Ready	N/A
U1	XAUI Rx on AMC Ports 4-7	Not Linked	RX Link	N/A
U2	XAUI Tx on AMC Ports 8-11	Not Ready	TX Ready	N/A
U3	XAUI Rx on AMC Ports 8-11	Not Linked	RX Link	N/A

Table 7: AMC502-XXX-210-XXX User LEDs

3.7.2 Checking the XAUI Transmitters at the Far Side

To test the XAUI transmitters it is necessary to check the XAUI link status at the 10GbE Switch on the both MCH1 and MCH2. First, on the MCH1/2 console, Type “sty rows 200” and “minicom -o -w ttyS2” commands to get to the MCH 10GbE prompt. Then type “axel_l1stat all” or “axel_l1stat <phys_port>” at least 2 times to ensure that the XAUI signals that are being transmitted by the FPGA are being received by each MCH. The ports should report LINK, ALIGN, SYNC3, SYNC2, SYNC1, SYNC0 steadily without any sporadic asterisk prefixes. It is normal to see the asterisks on the first status read however.

3.7.3 Troubleshooting

U0 Blinking:
Check the 156.25MHz (CLK156_25MHZ2_P/N) from the backplane.

U1 Blinking:
Check that a 10G MCH1 is in the first MCH slot. Check the AMC lanes 4-7.

U2 doesn't turn on:
Check the 156.25MHz (CLK156_25MHZ1_P/N) from the backplane.

U3 Blinking:
Check that a 10G MCH2 is in the second MCH slot. Check the AMC lanes 8-11.

3.7.4 Structure

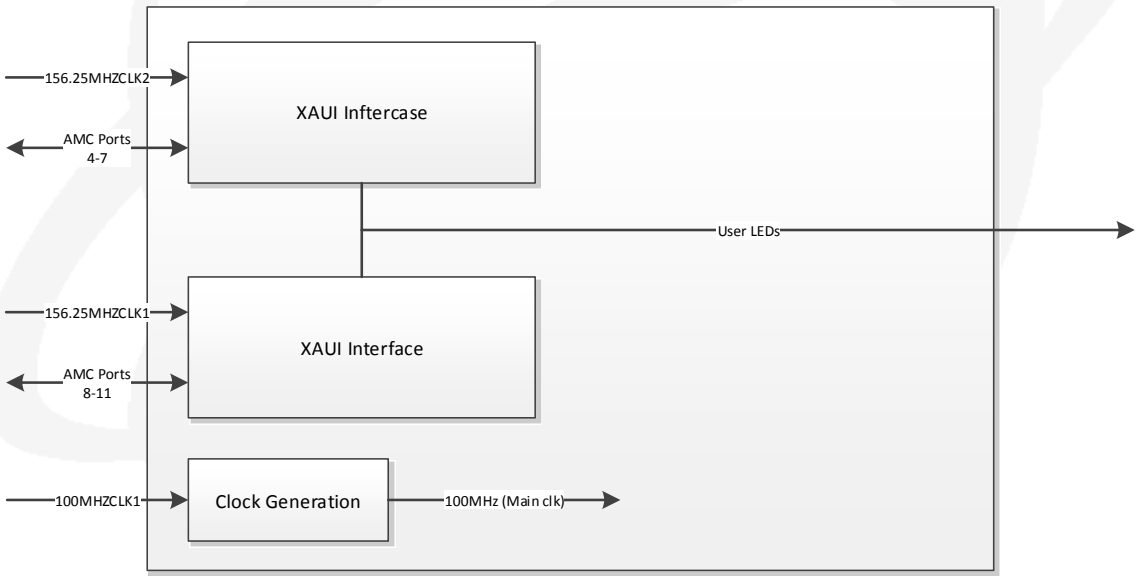


Figure 6: AMC502-XXX-210-XXX Structure

4 Clock Testing

The default FPGA image is used in conjunction with the MicroBlaze CPU interface to facilitate M-LVDS CBS and Quad PLL clock testing. The CPU sets up the following three clock testing scenarios when activated via the FPGA RS-232 interface:

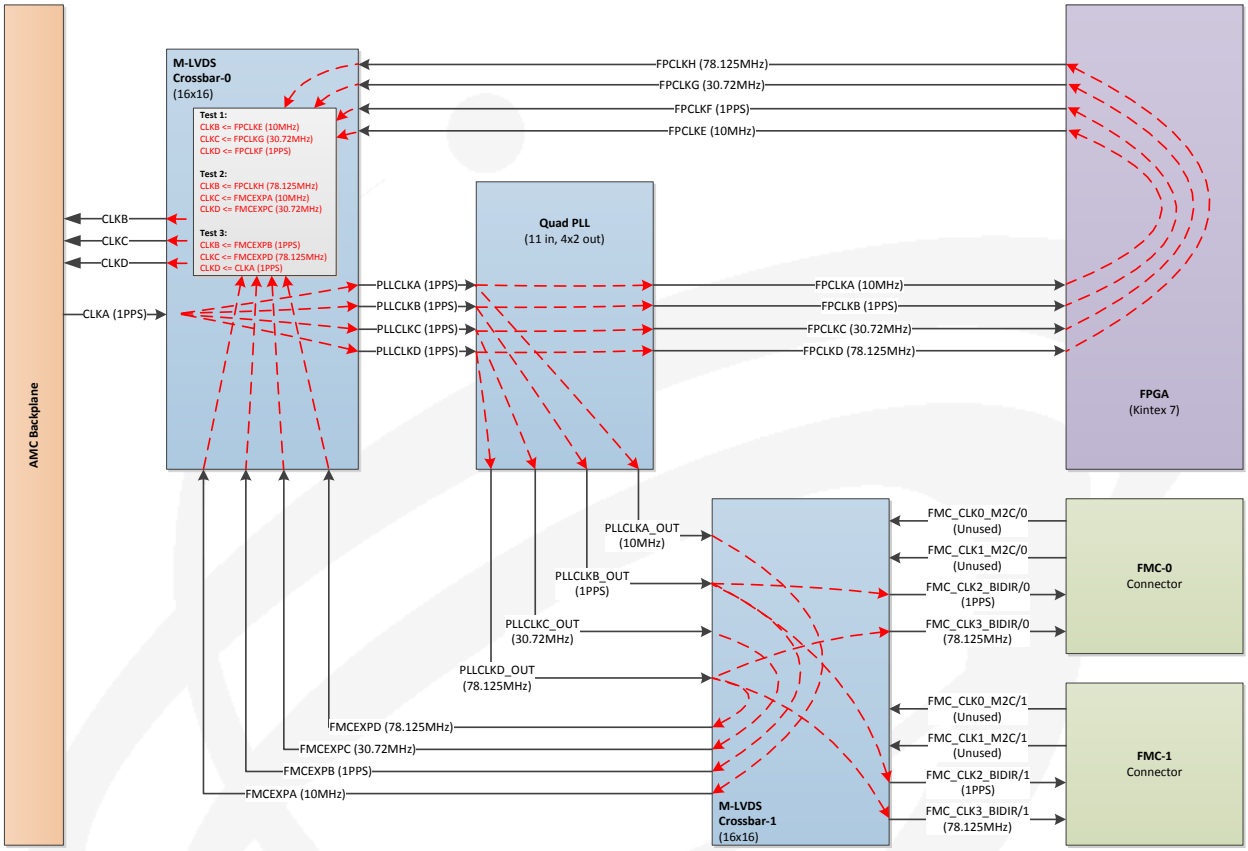


Figure 7: AMC502 M-LVDS and Quad PLL Clock Test Scenario

The test is setup so that an external 1PPS (or 1Hz) signal can be injected via backplane TCLKA/CLK1. The 1PPS is distributed through the crossbar to the first four reference inputs of the Quad PLL. The clock tool can be used to see the PLL qualify these references and lock its four PLLs to them. Then the PLL synthesizers are set up to output various frequencies to both the second M-LVDS CBS and the FPGA in parallel. The clocks going to the FPGA looped through to the first M-LVDS CBS. The outputs that went to the second CBS are routed back to the first M-LVDS CBS as well as to the FMC connectors. The three test setups simply select which clocks route out to the backplane TCLKB, TCLKC, and TCLKD ports for testing with an oscilloscope after they have been routed to an MCH, etc.

NOTE: The test scenario shown here is for diagnostic testing purposes only. Additional customer setup/development will be necessary to implement real-world application clocking. Refer to the

AMC502 Hardware Reference Manual for a clocking diagram showing the baseline capabilities of the hardware.

The MicroBlaze CPU interface appears as a menu on the FPGA RS-232 port of the front panel. The serial port settings are 115200-N-8-1-NOFLOW. The menu appears as follows:

```
AMC502 FPGA Reference Design - Telco Clocking Test Interface v1.0.0 R0

Please select a menu option below:
   1) Configure board for Telco Clocking Test 1
   2) Configure board for Telco Clocking Test 2
   3) Configure board for Telco Clocking Test 3
   4) Display M-LVDS CBS configuration
   5) Display Quad PLL Status
   6) Dump Quad PLL register space
>>
```

To configure the board for the clocking tests, press 1, 2, or 3 depending on the test scenario you'd like to run. The software will output the following:

Test 1:

```
Configuring M-LVDS CBS for test 1 setup
Configuring QPLL for test setup

Please inject a 1PPS into TCLKA for the PLL reference.

Expect 10MHz on TCLKB, 30.72MHz on TCLKC, 1PPS on TCLKD,
1PPS on FMC_CLK2_BIDIR/x, 78.125MHz on FMC_CLK3_BIDIR/x.

Check the Quad PLL status to verify reference qualification and PLL locking.
```

Test 2:

```
Configuring M-LVDS CBS for test 2 setup
Configuring QPLL for test setup

Please inject a 1PPS into TCLKA for the PLL reference.

Expect 78.125MHz on TCLKB, 10MHz on TCLKC, 30.72MHz on TCLKD,
1PPS on FMC_CLK2_BIDIR/x, 78.125MHz on FMC_CLK3_BIDIR/x.

Check the Quad PLL status to verify reference qualification and PLL locking.
```

Test 3:

```
Configuring M-LVDS CBS for test 3 setup
Configuring QPLL for test setup

Please inject a 1PPS into TCLKA for the PLL reference.

Expect 1PPS on TCLKB, 78.125MHz on TCLKC, 1PPS on TCLKD,
1PPS on FMC_CLK2_BIDIR/x, 78.125MHz on FMC_CLK3_BIDIR/x.

Check the Quad PLL status to verify reference qualification and PLL locking.
```

After configuration, the M-LVDS CBS configuration can be verified by pressing 4. The example below shows the expected configuration for Test 3:

```
M-LVDS CBS 0:
 0 (tclka           ): 0x60 (input  term  )
 1 (tclkb           ): 0xED (output term   noinv <= fmcexpb)
 2 (tclkc           ): 0xEF (output term   noinv <= fmcexpd)
 3 (tclkd           ): 0xE0 (output term   noinv <= tclka)
 4 (pllclka         ): 0xE0 (output term   noinv <= tclka)
 5 (pllclkb         ): 0xE0 (output term   noinv <= tclka)
 6 (pllclkc         ): 0xE0 (output term   noinv <= tclka)
 7 (pllclkd         ): 0xE0 (output term   noinv <= tclka)
 8 (fpclke          ): 0x60 (input  term  )
 9 (fpclkf          ): 0x60 (input  term  )
10 (fpclkg          ): 0x60 (input  term  )
11 (fpclkh          ): 0x60 (input  term  )
12 (fmcexpa         ): 0x60 (input  term  )
13 (fmcexpb         ): 0x60 (input  term  )
14 (fmcexpc         ): 0x60 (input  term  )
15 (fmcexpd         ): 0x60 (input  term  )

M-LVDS CBS 1:
 0 (fmcexpa         ): 0xE4 (output term   noinv <= pllclka_out)
 1 (fmcexpb         ): 0xE5 (output term   noinv <= pllclkb_out)
 2 (fmcexpc         ): 0xE6 (output term   noinv <= pllclkc_out)
 3 (fmcexpd         ): 0xE7 (output term   noinv <= pllclkd_out)
 4 (pllclka_out     ): 0x60 (input  term  )
 5 (pllclkb_out     ): 0x60 (input  term  )
 6 (pllclkc_out     ): 0x60 (input  term  )
 7 (pllclkd_out     ): 0x60 (input  term  )
 8 (fmc_clk0_m2c/0  ): 0x60 (input  term  )
 9 (fmc_clk1_m2c/0  ): 0x60 (input  term  )
10 (fmc_clk2_bidir/0): 0xE5 (output term   noinv <= pllclkb_out)
11 (fmc_clk3_bidir/0): 0xE7 (output term   noinv <= pllclkd_out)
12 (fmc_clk0_m2c/1  ): 0x60 (input  term  )
13 (fmc_clk1_m2c/1  ): 0x60 (input  term  )
14 (fmc_clk2_bidir/1): 0xE5 (output term   noinv <= pllclkb_out)
15 (fmc_clk3_bidir/1): 0xE7 (output term   noinv <= pllclkd_out)
```

Finally, the Quad PLL status can be verified by pressing 5. An example of the expected output is shown below.

```
                        TYPE         EXPECTING   PFM  GST  CFM  SCM  LOS
                        ------------ ----------- ---- ---- ---- ---- ----
Ref00 (pllclka     ): differential   1.000 Hz  OK   OK   OK   OK   OK
Ref01 (pllclkb     ): differential   1.000 Hz  OK   OK   OK   OK   OK
Ref02 (pllclkc     ): differential   1.000 Hz  OK   OK   OK   OK   OK
Ref03 (pllclkd     ): differential   1.000 Hz  OK   OK   OK   OK   OK
Ref04 (            ): differential   1.000 Hz  FAIL FAIL FAIL FAIL OK
Ref05 (            ): differential   1.000 Hz  FAIL FAIL FAIL FAIL OK
Ref06 (            ): differential   1.000 Hz  FAIL FAIL FAIL FAIL OK
Ref07 (            ): differential   1.000 Hz  FAIL FAIL FAIL FAIL OK
Ref08 (            ): differential   1.000 Hz  FAIL FAIL FAIL FAIL OK
Ref09 (            ): single-ended   1.000 Hz  FAIL FAIL FAIL FAIL OK
Ref10 (            ): single-ended   1.000 Hz  FAIL FAIL FAIL FAIL OK

      ENABLED LOCKED HOLDOVER SELECTED REF
      ------- ------ -------- ------------
PLL0: YES     YES    NO       Ref00
PLL1: YES     YES    NO       Ref01
PLL2: YES     YES    NO       Ref02
PLL3: YES     YES    NO       Ref03

                        ENABLED SOURCE LOCKED FREQUENCY
                        ------- ------ ------ -----------
Synth0:                 YES     PLL0   YES      1.000 GHz
 Out0A (pllclka_out): YES                    10.000 MHz
 Out0B (fpclka     ): YES                    10.000 MHz
 Out0C (           ): NO                     10.000 MHz
 Out0D (           ): NO                     10.000 MHz
Synth1:                 YES     PLL1   YES      1.000 GHz
 Out1A (pllclkb_out): YES                     1.000 Hz
 Out1B (fpclkb     ): YES                     1.000 Hz
 Out1C (           ): NO                      1.000 Hz
 Out1D (           ): NO                      1.000 Hz
Synth2:                 YES     PLL2   YES      1.014 GHz
 Out2A (pllclkc_out): YES                    30.720 MHz
 Out2B (fpclkc     ): YES                    30.720 MHz
 Out2C (           ): NO                     30.720 MHz
 Out2D (           ): NO                     30.720 MHz
Synth3:                 YES     PLL3   YES      1.094 GHz
 Out3A (pllclkd_out): YES                    78.125 MHz
 Out3B (fpclkd     ): YES                    78.125 MHz
 Out3C (           ): NO                     78.125 MHz
 Out3D (           ): NO                     78.125 MHz
```

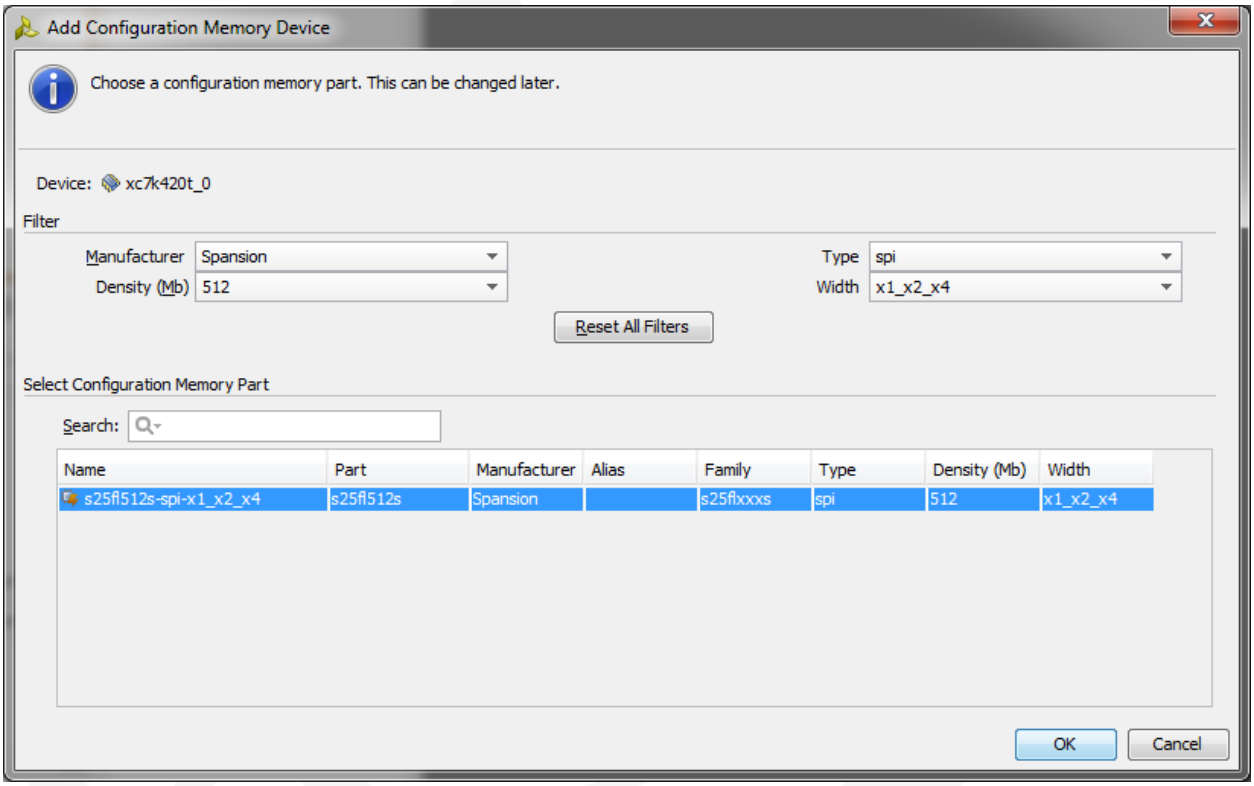
The software source code projects for the MicroBlaze CPU can be found in the **amc502_xxx_21x_xxx.sdk** directory and can be modified by the customer using Xilinx SDK to facilitate specific application clocking configurations.

5 Programming the FPGA QSPI Configuration Flash

The configuration flash on the board may be programmed via either JTAG or the iMX6 CPU.

5.1 Programming via JTAG

When programming via JTAG, use Vivado to add the configuration memory device to the Hardware Manager as shown below:



The flash can be programmed from the .bin file that is generated by the project.

NOTE: The optimal settings for the flash are SPI x4 mode using the external configuration clock (50MHz) in DIV-1 mode. However, there is a problem with the Vivado 2014.x software which requires extra steps to enable the x4 mode with the Spansion flash. Please refer to this answer record for details: http://www.xilinx.com/support/answers/61067.html

Due to this software problem, Vadatech has tested the x4 mode as working on the board but is shipping the flash image as x2 mode to eliminate time consuming extra steps in the production process and incompatibility with the iMX6 upgrade method and external pre-programmers. Customers may use the x4 mode if needed using JTAG upgrade method and the workaround provided by Xilinx. Xilinx expects to have this problem fixed in the 2015.1 version of the tool.

5.2 Programming via iMX6 CPU

To program the FPGA QSPI flash via the iMX6 CPU:

1) Transfer the **`.bin`** file to the **`/upgrade`** directory of the CPU using **`scp`** or some other method.
2) Run: **`fpga_upgrade <filename>`**
3) The programming sequence described in the hardware reference manual will be performed.