VadaTech UTC001

Hardware Reference Manual

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Table of Contents

1 Overview 7
1.1 About This Manual 7
1.1.1 Feedback 8
1.1.2 Document References 8
1.2 Acronyms Used in this Document 8
2 UTC001 General Description 9
2.1 Mechanical Description 9
2.2 Architectural Description 11
2.3 IPMI Controller 12
2.4 1GbE Layer 2 Managed Switch Option (B = 1) 12
2.5 SAS/SATA Expander Option (C = 1) 13
2.6 Fabric Clock Option (F != 0) 14
2.7 Telcom TCXO Clock Option (E = 1) 14
2.8 GPS VCTCXO Clock Option (E = 2 or 3) 15
2.9 Telco Clock Routing Support w/ Telcom/GPS Clock Options (E = 1, 2, or 3) 16
2.10 PCIe Fabric Option – DA111 (D = 1) 17
2.11 10GbE Fabric Option – DA112 (D = 3 or 4) 18
2.12 SRIO Fabric Option - DA113 (D = 2) 19
2.13 Front Panel 20
2.14 The ATCA Management LEDs 21
2.15 Insertion/Removal Mechanism 21
2.16 Port Pin-outs 22
2.17 Switch settings 23
3 Software 24
4 Specifications 25

Figures

Figure 1: UTC001 (Base board) component side layout 9
Figure 2: VT002 (IPMI Controller) component side layout 9
Figure 3: DA111 (PCIe Fabric) component side layout 10
Figure 4: DA112 (10GbE Fabric) component side layout 10
Figure 5: DA113 (SRIO Fabric) component side layout 10
Figure 6: UTC001 base block diagram 11
Figure 7: DA112 block diagram 18
Figure 8: UTC001 front panel 20

Tables

Table 1: Acronyms....8
Table 2: Port configuration of the 1GBE switch....12
Table 3: SAS/SATA connectivity options....13
Table 4: SAS/SATA expander configuration....13
Table 5: Fabric clock connectivity options....14
Table 6: Telco clock connectivity options....16
Table 7: PCIe configuration....17
Table 8: 10GBE switch port configuration....18
Table 9: SRIO x4 switching fabric port configuration....19
Table 10: UTC001 ATCA LEDs....21
Table 11: Serial port pin out....22
Table 12: Expansion ports pin out....22
Table 13: Specifications....25

1 Overview

The UTC001 is a feature-rich MicroTCA Carrier Hub (MCH) module based on the MicroTCA (µTCA) specification. It provides complete µTCA Carrier Management Controller (MCMC) as well as an optional Shelf Manager functionality. It comes with a 1GbE (L2 Managed) switch fabric option with an optional SAS/SATA Expander plus one additional optional fabric for PCIe (Gen2 x4), SRIO (x4), or 10GbE (L3 Managed). PCIe clock generation with or without Spread Spectrum Clocking is optionally available. The UTC001 also provides Telco clock distribution and synchronization with Stratum 3 holdover via Telecom and GPS synchronized clocking options.

As a hot-swappable field replaceable unit (FRU), the UTC001 follows a stringent carrier grade feature set to provide Reliability, Availably, Serviceability and Maintainability (RASM). The UTC001 supports a redundant configuration with two UTC001's in the same chassis with automatic failover. When two UTC001's are used in a chassis, advanced high-speed fabric combinations are supported such as PCIe + 10GbE.

The software is IPMI 2.0 Compliant and can also be ordered as a protocol analyzer to aid in system integration/debugging (ordering option 'A' determines the software load for MCMC only, MCMC and Shelf Manager, or Protocol Analyzer).

1.1 About This Manual

The UTC001 reference manual provides functional, architectural, and mechanical descriptions of the UTC001 module. This manual is intended for anyone who designs OEM products which have requirements for an MCH to provide chassis/shelf management, switch fabrics, and/or Telco clocking.

The UTC001 design is highly modular and includes various mount options and daughter cards. These options are exposed as ordering options in the UTC001 Datasheet. These ordering options are mentioned in the remainder of this manual such as 'E = 3' to explain how the ordering options affect the hardware functionality. Please refer to the last page of the UTC001 Datasheet for a list of these options. They generally take the form of 'UTC001-ABC-DEF-GHJ'. The letters are replaced by numbers selected from the lists of available options. Please keep your model number handy when reviewing the remainder of this document so that you can keep your particular configuration in mind.

1.1.1 Feedback

VadaTech welcomes feedback about how we can make our manuals and technical documentation more useful to our customers. Please feel free to send comments and suggestions to support@vadatech.com.

1.1.2 Document References

- VadaTech UTC001 Management Software Reference Manual
- VadaTech UTC001 Getting Started Guide

1.2 Acronyms Used in this Document

Acronym	Description
AMC	Advanced Mezzanine Card
ATCA	Advanced Telecommunications Computing Architecture
FRU	Field Replaceable Unit
GbE	Gigabit Ethernet
GPS	Global Positioning System
I-PASS	Infiniband (connector)
IPMI	Intelligent Platform Management Interface
L2	Layer 2 (i.e. Link Layer)
L3	Layer 3 (i.e. IP Layer)
MCH	MicroTCA Carrier Hub
MCMC	MicroTCA Carrier Management Controller
PCIe	Peripheral Component Interconnect Express
SAS	Serial Attached SCSI
SATA	Serial AT Attachment
SMA	SubMiniature Version A (connector)
SRIO	Serial Rapid I/O
TCXO	Temperature Compensated Crystal Oscillator
*u*TCA	MicroTCA
VCTCXO	Voltage Controlled Temperature Compensated Crystal Oscillator
XAUI	10 Gigabit Attachment Unit Interface

Table 1: Acronyms

2 UTC001 General Description

2.1 Mechanical Description

The UTC001 is a µTCA Carrier Hub (full-height) measuring 180.6 mm by 73.5 mm. The UTC001 module is made up of several boards; the UTC001 base board, the VT002 IPMI Controller board, and an optional high-speed fabric board which is one of DA111 (PCIe Gen2 x4), DA112 (10GbE), or DA113 (SRIO). The following figures show the component side layouts of these boards:

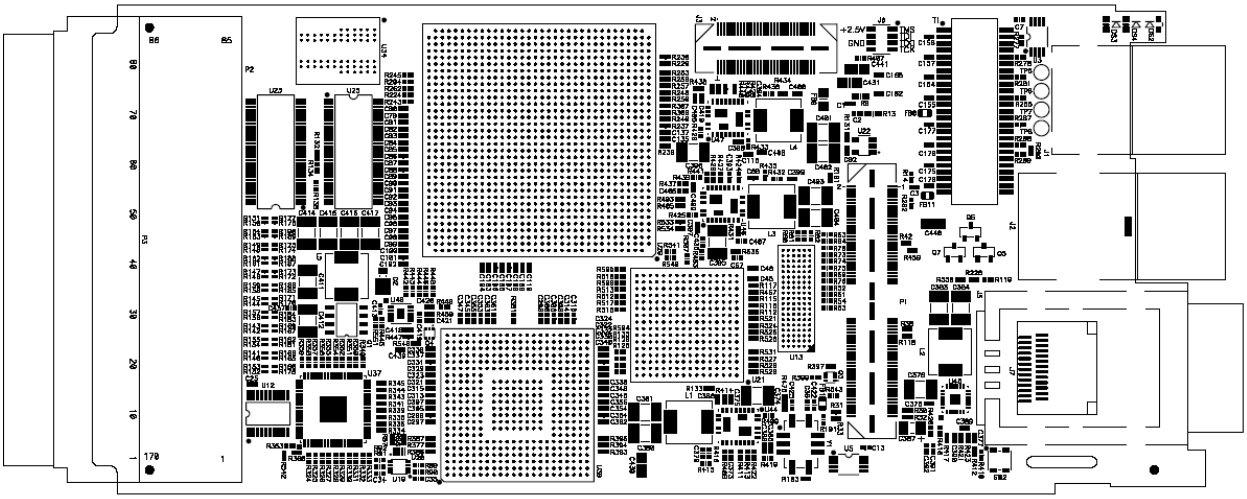

Figure 1: UTC001 (Base board) component side layout

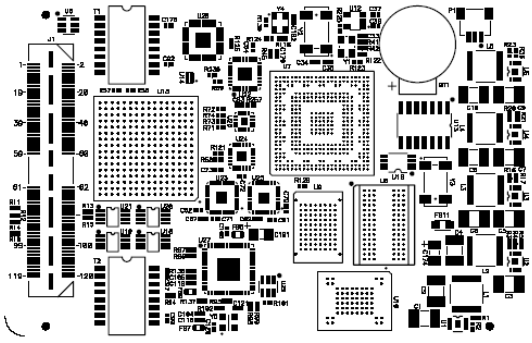

Figure 2: VT002 (IPMI Controller) component side layout

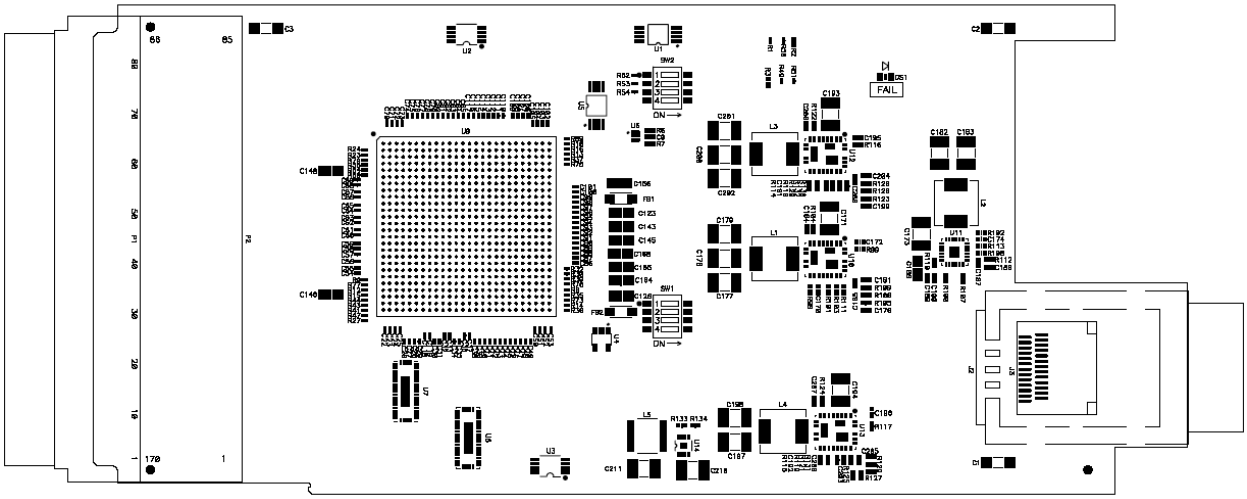

Figure 3: DA111 (PCIe Fabric) component side layout

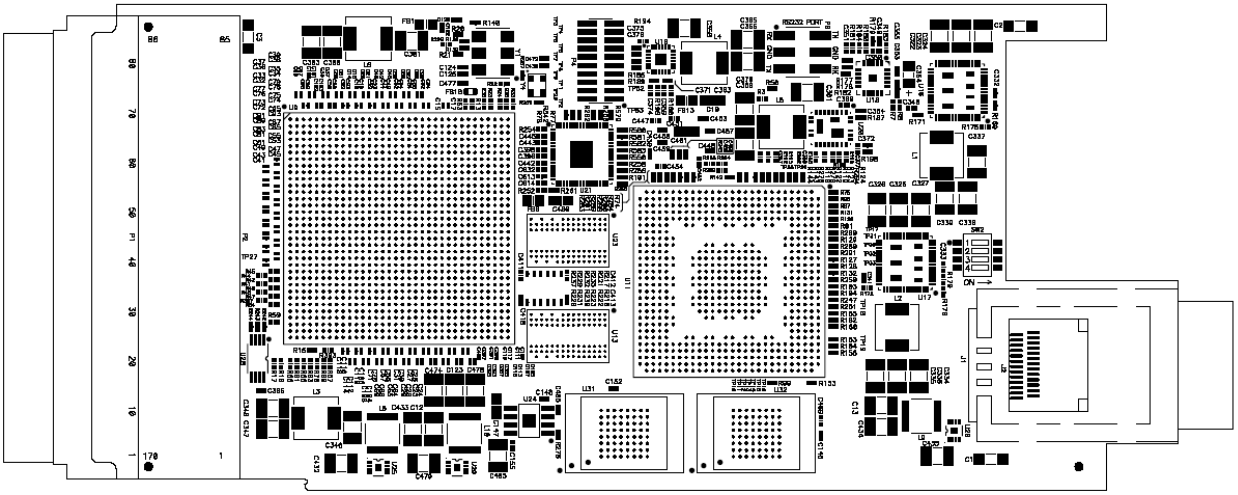

Figure 4: DA112 (10GbE Fabric) component side layout

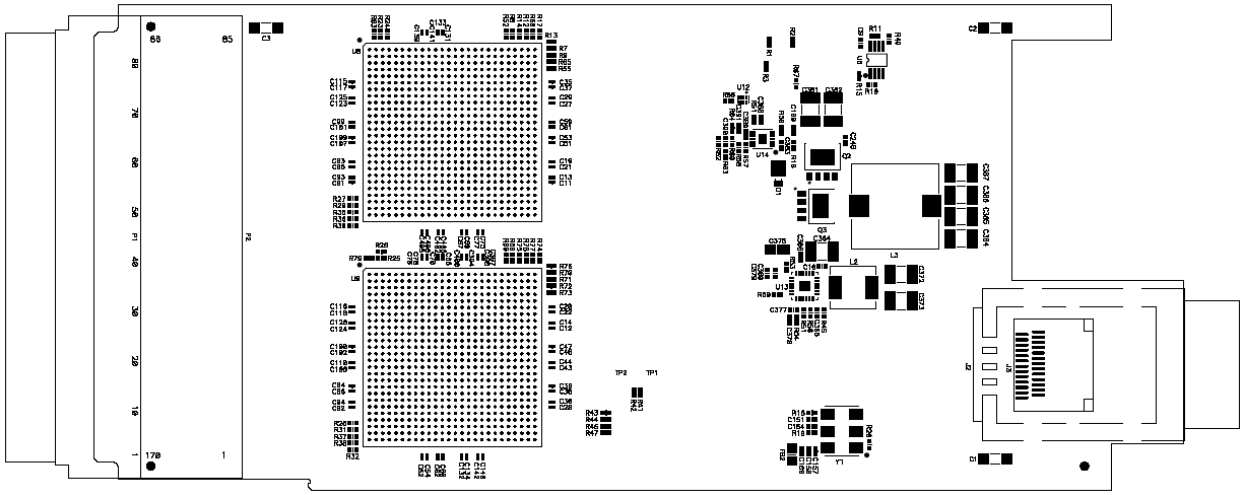

Figure 5: DA113 (SRIO Fabric) component side layout

2.2 Architectural Description

A block diagram for the UTC001 base board and VT002 daughter card is shown below:

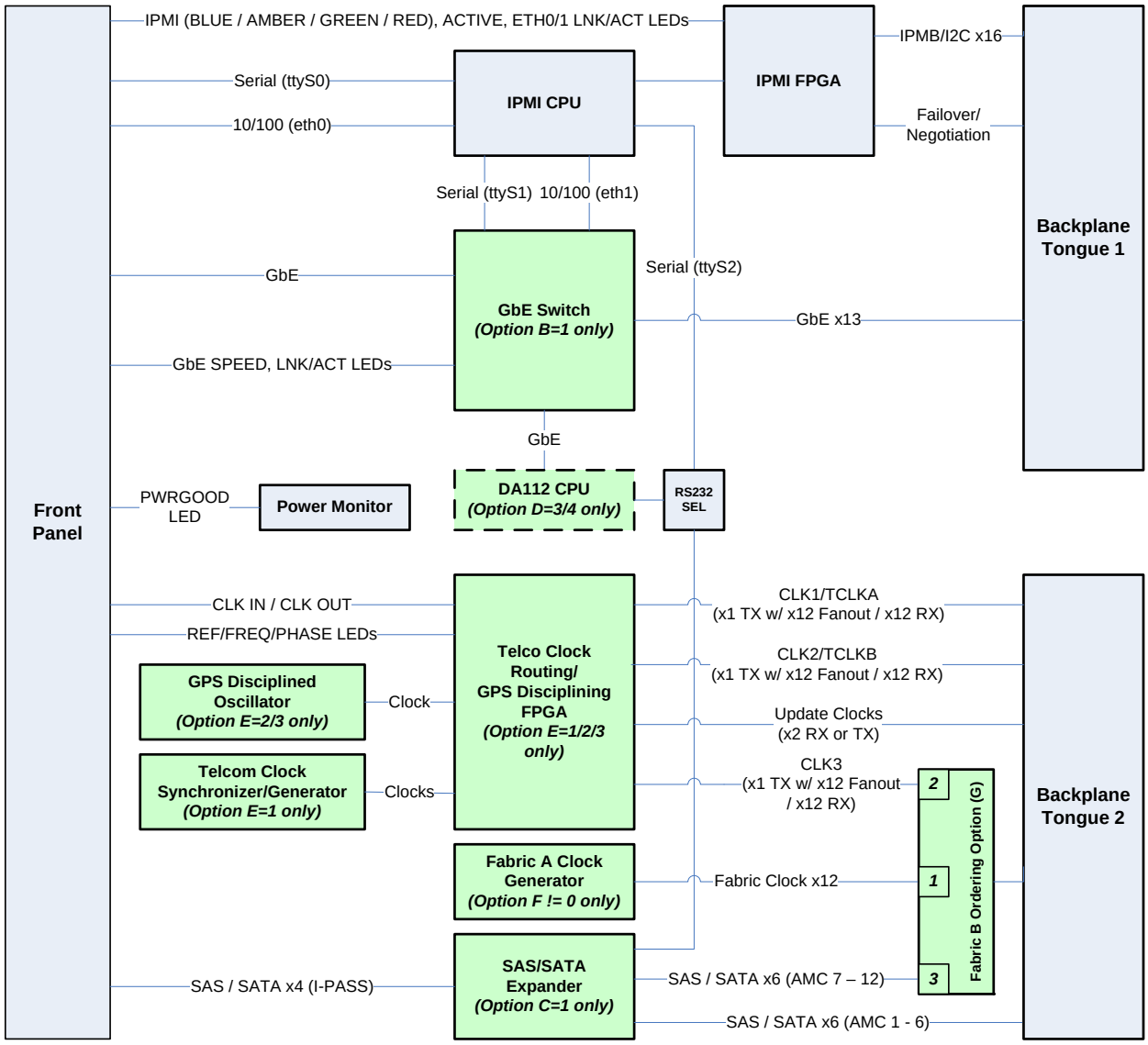

Figure 6: UTC001 base block diagram

2.3 IPMI Controller

At its core, the UTC001 module contains an IPMI Controller (VT002 board) made up of a 400 MHz CPU and custom FPGA for carrier/shelf management. This controller includes separate IPMB buses for Host, Local, IPMB-A, IPMB-B, CF-A, CF-B, and up to 12 AMC slots. Each IPMB bus has an associated 128-byte RX FIFO and 128-byte TX FIFO to provide improved parallelism and performance using CPU interrupt coalescing. The controller includes an integrated activation/failover arbiter at the hardware level for seamless failover between two UTC001 modules. The IPMI Controller provides a serial port on the front panel for gaining access to the Linux OS console. It also provides a 10/100 Ethernet port (eth0) to the front panel for out-of-band access and internally has a 10/100 Ethernet port (eth1) to the 1GbE switch for in-band access.

2.4 1GbE Layer 2 Managed Switch Option (B = 1)

An optional 1GbE switch is provided which includes an integrated 266 MHz CPU providing Layer 2 management. This switch connects to up to 12 AMC slots, a front panel RJ45, the VT002 internal port (eth1), and also has an update channel link to the second UTC001 when present. A serial port connection is present between the switch management CPU and the IPMI Controller CPU. However, the primary management for this switch is via a supplied web interface. Please do not use the serial port connection unless instructed by VadaTech.

The port configuration of the 1GbE switch is as follows:

Logical Port #	Port Description	Logical Port #	Port Description
1	AMC 1	9	AMC 9
2	AMC 2	10	AMC 10
3	AMC 3	11	AMC 11
4	AMC 4	12	AMC 12
5	AMC 5	13	VT002 (eth1)
6	AMC 6	14	Front Panel
7	AMC 7	15	MCH Daughtercard
8	AMC 8	16	MCH <-> MCH

Table 2: Port configuration of the 1GBE switch

2.5 SAS/SATA Expander Option (C = 1)

An optional SAS/SATA expander is available which includes an integrated CPU providing SAS management. This expander connects to up to 12 AMC slots (x1 links), a front panel I-PASS connector (x4 wide-link), and also has an update channel link (x1 link) to the second UTC001 when present. A serial port connection is present between the expander management CPU and the IPMI Controller CPU. Please do not use the serial port connection unless instructed by VadaTech. Ordering option 'G' affects which AMCs the SAS/SATA expander connects to. The following table shows the connectivity for each option:

Option 'G'	Selection Name	SAS/SATA AMC Connectivity
0	None	No AMC connections
1	Fabric clock shared with Fabric B	Connection to AMC Slots 1 – 6 only
2	Telcom clock shared with Fabric B	Connection to AMC Slots 1 – 6 only
3	No clocks – all Fabric B	Connection to all AMC Slots 1 – 12

Table 3: SAS/SATA connectivity options

The port configuration for the SAS/SATA Expander is as follows:

Physical Port #	Port Description	Physical Port #	Port Description
0	AMC 1	8	AMC 9
1	AMC 2	9	AMC 10
2	AMC 3	10	AMC 11
3	AMC 4	11	AMC 12
4	AMC 5	12	MCH <-> MCH
5	AMC 6	13 – 16	Front Panel (x4)
6	AMC 7	17	Top Board (currently unused)
7	AMC 8		

Table 4: SAS/SATA expander configuration

2.6 Fabric Clock Option (F != 0)

The base board also includes a 100 MHz PCIe clock generator option. This clock generator provides clocking to up to 12 AMC slots. It can be configured with Spread Spectrum Clocking (SSC) on or off and is required when SSC is desired for the PCIe fabric. Other types of fabric clock are possible; please contact VadaTech sales with your requirement.

Whenever the fabric clock option is selected, you should also select Option 'G' as '1' so that the fabric clock will be visible to the AMC slots. The connectivity for the fabric clock is shown below:

Option 'G'	Selection Name	Fabric Clock Connectivity
0	None	No AMC connections
1	Fabric clock shared with Fabric B	Connection to all AMC Slots 1 – 12
2	Telcom clock shared with Fabric B	No AMC connections
3	No clocks – all Fabric B	No AMC connections

Table 5: Fabric clock connectivity options

2.7 Telcom TCXO Clock Option (E = 1)

The base board includes two different options for Telco clocking. There is an ordering option 'E=1' for Telcom clock synchronization/generation which supports many telecom standards such as T1/E1/SDH with an on-board Stratum 3 oscillator and automatic failover/holdover.

The Telcom synchronizer supports the following clock frequencies:

2 kHz, 8 kHz, 1.544 MHz, 2.048 MHz, 8.192 MHz, 16.384 MHz, and 19.44 MHz

The Telcom clock generator provides the following clock frequencies:

1.544 MHz (T1/DS1), 2.048 MHz (E1), 3.088 MHz, 16.384 MHz, and 19.44 MHz (SDH), and either 4.096 MHz and 8.192 MHz or 32.768 MHz and 65.536 MHz, and a choice of 6.312 MHz (DS2), 8.448 MHz (E2), 44.736 MHz (DS3), or 34.368 MHz (E3). It also provides 5 styles of 8 kHz framing pulses and a 2 kHz multi-frame pulse.

The REF, FREQ, and PHASE LEDs are updated based on the Telcom synchronizer status. A complete description of the Telcom/GPS clocking functionality of the UTC001 can be found in the UTC001 and VT850 Telco / GPS Clock Configuration Guide document.

2.8 GPS VCTCXO Clock Option (E = 2 or 3)

The other Telcom clocking option is a GPS disciplined oscillator solution. The GPS disciplined oscillator takes in a 1 Pulse-Per-Second (1PPS) reference from a GPS receiver (sold separately) and disciplines a Stratum 3 10 MHz or 30.72 MHz oscillator depending on the ordering option and outputs this frequency as well as a regenerated 1PPS signal which is phase aligned to the reference. Automatic holdover mode is activated any time the reference is lost. The regenerated 1PPS pulse continues to be generated even during holdover when the reference pulse would otherwise be missing.

The REF, FREQ, and PHASE LEDs are updated based on the GPS disciplining algorithm's status. A complete description of the Telcom/GPS clocking functionality of the UTC001 can be found in the UTC001 and VT850 Telco / GPS Clock Configuration Guide document.

2.9 Telco Clock Routing Support w/ Telcom/GPS Clock Options (E = 1, 2, or 3)

Both of the Telcom ordering option types (when present) include clock routing support based on the AMC.0 v1 and AMC.0 v2 specifications. The clock router can provide M-LVDS clocking signals to up to 12 AMC slots on CLK1/TCLKA, CLK2/TCLKB, or CLK3. It also provides a front panel SMA clock output, two update channel clock paths to the second UTC001 when present, and internal on-board destinations such as the Telcom clock synchronizer/GPS reference 1PPS. The clock router can be configured to select the sources of these clocks from any of the 12 AMC slots on CLK1/TCLKA, CLK2/TCLKB, or CLK3, from the front panel SMB input, from one of the update clock paths from the second UTC001 when present, or from internal on-board sources such as the Telcom clock generator/GPS oscillator/1PPS.

Note that AMC TCLKC and TCLKD were added in the AMC.0 v2 specification after the uTCA specification was developed and therefore they are not supported by the uTCA MCH pin-out. Therefore these clocks are not supported by the UTC001. If you require routing of these clocks please consider the VadaTech VT850 1U chassis which includes AMC TCLKC and TCLKD routing capability. The ordering option 'G' affects how the CLK3 channels will connect to the AMC slots.

The following table shows the connectivity for each option:

Option 'G'	Selection Name	Telco CLK3 Connectivity (non-fabric usage)
0	None	No AMC connections
1	Fabric clock shared with Fabric B	No AMC connections
2	Telcom clock shared with Fabric B	Connection to all AMC Slots 1 – 12
3	No clocks – all Fabric B	No AMC connections

Table 6: Telco clock connectivity options

A complete description of the Telcom/GPS clocking functionality of the UTC001 can be found in the UTC001 and VT850 Telco / GPS Clock Configuration Guide document.

2.10 PCIe Fabric Option – DA111 (D = 1)

The DA111 daughter card provides a PCIe Gen2 (2.5 GHz) x4 switching fabric on MCH Tongues 3 and 4. The PCIe switch has connections to up to 12 AMCs (x4 wide links with automatic x1 downshift) and a front panel I-PASS (x4 wide link) for chassis-to-chassis or PC-to-chassis expansion. The switch will automatically downshift to Gen1 (1.25 GHz) on a port-by-port basis depending on what is connected. The upstream (host) port is determined by E-Keying, and the AMC with this port is activated last so that all of the downstream devices are present prior to the host seeing the PCIe fabric.

When Spread Spectrum Clocking (SSC) is desired, option 'G' must be '1' and option 'F' must be '1' so that the AMCs will receive the same spread clock as the fabric.

The port configuration of the PCIe switch is as follows:

Physical Port #	Port Description
0 – 3	AMC 1 (x4)
4 – 7	AMC 2 or Front I-PASS (x4)
8 – 11	AMC 3 (x4)
12 – 15	AMC 4 (x4)
16 – 19	AMC 5 (x4)
20 - 23	AMC 6 (x4)
24 – 27	AMC 7 (x4)
28 – 31	AMC 8 (x4)
32 – 35	AMC 9 (x4)
36 – 39	AMC 10 (x4)
40 – 43	AMC 11 (x4)
44 - 47	AMC 12 (x4)

Table 7: PCIe configuration

NOTE: When the front panel connector is in selected for use AMC slot 2 will not be connected to the fabric due to port sharing on the switch. This selection is made by software.

2.11 10GbE Fabric Option – DA112 (D = 3 or 4)

The DA112 daughter card provides a 10GbE (XAUI) switching fabric on MCH Tongues 3 and 4. The DA112 includes an on-board 400 MHz management CPU which can run an optional Layer 3 (hybrid switch/router) management stack. Ordering option 'D' must be '3' (managed) or '4' (unmanaged) to receive this functionality. The 10GbE switch connects to up to 12 AMC slots (XAUI), a front panel I-PASS connector (XAUI) for expansion, the on-board management CPU (1GbE – eth0), and an update channel link (XAUI) to the second UTC001 when present. The management CPU also has a 1GbE (eth1) connection to the 1GbE switch on the base board. Therefore, routing or bridging is possible between the 10GbE segment and the 1GbE segment. The following block diagram shows the DA112 architecture:

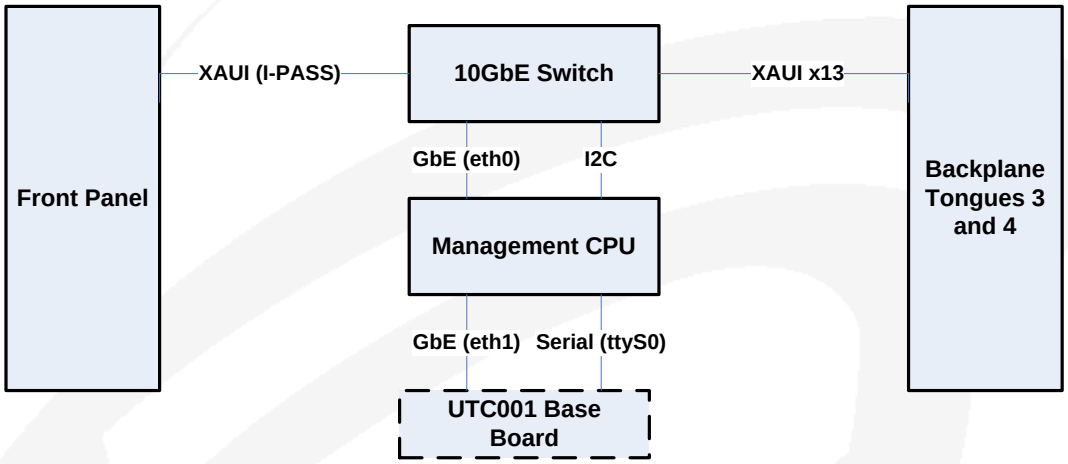

Figure 7: DA112 block diagram

Physical Port #	Port Description	Physical Port #	Port Description
0	AMC 3 (XAUI)	10	(no connect)
1	(no connect)	11	AMC 8 (XAUI)
2	(no connect)	12	AMC 11 (XAUI)
3	AMC 9 (XAUI)	13	AMC 6 (XAUI)
4	AMC 10 (XAUI)	14	Front I-PASS (XAUI)
5	(no connect)	15	AMC 1 (XAUI)
6	(no connect)	16	AMC 5 (XAUI)
7	AMC 2 (XAUI)	17	AMC 12 (XAUI)
8	AMC 4 (XAUI)	18	MCH <-> MCH (XAUI)
9	Management CPU (1GbE – eth0)	19	AMC 7 (XAUI)

Table 8: 10GBE switch port configuration

2.12 SRIO Fabric Option - DA113 (D = 2)

The DA113 daughter card provides SRIO x4 switching fabric on MCH Tongues 3 and 4. Ordering option 'D' must be '3' to receive this functionality. The SRIO switch connects to up to 12 AMCs (x4) as well as a front I-PASS (x4) connector for expansion. The SRIO fabric is made up of two on-board switches, one of which handles AMC slots 1-6 and other of which handles slots 7-12 and the front port. The two switches are cross-connected using three x4 links.

The port configuration of the two switches is shown below:

Switch #	Physical Port #	Port Description
0	0 – 3	AMC 6 (x4)
0	4 – 7	AMC 5 (x4)
0	8 – 11	AMC 4 (x4)
0	12 – 15, 20 - 23, 28 - 31	SWITCH <-> SWITCH (3 x4)
0	16 – 19	AMC 1 (x4)
0	24 – 27	AMC 3 (x4)
0	32 – 35	(No connect)
0	36 – 39	AMC 2 (x4)
1	0 – 3	AMC 10 (x4)
1	4 – 7	AMC 9 (x4)
1	8 – 11	AMC 8 (x4)
1	12 – 15	AMC 7 (x4)
1	16 – 19	AMC 11 (x4)
1	20 – 23, 28 – 35	SWITCH <-> SWITCH (3 x4)
1	24 – 27	Front I-PASS (x4)
1	36 – 39	AMC 12 (x4)

Table 9: SRIO x4 switching fabric port configuration

2.13 Front Panel

The front panel of the UTC001 consists of the MCH hot-swap handle, IPMI LEDs, RJ45 for IPMI Serial Console port, RJ45 for IPMI 10/100 Ethernet port, RJ-45 for the GbE Switch, I-PASS for SAS/SATA expansion, I-PASS for PCIe or SRIO or 10GbE expansion, SMA clock in/out for Telcom clocking, and LEDs. The figures below show the front panel connections with callouts to help clarify the purpose of connectors/LEDs:

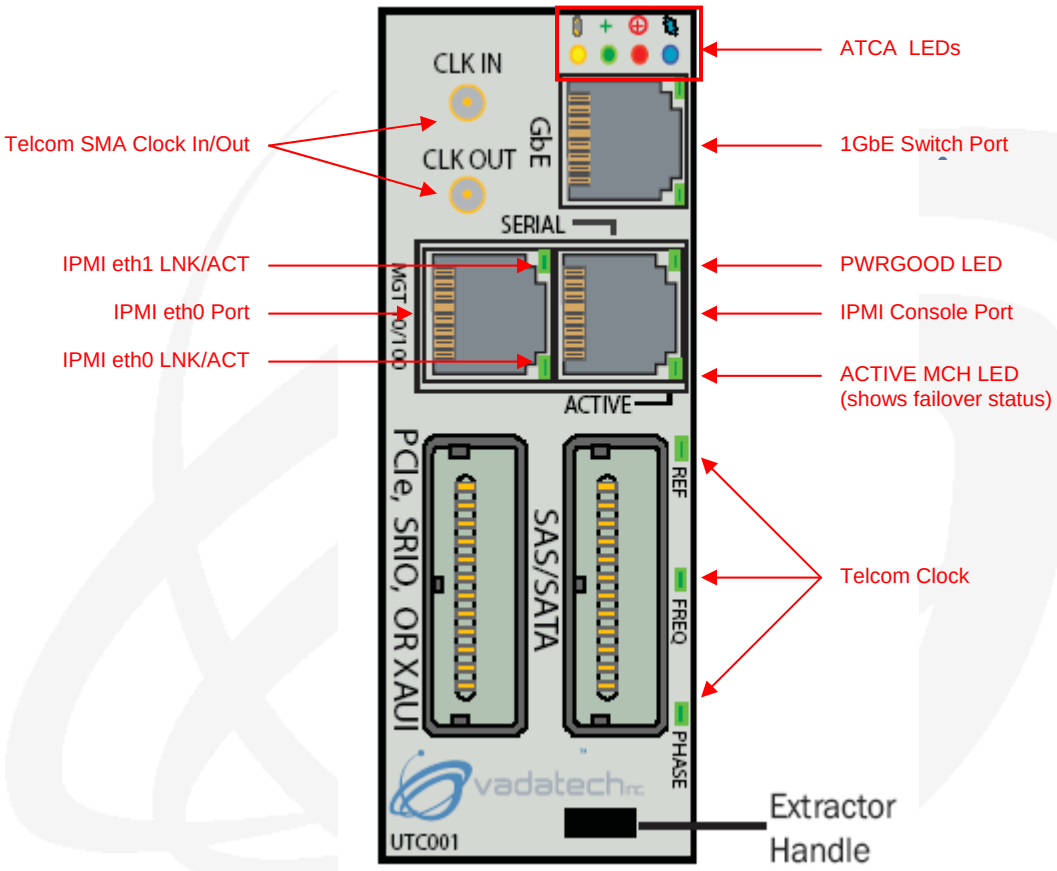

Figure 8: UTC001 front panel

2.14 The ATCA Management LEDs

Per the µTCA MCH specification there are four LEDs that are opposite the handle and are controlled by the IPMI management controller. These four ATCA LEDs are colored Blue, Green, Amber/Yellow and Red. The Blue indicates the hot-swap state of the MCH. Initially, the Blue LED is on. When the MCH handle is closed upon insertion, and acknowledge by the carrier, the blue LED will blink (long blink). When the MCH has been powered up by the carrier, the blue LED will go off indicating that the MCH is fully operational in the system. If the AMC handle is opened, starting a removal sequence, and acknowledged by the carrier the blue LED will blink (short blink) until the MCH has been completely powered down at which point the blue LED will be continuously lit. This indicates to the operator that it is safe to remove the MCH from the chassis.

Name	Color	Description
Hotswap	Blue	hotswap state, per PICMG AMC.0 and MicroTCA specifications
Error	Red	ON indicates failure has occurred on the UTC001 OFF indicates normal operation
Health	Green	ON indicates normal operation OFF indicates a failure has occurred on the UTC001
Application	Amber	is not currently being used

Table 10: UTC001 ATCA LEDs

2.15 Insertion/Removal Mechanism

The UTC001 is a hot-plugged FRU, which allows it to be inserted into the chassis while the system is up. The UTC001 could also be removed live from the system. The front panel handle is pulled outward to notify the hot removal. The blue light starts blinking, which during this time the module must not be removed. The IPMI Management controller notifies the carrier of the intention of removing the module. The solid Blue light is an indicator that it is safe to remove the Module.

For more information on UTC001 Hotswap States please refer to the UTC001 Management Software Reference Manual.

2.16 Port Pin-outs

The **MGT 10/100** port is pinned out in compliance with 100BASE-T.

The **GbE** port is pinned out in compliance with 1000BASE-T.

The **SERIAL** port is pinned out as follows:

Pin #	Pin Description
1	(no connect)
2	TX of IPMI Controller (RS232)
3	RX of IPMI Controller (RS232)
4	(no connect)
5	GND
6	(no connect)
7	(no connect)
8	(no connect)

Table 11: Serial port pin out

The CLK IN port accepts square or sine wave 3.3v LVCMOS signals. The CLK OUT port produces 3.3v LVCMOS square wave signals. Both ports are SMA format with the active signal on the center conductor and GND on the shield. A more complete description of these ports can be found in the UTC001 and VT850 Telco / GPS Clock Configuration Guide.

The SAS/SATA, PCIe, SRIO, and 10GbE (XAUI) expansion ports are pinned out as follows and carry the SERDES signals for the corresponding bus standard:

Pin #	Pin Description	Pin #	Pin Description
A1	GND	B1	GND
A2	RX0+	B2	TX0+
A3	RX0-	B3	TX0-
A4	GND	B4	GND
A5	RX1+	B5	TX1+
A6	RX1-	B6	TX1-
A7	GND	B7	GND
A8	RX2+	B8	TX2+
A9	RX2-	B9	TX2-
A10	GND	B10	GND
A11	RX3+	B11	TX3+
A12	RX3-	B12	TX3-
A13	GND	B13	GND

Table 12: Expansion ports pin out

2.17 Switch settings

There are a number of switch settings within the UTC001 module, however all of the switches are pre-configured during manufacturing and their settings should not be changed by the customer.

3 Software

Please refer to the UTC001 software manuals for complete description of the software behavior and user interfaces available for configuration and monitoring.

4 Specifications

The following table shows the recommended operating conditions for UTC001:

UTC001 Air Flow	400 LFM
Pay load power	Module option dependent (min 3W, max 35W)
IPMI Controller	0.2W
Operating Temperature	0° to +65° C with 400 LFM
Storage Temperature	-40° to +90° C
Relative Humidity	5 to 95 percent, non-condensing
Operating Altitude	10,000 ft
Non Operating Altitude	28,000 ft
Shock Operating	30Gs each axis
Vibration operating	1G, 5-500Hz each axis
Safety; Design to meet or exceed	UL 60950 3rd Ed.; CSA C22.2 No.60950-00; EN60950; IEC 60950-a
EMC; Design to meet or exceed	FCC 47 CFR Part 15, Class B; CE Mark to EN55022/EN55024
Warranty	2 year limited

Table 13: Specifications