VadaTech MicroTCA

# Telco / GPS Clock Configuration Guide

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# Revision History

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|---|---|---|
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| 2.1 | Added Clock Routing Only operating type to support front panel/backplane routing without Telco/GPS oscillator circuitry present. | 4/14/2009 |
| 2.2 | Added documentation of UTC002, VT851, VT852, and VT853. | 2/25/2010 |

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# 1 Overview

This document describes the Telco/GPS clocking option on the VadaTech UTC001/UTC002 MCH and VT850/VT851/VT852/VT853 1U chassis. The clocking for the 1U chassis is taken care of by the MCH-equivalent portion of the chassis mainboard. Therefore the term 'MCH' will be used throughout the remainder of this document to describe the clocking support on both the separate MCH products and the built-in MCH products.

## 1.1 Document References

- PICMG MicroTCA Specification
- PICMG Advanced Mezzanine Card Specification (v1 and v2 both apply)
- VadaTech MicroTCA MCH Getting Started Guide
- VadaTech UTC001 Hardware Reference Manual
- VadaTech UTC002 Hardware Reference Manual
- VadaTech VT850 Hardware Reference Manual
- VadaTech VT851 Hardware Reference Manual
- VadaTech VT852 Hardware Reference Manual
- VadaTech VT853 Hardware Reference Manual

## 1.2 Acronyms Used in this Document

| Acronym | Description |
|---|---|
| 1PPS | One Pulse Per Second |
| AMC | Advanced Mezzanine Card |
| CLK | Clock |
| DAC | Digital to Analog Converter |
| DC | Direct Current |
| E1 | E-carrier 1 |
| ESD | Electrostatic Discharge |
| FPGA | Field Programmable Gate Array |
| GPS | Global Positioning System |
| IPMI | Intelligent Platform Management Interface |
| kHz | Kilohertz |
| LED | Light Emitting Diode |
| LVCMOS | Low Voltage Complimentary Metal Oxide Semiconductor |
| M-LVDS | Multipoint Low Voltage Differential Signalling |
| MCH | MicroTCA Carrier Hub |
| MHz | Megahertz |
| ns | Nanoseconds |
| PCIe | Peripheral Component Interconnect Express |
| PDH | Plesiochronous Digital Heirarchy |
| PLL | Phase Locked Loop |
| PPM | Parts Per Million |
| PPS | *(See 1PPS)* |
| Rx | Receive |
| SAS | Serial Attached SCSI |
| SDH | Synchronous Digital Heirarchy |
| SMA | SubMiniature version A (connector) |
| SMB | SubMiniature version B (connector) |
| T1 | T-carrier 1 |
| TCVCXO | Temperature Compensated Voltage Controlled Crystal Oscillator |
| TCXO | Temperature Compensated Crystal Oscillator |
| Tx | Transmit |
| *u*TCA | Micro Telephony Computing Architecture |
| VCTCXO | *(see TCVCXO)* |

Table 1: Acronyms

# 2 Clocking Overview

The MCHs have ordering options for Telcom (20 MHz TCXO) and GPS (10 MHz or 30.72 MHz TCVCXO) clocking as well as an option for 'Clock Routing Only'. All of these options include equivalent clock routing and distribution support. However, the Telcom option comes with a sophisticated telecom PLL chip made by Zarlink while the GPS option includes a custom-designed GPS clock disciplining hardware/software solution. All of the related hardware and software is referred to as the VTCLOCK sub-system.

## 2.1 VTCLOCK Hardware Logical Diagram

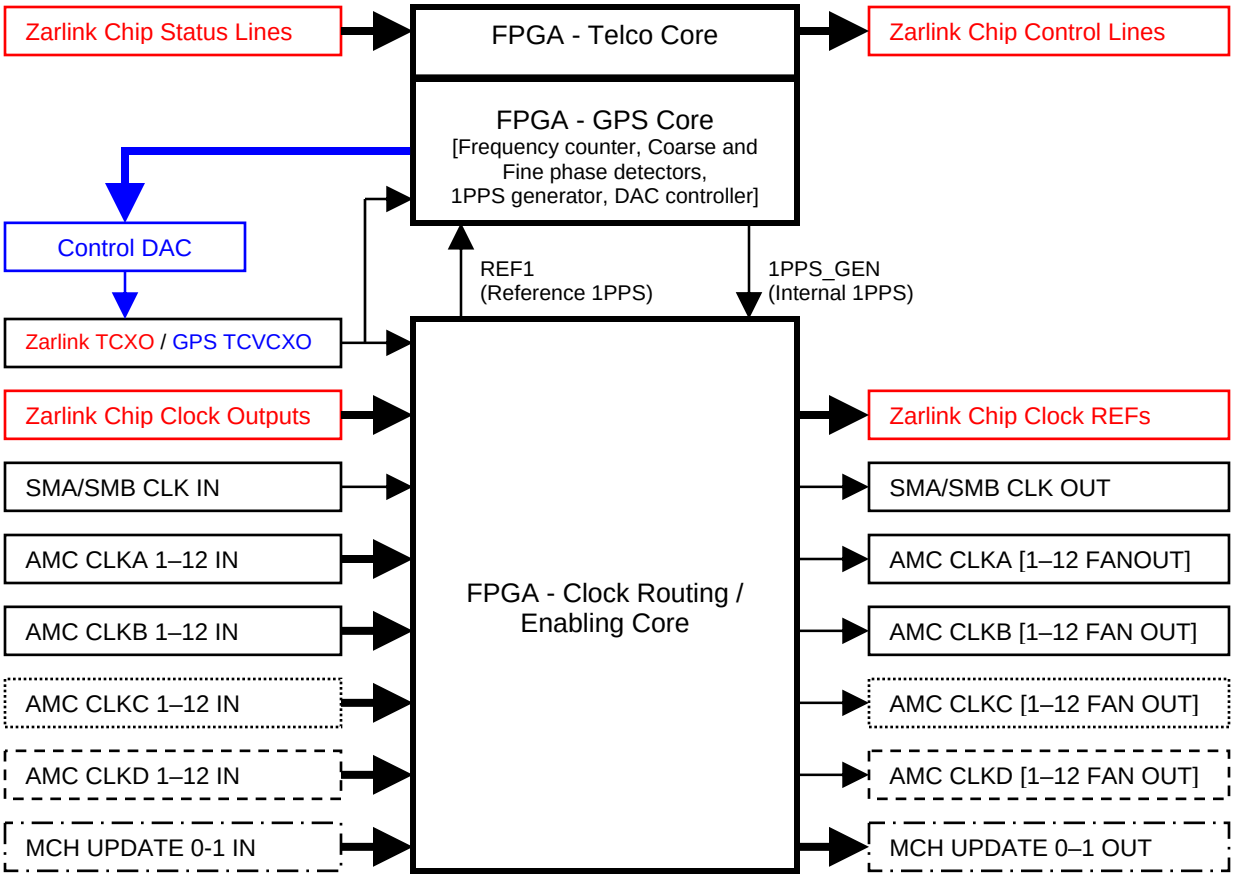


Figure 1: VTCLOCK Hardware Logical Diagram

**NOTES:**

- Wide arrows indicate buses containing multiple signals while narrow arrows are single signals.
- Portions present only with the Telcom TCXO ordering option are shown in red. Portions present only with the GPS TCVCXO ordering option are shown in blue. Portions present only with the 1U chassis or the standalone MCH Fabric B Telcom clock ordering option is shown with a dotted line. Portions present only with the 1U chassis are shown with a dashed line. Portions present only with the standalone MCH are shown with a dash-dot line.
- Receiver/transmitter enables are not shown but are present for any clock coming into or out of the MCH.
- Backplane clocks (labeled starting with AMC or MCH) all follow the M-LVDS standard.
- The MCH has an option for PCIe clocking but it is not a part of the VTCLOCK subsystem and is not the focus of this guide.

## 2.2 Resolving Differences in Clock Naming

The AMC v1, uTCA, and AMC v2 specifications differ in their handling and naming of the various backplane clocks. The VTCLOCK subsystem primarily uses AMC v2 naming, but makes some special provisions for uTCA. Although the naming is based on AMC v2, there is backward compatibility built in for AMC v1 clocking. AMC v2 and uTCA specifications recommend some directionality for the telecom clocks. However, the specifications don't make the directionality mandatory. **The VTCLOCK sub-system supports bi-directional clocking on all backplane clock channels for complete flexibility.** The AMC v2 and uTCA suggested clock directions are shown in the following tables merely as a guide. See **Appendix A: UTC001/UTC002 Clocking Pin-out** for a complete pin-out of the clocks on the backplane connector.

| VadaTech 1U Chassis (VTCLOCK) | AMC v1 Card | AMC v2 Card |
|---|---|---|
| CLKA (bi-dir) | CLK1 (bi-dir) | TCLKA (in) |
| CLKB (bi-dir) | CLK2 (bi-dir) | TCLKB (out) |
| PCIe Clock (out) | CLK3 (bi-dir) | FCLKA (in) |
| CLKC (bi-dir) | N/A | TCLKC (in) |
| CLKD (bi-dir) | N/A | TCLKD (out) |

Table 2: VadaTech 1U Chassis Clock Naming

| VadaTech Standalone MCH (VTCLOCK) | uTCA Backplane | AMC v1 Card | AMC v2 Card |
|---|---|---|---|
| CLKA (bi-dir) | CLK1 | CLK1 (bi-dir) | TCLKA (in) |
| CLKB (bi-dir) | CLK2 | CLK2 (bi-dir) | TCLKB (out) |
| CLKC (bi-dir – option) | CLK3 | CLK3 (bi-dir) | FCLKA (in) |
| N/A | N/A | N/A | TCLKC (in) |
| N/A | N/A | N/A | TCLKD (out) |
| MCH_UPDATE0 (bi-dir) | CLK1_Tx | N/A | N/A |
| MCH_UPDATE1 (bi-dir) | CLK1_Rx | N/A | N/A |

Table 3: VadaTech Standalone MCH (Non-Redundant Backplane) Clock Naming

The CLKC channels are only routed between the backplane connector and the VTCLOCK subsystem when the 'Fabric C Ports Configuration' ordering option is 'Telcom clock shared with Fabric B (SAS)'.

| MCH A (VTCLOCK) | MCH B (VTCLOCK) | uTCA Backplane | AMC v1 Card | AMC v2 Card |
|---|---|---|---|---|
| CLKA (out) | N/A | CLK1A | CLK1 (bi-dir) | TCLKA (in) |
| CLKB (in) | CLKB (in) | CLK2 | CLK2 (bi-dir) | TCLKB (out) |
| N/A | CLKA (out) | CLK1B | CLK3 (bi-dir) | FCLKA (in) |
| N/A | N/A | N/A | N/A | TCLKC (in) |
| N/A | N/A | N/A | N/A | TCLKD (out) |
| MCH_UPDATE0 (out) | MCH_UPDATE0 (in) | CLK1_Tx (crossover) | N/A | N/A |
| MCH_UPDATE1 (in) | MCH_UPDATE1 (out) | CLK1_Rx (crossover) | N/A | N/A |

Table 4: VadaTech Standalone MCH (Redundant Backplane) Clock Naming

The CLKC channels on the MCH are not used with this type of backplane since the backplane does not route them in favor of routing a redundant CLK1 from the other MCH to the AMCs.

# 3 Front Panel Input / Output and Indicators

The front panel of the MCH or 1U chassis which supports the VTCLOCK subsystem will include:

- An SMA or SMB clock input named CLK IN or REF IN (this signal is named CLOCK_IN in the VTCLOCK subsystem)
- An SMA or SMB clock output named CLK OUT or REF OUT (this signal is named CLOCK_OUT in the VTCLOCK subsystem)
- A Clock Reference Good indicator labeled REF or REF GOOD
- A Frequency Locked indicator labeled FREQ or FREQ LOCK
- A Phase Locked indicator labeled PHASE or PHASE LOCK

Please refer to the appropriate hardware reference manual for details on the location of these items on the front panel, electrical compatibility, etc.

Note that the LEDs may not be present for the 'Clock Routing Only' option since they are unused in this configuration.

## 3.1 LED Indicators

The LED indicators behave as follows for the **Telcom TCXO** ordering option:

| | REF GOOD | FREQ LOCK | PHASE LOCK |
|---|---|---|---|
| OFF | No valid reference | Not locked | |
| ALTERNATING BLINK | N/A | Holdover | |
| ON | Reference valid | Locked | |

Table 5: Telcom TCXO LEDs

The LED indicators behave as follows for the **GPS VCTCXO** ordering option:

| | REF GOOD | FREQ LOCK | PHASE LOCK |
|---|---|---|---|
| OFF | No valid reference | Not locked | Not locked |
| RAPID BLINK | N/A | | Slewing generated 1PPS |
| BLINK | Validating reference | Validating frequency | Validating phase |
| ALTERNATING BLINK | N/A | Holdover | |
| ON | Reference valid | Frequency locked | Phase locked |

Table 6: GPS VCTCXO LEDs

**NOTE:** GPS Disciplined mode shown, in GPS Freerun mode there is no reference to lock to so the LEDs simply display a moving pattern to show that the system is operating. Also, in the Clock Routing Only mode, the LEDs may or may not be present and if they are they will be OFF.

# 4 VTCLOCK Software

The VTCLOCK software consists of a device driver, tool/daemon executable, and a configuration file; all found on the MCH's VT002 IPMI daughter card. The driver and daemon are factory configured to automatically load at VT002 boot-time. The daemon will load the configuration file when it starts up and also whenever it is commanded to reload it.

The diagram below shows an overview of how the software fits into the overall VTCLOCK sub-system.

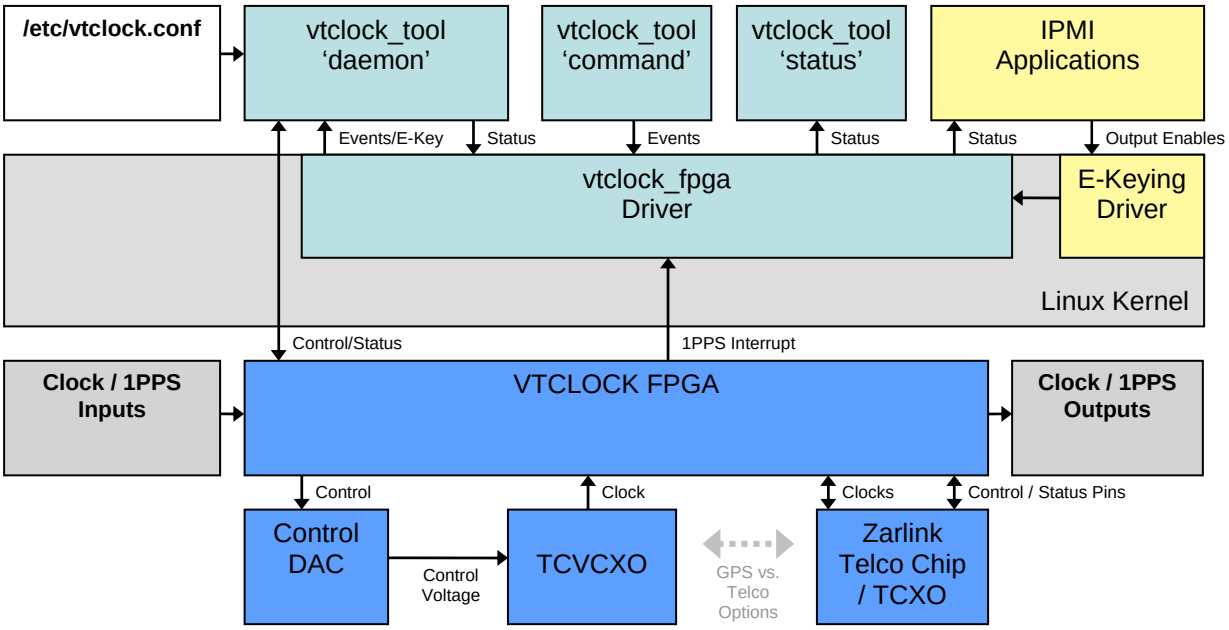


Figure 2: VTCLOCK software architecture

## 4.1 vtclock_tool (vc)

The **vtclock_tool** application runs on the VT002 board and provides various options for configuring and monitoring the VTCLOCK sub-system. These options are described below.

NOTE: **vc** is defined as an alias for **vtclock_tool**.

### 4.1.1 vc detect

Usage: **vc detect**

This command prints the version numbers of the tool, driver, and FPGA as well as the Telcom vs. GPS ordering option and various internal FPGA capability flags.

### 4.1.2 vc status

Usage: **vc status [monitor]**

This command prints the current operating status of the VTCLOCK sub-system. The status includes the following items in all operating modes:

| | |
|---|---|
| **REFGOOD** | *(YES/NO)* |
| **FREQLOCK** | *(YES/NO)* |
| **PHASELOCK** | *(YES/NO)* |
| **HOLDOVER** | *(YES/NO)* |
| **TX ENABLES CLKA** | *(unsigned short hexadecimal – valid bits are 13:0)* |
| **TX ENABLES CLKB** | *(unsigned short hexadecimal – valid bits are 11:0)* |
| **TX ENABLES CLKC** | *(unsigned short hexadecimal – valid bits are 11:0)* |
| **TX ENABLES CLKD** | *(unsigned short hexadecimal – valid bits are 11:0)* |

NOTE: MCH UPDATE 0 and MCH UPDATE 1 enables are reported as CLKA bit 12 and bit 13 respectively since this is how they are organized in the hardware.

When in Telco operating mode the following additional items are displayed:

| | |
|---|---|
| **TELCO REFSEL** | *(1, 2, or 3 - as selected by the Zarlink chip in Automatic mode or the conf file otherwise)* |
| **TELCO REFGOOD0** | *(YES/NO)* |
| **TELCO REFGOOD1** | *(YES/NO)* |
| **TELCO REFGOOD2** | *(YES/NO)* |

If the additional **monitor** argument is provided then the tool will enter an event monitoring loop and report time-stamped status information any time it is notified of a change by the device driver.

### 4.1.3 vc command

Usage: **vc command <cmd>**

| Cmd Argument | Description |
|---|---|
| **reload** | Re-load the configuration file and re-initialize the daemon control/status monitoring loop |
| **stop** | Stop the daemon *(not recommended)* |
| **info** | Switch to info log level |
| **detail** | Switch to detail log level |
| **verbose** | Switch to verbose log level |
| **data_file_on** | Turn data file recording on or rotate the file if it is already on |
| **data_file_off** | Turn data file recording off |

Table 7: vc command arguments

The **vc command reload** command allows the customer to send a **reload** event to the daemon after the configuration file has been modified. This will cause the daemon to reload the file, apply the new settings, and then re-enter its control/status monitoring loop with minimal disruption to the current system operation.

However, if any change is made to the 'Clock Routing' portion of the configuration file it is recommended that the system be power-cycled. This will ensure that the system-wide Clock E-Keying mechanism will remain in sync with the VTCLOCK subsystem's clock routing. Other changes such as to the 'Telco', 'GPS', or 'Clock Enables' section may be activated with **vc command reload** to minimize system disruption.

NOTE: The command events other than **reload** are for use during development testing and are not intended for customer use. *It is not recommended that the daemon be stopped since this can cause disruption to the system and loss of important run-time information.*

### 4.1.4 vc load

Usage: **vc load <bit_file>**

This command loads the VTCLOCK FPGA image and sets the appropriate pin multiplexing option based on the board the FPGA is residing on. This step is performed automatically during the VT002 boot sequence.

NOTE: This is an infrastructure support command and is not intended to be used by the customer.

### 4.1.5 vc dump / regs / sig_test / scratch_test / write

Usage: `vc dump [alt]`
`vc regs [snap]`
`vc sig_test`
`vc scratch_test`
`vc write <addr> <bytes>`

These commands are for development / manufacturing testing. They are not intended to be used by the customer.

**WARNING:** The **`vc regs snap`** and **`vc write`** commands may cause mis-operation if issued while the daemon is running in the background.

### 4.1.6 vc daemon

Usage: `vc daemon <args>`

| Daemon args | Description |
|---|---|
| `-r <val>` | Use real-time scheduling policy with priority **`val`** (1-99) |
| `-f <conf_file>` | Use the specified configuration file (defaults to **`/etc/vtclock.conf`** otherwise) |
| `-d <info\|detail\|verbose>` | Specify the starting debug level (defaults to info otherwise) |
| `-l` | Turn on data file recording from the start |
| `-x <host> <port>` | Send data file entries to network server instead of local file |
| `-n` | Do not daemonize, foreground execution only |
| `-t` | Test mode (random DAC setting / random 1PPS phase at startup) |
| `-t0` | Test mode (minimum DAC setting / random 1PPS phase at startup) |
| `-t1` | Test mode (maximum DAC setting / random 1PPS phase at startup) |

Table 8: vc daemon arguments

The daemon typically executes in the background and is started automatically at VT002 boot-time. It first reads the configuration file and applies the settings, then it enters a mode-specific monitoring/control loop depending on the particular operating mode (Telco / GPS Freerun / GPS Disciplined / Routing Only). The daemon controls the front panel LEDs, reports status to the driver (see vc status), and logs status changes to **`/var/log/messages`**.

The customer may use the vc command option described earlier to control the daemon during execution.

**NOTE:** The proper options for daemon startup have been provided in the VT002 startup scripts. The other available options are for development testing purposes only and are not intended to be used by the customer.

## 4.2 VTCLOCK Configuration File

The VTCLOCK configuration file is found on the VT002 as **`/etc/vtclock.conf`**. This file is heavily commented to assist you during configuration. The file is loaded whenever the **`vtclock_tool daemon`** starts or whenever the **`vtclock_tool command reload`** command is issued.

The configuration file includes the following sections which are described in the remainder of this guide:

- Top Level
- GPS
- Telco
- Clock Routing
- Clock Enables

### 4.2.1 Top Level Configuration Option

The top level configuration section affects all operating modes.

#### 4.2.1.1 TCXO_FREQ – TCXO/TCVCXO Frequency

The desired TCXO frequency is important to the GPS disciplined mode in that this is the exact frequency that it will discipline the oscillator to output. This option will usually be set to **`READ_SWITCHES`** which instructs the software to read the frequency of the oscillator from factory configuration switches which are set during the manufacturing process. The switches are set on Standalone MCH SW1 or 1U Chassis SW4 as follows:

| | 1 | 2 | 3 | 4 |
|---|---|---|---|---|
| 10.00 MHz | X | X | OFF | OFF |
| 20.00 MHz | X | X | OFF | ON |
| 30.72 MHz | X | X | ON | OFF |
| NONE (Clock Routing Only) | X | X | ON | ON |

Table 9: TCXO Frequency Switch Settings

NOTE: The 'X's indicate that the specified switch is not a part of the setting and should be left as it was originally configured.

If some non-standard frequency crystal is mounted, then the switches cannot be used and instead a frequency in the range of 8000000 to 52000000 may be specified in the configuration file.

EXAMPLE CONFIGURATION FILE ENTRY:

```
TCXO_FREQ=READ_SWITCHES
```

This tells the software to read the hardware switches to determine the oscillator frequency.

### 4.2.2 Clock Routing

The VTCLOCK FPGA contains a routing matrix which is used in any of the operating modes to route clocks from one place to another. The routing is target-centric meaning that there are fixed destinations and the clock source routed *to* that target is specified in the configuration file. It supports *up to* 65 unique sources for each of the 11 targets; with 661 total unique routes. The unsupported routes are only those that provide no value; such as routing a Zarlink output to one of its reference inputs. A given clock target can only have one clock source, but a given clock source can be used to feed multiple clock targets.

The following table details the routing capabilities of the VTCLOCK FPGA. Sources (inputs) are listed along the top and targets (outputs) are listed along the side:

| Target (Output) | Disabled | Clock In (SMA/SMB) | Generated 1PPS | TCXO / TCVCXO | AMC A1 – A12 | AMC B1 – B12 | AMC C1 – C12 | AMC D1 – D12 | MCH Update 0 | MCH Update 1 | Zarlink CLK2.048 | Zarlink CLK4.096/65.536 | Zarlink CLK8.192/32.768 | Zarlink CLK16.384 | Zarlink F4/F65 | Zarlink F8/F32 | Zarlink F16 | Zarlink CLK1.544 | Zarlink CLK3.088 | Zarlink CLK19.44 | Zarlink F2K | Zarlink CLK6.312/8.448/34.368/44.736 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Clock Out (SMA/SMB) | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ |
| REF0 | ✔ | ✔ | | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | | | | | | | | | | | | |
| REF1 / 1PPS Reference | ✔ | ✔ | | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | | | | | | | | | | | | |
| REF2 | ✔ | ✔ | | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | | | | | | | | | | | | |
| REF2 FrameSync | ✔ | ✔ | | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | | | | | | | | | | | | |
| CLKA | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ |
| CLKB | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ |
| CLKC | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ |
| CLKD | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ |
| MCH Update 0 | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ |
| MCH Update 1 | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ |

Table 10: VTCLOCK FPGA Clock Routing Capability

NOTE: This table follows the VTCLOCK subsystem naming convention. Please refer to the Resolving Differences in Clock Naming section to see the backplane or AMC equivalent clock name for your particular configuration.

The REFx clocks go to the Zarlink chip and provide its reference(s). As a special case, when the GPS VCTCXO ordering option is used, REF1 instead specifies the source of the GPS reference 1PPS signal.

You will note that only one clock source can be specified for each of CLKA, CLKB, CLKC, and CLKD. The FPGA outputs only 4 of these clocks (A, B, C, D) whereas it takes in 12 * 4 = 48 of these clocks (A1-12, B1-12, C1-12, D1-12). The 4 outputs are fanned out to become 48 outputs by M-LVDS clock transceivers as point-to-point clocks to the AMCs. But all A output clocks must share the same source, all B output clocks must share the same source, etc.

The MCH Update clocks are for use with two MCH's in a redundant configuration. These channels can be used to forward clocks between the MCH's for slaving/redundancy. Due to backplane crossover, the MCH Update 0 on one MCH connects to the MCH Update 1 on the other MCH and vice-versa. These are general purpose clock routes available to be used for the specific needs of the customer's system design.

#### 4.2.2.1 Clock Routing Configuration Options

**IMPORTANT:** ***By default all clock routes are disabled in the configuration file*** *since the desired routing is not known at the time of manufacture. The customer must configure the clock routing prior to using the VTCLOCK subsystem, otherwise no clocks will come out.*

All of the configuration options in this section use a common set of clock source names. The available names are as follows:

| Source Name | Description | UTC001 | VT850 | Fabric B option (UTC001 Req'd) | Telcom TCXO option (Req'd) |
|---|---|---|---|---|---|
| **DISABLED** | From fixed logic level '0' | ✔ | ✔ | | |
| **CLOCK_IN** | From front panel SMA/SMB clock input | ✔ | ✔ | | |
| **1PPS_GEN** | From internal GPS block's 1PPS generator | ✔ | ✔ | | |
| **TCXO** | From the TCXO/TCVCXO | ✔ | ✔ | | |
| **AMC_A1 – AMC_A12** | From AMC slot X's CLKA | ✔ | ✔ | | |
| **AMC_B1 – AMC_B12** | From AMC slot X's CLKB | ✔ | ✔ | | |
| **AMC_C1 – AMC_C12** | From AMC slot X's CLKC | ✔ | ✔ | ✔ | |
| **AMC_D1 – AMC_D12** | From AMC slot X's CLKD | | ✔ | | |
| **MCH_UPDATE0** | From the other MCH on channel 0 | ✔ | | | |
| **MCH_UPDATE1** | From the other MCH on channel 1 | ✔ | | | |
| **CLK1.544** | From Zarlink 1.544 MHz | ✔ | ✔ | | ✔ |
| **CLK2.048** | From Zarlink 2.048 MHz | ✔ | ✔ | | ✔ |
| **CLK3.088** | From Zarlink 3.088 MHz | ✔ | ✔ | | ✔ |
| **CLK4.096** | From Zarlink 4.096/65.536 MHz | ✔ | ✔ | | ✔ |
| **CLK6.312** | From Zarlink 6.312/8.448/34.358/44.736 MHz | ✔ | ✔ | | ✔ |
| **CLK8.192** | From Zarlink 8.192/32.768 MHz | ✔ | ✔ | | ✔ |
| **CLK16.384** | From Zarlink 16.384 | ✔ | ✔ | | ✔ |
| **CLK19.44** | From Zarlink 19.44 MHz | ✔ | ✔ | | ✔ |
| **F4** | From Zarlink F4/F65 | ✔ | ✔ | | ✔ |
| **F8** | From Zarlink F8/F32 | ✔ | ✔ | | ✔ |
| **F16** | From Zarlink F16 | ✔ | ✔ | | ✔ |
| **F2K** | From Zarlink F2K | ✔ | ✔ | | ✔ |

Table 11: Clock Routing Configuration Settings

**NOTE:** This table follows the VTCLOCK subsystem naming convention. Please refer to Section 2.2 to see the backplane or AMC equivalent clock name for your particular configuration.

Available configuration options (routing targets) are:

| Option Name | Description | UTC001 | VT850 | Fabric B option (UTC001 Req'd) | Telcom TCXO option (Req'd) |
|---|---|---|---|---|---|
| **ROUTE_CLOCK_OUT_FROM** | Specify Front panel output - SMA/SMB's source | ✔ | ✔ | | |
| **ROUTE_REF0_FROM** | Specify Zarlink input - REF0's source | ✔ | ✔ | | ✔ |
| **ROUTE_REF1_FROM** | Specify (Zarlink input - REF1) or GPS block - Reference 1PPS's source | ✔ | ✔ | | ( ✔ ) |
| **ROUTE_REF2_FROM** | Specify Zarlink input - REF2's source | ✔ | ✔ | | ✔ |
| **ROUTE_REF2_FRAME_SYNC_FROM** | Specify Zarlink input - REF2 Frame Sync's source | ✔ | ✔ | | ✔ |
| **ROUTE_CLKA_FROM** | Specify Backplane output - AMC CLKA's source | ✔ | ✔ | | |
| **ROUTE_CLKB_FROM** | Specify Backplane output - AMC CLKB's source | ✔ | ✔ | | |
| **ROUTE_CLKC_FROM** | Specify Backplane output - AMC CLKC's source | ✔ | ✔ | ✔ | |
| **ROUTE_CLKD_FROM** | Specify Backplane output - AMC CLKD's source | | ✔ | | |
| **ROUTE_MCH_UPDATE0_FROM** | Specify Backplane output - Other MCH on update channel 0's source | ✔ | | | |
| **ROUTE_MCH_UPDATE1_FROM** | Specify Backplane output – Other MCH on update channel 1's source | ✔ | | | |

Table 12: Clock Routing Configuration Items

NOTE: This table follows the VTCLOCK subsystem naming convention. Please refer to section 2.2 to see the backplane or AMC equivalent clock name for your particular configuration.

Particular attention should be paid to the ROUTE_REF1_FROM option since this clock routing target is used in both the Telcom and GPS ordering options whereas the other REFx options are only for Telcom. When the GPS ordering option is used, the REF1 target routes the reference 1PPS signal into the FPGA's GPS core. Routing this reference 1PPS signal is ***required*** for GPS Disciplined operation.

EXAMPLE CONFIGURATION FILE ENTRY:

```
ROUTE_REF1_FROM=CLOCK_IN
```

This routes the front panel clock input to the Zarlink REF1 input or the GPS Reference 1PPS input.

### 4.2.3 Clock Input/Output Enables and Clock E-Keying

Clock receivers are enabled automatically whenever a given clock is named as the source of a clock route. Clock transmitters, however, may be enabled in two different ways. By default the IPMI Clock E-Keying mechanism from the AMC v2 specification will attempt to match up on-board clocks with AMC clocks and enable the on-board clock transmitters as appropriate. However, since many AMCs still follow the AMC v1 specification which did not have Clock E-Keying or they may not implement Clock E-Keying in a compatible manner, the VTCLOCK subsystem provides options for forcing a clock transmitter to be enabled outside of the E-Keying framework.

#### 4.2.3.1 Clock Enables Configuration Options

All of the configuration options in this section use common settings. The available settings are as follows:

| Setting | Description |
|---|---|
| **AUTO** | Enabled by Clock E-Keying else disabled |
| **ON** | Force enabled regardless of Clock E-Keying |

Table 13: Clock Enables Configuration Settings

Available clock enable configuration items are as follows:

| Option Name | Description | UTC001 | VT850 | Fabric B option (UTC001 Req'd) |
|---|---|---|---|---|
| **ENABLE_TX_CLKA1 – 12** | Output to AMC Slot 1 - 12 CLK1/A | ✔ | ✔ | |
| **ENABLE_TX_CLKB1 – 12** | Output to AMC Slot 1 – 12 CLK2/B | ✔ | ✔ | |
| **ENABLE_TX_CLKC1 – 12** | Output to AMC Slot 1 – 12 CLK3/FCLKA or CLKC | ✔ | ✔ | ✔ |
| **ENABLE_TX_CLKD1 – 12** | Output to AMC Slot 1 – 12 CLKD | | ✔ | |
| **ENABLE_TX_MCH_UPDATE0 – 1** | Output to other MCH on channel 0 or 1 | ✔ | | |

Table 14: Clock Enables Configuration Items

**NOTE:** This table follows the VTCLOCK subsystem naming convention. Please refer to section 2.2 to see the backplane or AMC equivalent clock name for your particular configuration.

**EXAMPLE CONFIGURATION FILE ENTRY:**

```
ENABLE_TX_CLKA3=ON
```

This forces the transmitter to be enabled for outputting a clock to the AMC Slot 3 CLKA channel.

### 4.2.4 Telco Operating Mode

Telco operating mode is selected automatically on boards using the Telcom TCXO ordering option. In this mode, a Zarlink ZL30105 T1/E1/SDH Stratum 3 Redundant System Clock Synchronizer chip is used in combination with a 20 MHz Stratum 3 TCXO. This chip acts as a PLL to synchronize the local system clocks to a reference clock and supports failover and holdover when a reference is lost.

The Zarlink chip accepts and provides many different telecom-specific clocks and framing pulses. Please refer to the chip's datasheet for a complete description of its functionality and as a guide for choosing the configuration options described below.

http://www.zarlink.com/zarlink/zl30105-datasheet-nov2005.pdf

The VTCLOCK subsystem reads the configuration file settings and sets the control pins on the Zarlink accordingly. After this initial setting, no further control changes are made (please contact Vadatech sales if you have specific control needs that go beyond the configuration file). The status pins are monitored and all changes in status are reflected on the front panel LEDs, are logged to /var/log/messages, may be viewed using **`vc status`**, and are also reflected in IPMI sensors.

#### 4.2.4.1 Telco Mode Configuration Options

The following options are available for Telco operating mode.

##### 4.2.4.1.1 TELCO_MODESEL – Telco mode selection

This option sets the MODE_SEL[1:0] control lines of the Zarlink chip (please refer to datasheet for complete description).

Available settings:

| Setting | Description |
|---|---|
| **NORMAL** | Normal (with automatic Holdover) |
| **HOLDOVER** | Holdover |
| **FREERUN** | Freerun |
| **AUTOMATIC** | Automatic (Normal with automatic Holdover and automatic reference switching) |

Table 15: TELCO_MODESEL Settings

EXAMPLE CONFIGURATION FILE ENTRY:

```
TELCO_MODESEL=AUTOMATIC
```

#### 4.2.4.1.2 TELCO_FASTLOCK – Telco Fast Locking

This option sets the FASTLOCK control line of the Zarlink chip (please refer to datasheet for complete description).

Available settings:

| Setting | Description |
|---|---|
| **0** | Lock the PLL normally |
| **1** | Lock the PLL quickly |

Table 16: TELCO_FASTLOCK Settings

EXAMPLE CONFIGURATION FILE ENTRY:

```
TELCO_FASTLOCK=1
```

#### 4.2.4.1.3 TELCO_TIECLR – Telco TIE Clear

This option sets the *TIE_CLR control line of the Zarlink chip (please refer to datasheet for complete description).

NOTE: Use positive logic, glue logic inverts this line for you.

Available settings:

| Setting | Description |
|---|---|
| **0** | Do not reset the TIE Circuit |
| **1** | Reset the TIE Circuit |

Table 17: TELCO_TIECLR Settings

EXAMPLE CONFIGURATION FILE ENTRY:

```
TELCO_TIECLR=1
```

This setting makes *TIE_CLR go LOW.

#### 4.2.4.1.4 TELCO_HMS – Telco Hitless Mode Switching

This option sets the HMS control line of the Zarlink chip (please refer to datasheet for complete description).

Available settings:

| Setting | Description |
|---|---|
| **0** | Disabled |
| **1** | Enabled |

Table 18: TELCO_HMS Settings

EXAMPLE CONFIGURATION FILE ENTRY:

```
TELCO_HMS=1
```

#### 4.2.4.1.5 TELCO_REFSEL – Telco Reference Selection

This option sets the REFSEL[1:0] control lines of the Zarlink chip (please refer to datasheet for complete description).

NOTE: When TELCO_MODESEL=AUTOMATIC this setting has no effect since the REFSEL[1:0] lines change direction in automatic mode to become inputs to the FPGA. The software uses these inputs to report the Zarlink-selected reference in this case.

Available settings:

| Setting | Description |
|---|---|
| **0** | Select REF0 input |
| **1** | Select REF1 input |
| **2** | Select REF2 / REF2_SYNC inputs |

Table 19: TELCO_REFSEL Settings

EXAMPLE CONFIGURATION FILE ENTRY:

```
TELCO_REFSEL=1
```

#### 4.2.4.1.6 TELCO_OUTSEL2 – Telco Output Selection 2

This option sets the OUT_SEL2 control line of the Zarlink chip (please refer to datasheet for complete description).

Available settings:

| Setting | Description |
|---|---|
| **0** | Generate the following clocks:<br><br>C2o, *C4o, C8o, *C16o<br><br>Generate the following frame pulses:<br><br>*F4o, F8o, *F16o |
| **1** | Generate the following clocks:<br><br>C2o, *C16o, C32, *C65o<br><br>Generate the following frame pulses:<br><br>*F16o, F32o, *F65o |

Table 20: TELCO_OUTSEL2 Settings

EXAMPLE CONFIGURATION FILE ENTRY:

```
TELCO_OUTSEL2=1
```

#### 4.2.4.1.7 TELCO_OUTSEL – Telco Output Selection

This option sets the OUTSEL[1:0] control lines of the Zarlink chip (please refer to datasheet for complete description).

Available settings:

| Setting | Description |
|---|---|
| **0** | C6o |
| **1** | C8.4o |
| **2** | C34o |
| **3** | C44o |

Table 21: TELCO_OUTSEL Settings

EXAMPLE CONFIGURATION FILE ENTRY:

```
TELCO_OUTSEL=2
```

#### 4.2.4.1.8 TELCO_SECMSTR – Telco Secondary Master

This option sets the SEC_MSTR control line of the Zarlink chip (please refer to datasheet for complete description).

Available settings:

| Setting | Description |
|---|---|
| **0** | Primary Master |
| **1** | Secondary Master |

Table 22: TELCO_SECMSTR Settings

EXAMPLE CONFIGURATION FILE ENTRY:

```
TELCO_SECMSTR=1
```

#### 4.2.4.1.9 TELCO_APPSEL – Telco Application Selection

This option sets the APP_SEL[1:0] control lines of the Zarlink chip (please refer to datasheet for complete description).

Available settings:

| Setting | Description |
|---|---|
| **DS1** | ANSI T1.403 / Telcordia GR-1244-CORE Stratum 4/4E |
| **E1** | ITU-T G.703 / ETSI ETS 300 011 |
| **PDH** | Telcordia GR-1244-CORE Stratum 3 |
| **SDH** | ITU-T G.813 Option 1 / Telcordia GR-253-CORE |

Table 23: TELCO_APPSEL Settings

EXAMPLE CONFIGURATION FILE ENTRY:

```
TELCO_APPSEL=E1
```

#### 4.2.4.2 Zarlink Clock Signal Mapping

The Zarlink chip has fairly cryptic naming for its clock and frame pulse signal lines and many of them are multiplexed. Therefore, these signals have been mapped to more user friendly names for use in the configuration file and documentation. The mapping of the names is shown below:

| Zarlink Name | VTCLOCK Source Name | Zarlink Pin Mux Control | Resulting Clock |
|---|---|---|---|
| C1.5 | **CLK1.544** | N/A | 1.544 MHz |
| C2 | **CLK2.048** | N/A | 2.048 MHz |
| C3 | **CLK3.088** | N/A | 3.088 MHz |
| *C4 | **CLK4.096** | **TELCO_OUTSEL2=0** | 4.096 MHz (inverted) |
| *C65 | **CLK4.096** | **TELCO_OUTSEL2=1** | 65.536 MHz (inverted) |
| C6 | **CLK6.312** | **TELCO_OUTSEL=0** | 6.312 MHz |
| C8.4 | **CLK6.312** | **TELCO_OUTSEL=1** | 8.448 MHz |
| C34 | **CLK6.312** | **TELCO_OUTSEL=2** | 34.358 MHz |
| C44 | **CLK6.312** | **TELCO_OUTSEL=3** | 44.736 MHz |
| C8 | **CLK8.192** | **TELCO_OUTSEL2=0** | 8.192 MHz |
| C32 | **CLK8.192** | **TELCO_OUTSEL2=1** | 32.768 MHz |
| *C16 | **CLK16.384** | N/A | 16.384 MHz (inverted) |
| C19 | **CLK19.44** | N/A | 19.44 MHz |
| *F4 | **F4** | **TELCO_OUTSEL2=0** | 8 kHz (244ns low) Framing Pulse |
| *F65 | **F4** | **TELCO_OUTSEL2=1** | 8 kHz (15ns low) Framing Pulse |
| F8 | **F8** | **TELCO_OUTSEL2=0** | 8 kHz (122ns high) Framing Pulse |
| F32 | **F8** | **TELCO_OUTSEL2=1** | 8 kHz (32ns high) Framing Pulse |
| *F16 | **F16** | N/A | 8 kHz (61ns low) Framing Pulse |
| F2K | **F2K** | N/A | 2 kHz (51ns high) Framing Pulse |

Table 24: Zarlink Clock Signal Mapping

NOTE: '*' means inverted signal and is typically shown as a bar over the signal name in the Zarlink datasheet. The VTCLOCK FPGA does not do any additional inversion for clock signals, so the output clock looks the same as when it originated from the Zarlink chip.

### 4.2.5 GPS Operating Modes

The GPS option provides two different operating modes: Freerun and Disciplined. These modes are discussed in the following sections.

#### 4.2.5.1 GPS Freerun Operating Mode

GPS Freerun mode is provided as an aid to system development when in a lab setting. This mode does not discipline the oscillator nor attempt to phase align to a reference 1PPS input. Instead it allows for a specific DAC control setting to be specified in the configuration file for manual calibration and acts as a frequency/1PPS source to the chassis during development (when slaving to a GPS receiver may not be practical).

**NOTE:** This mode is NOT recommended for deployed products unless the undisciplined oscillator performance/drift is considered acceptable enough to use as a master clock in your particular system. Use of the GPS DISCIPLINED mode with an external GPS receiver is strongly recommended.

#### 4.2.5.2 GPS Disciplined Operating Mode

GPS Disciplined mode tracks an external reference positive one pulse per second (1PPS) signal from a GPS receiver (or other similar stable reference) and provides the precisely desired TCVCXO output frequency (10 MHz or 30.72 MHz option) as well as a corresponding phase-aligned internally generated 1PPS signal. Both the TCVCXO frequency and the internally generated 1PPS signal are capable of holding over (flywheeling) if the reference signal is lost. This ensures that there is minimal or no disruption to the rest of the system which is relying on these clocks.

This mode enables a plesiosynchronous clocking model whereby physically separated entities (such as cell towers) can remain synchronized with each other without directly sharing a wired clock. Each entity derives its own accurate clock frequency from the reference provided by the GPS system's satellites. Since each GPS satellite contains an atomic clock that is synchronized to every other GPS satellite, accurate timing synchronization can be achieved at different points around the world.

The GPS Disciplined mode locks to the reference 1PPS signal by going through the following steps:

1. **Qualify the reference 1PPS:** Back-to-back rising edges of the reference 1PPS signal must be occurring within +/- 18.4 PPM ticks of the TCVCXO clock. After the reference 1PPS signal is qualified (with hysteresis) then the REFGOOD indication turns on and processing can move to step 2.

2. **Discipline the TCVCXO frequency:** The TCVCXO is tuned to the desired frequency as measured against back-to-back rising edges of the reference 1PPS signal through changes to the setting of the control DAC. After the TCVCXO is within +/- 1 Hz (with hysteresis) then the FREQLOCK indication turns on and processing can move to step 3.

3. **Slew the internally generated 1PPS phase close to the reference 1PPS phase:** The internal 1PPS generator is slewed until the phases of the reference and internal 1PPS fall within the fine phase capture window. During this time the PHASELOCK indication is off but the PHASELOCK LED is blinking rapidly. Then processing moves to step 4.

4. **Fine phase alignment/tracking:** The phase of the internally generated 1PPS is precisely aligned to the reference 1PPS phase by making small adjustments to the TCVCXO control DAC. Once the rising edges are aligned within +/- 25ns of each other (as measured within the FPGA with filtering and hysteresis) then the PHASELOCK indication turns on and from that point on the phase is tracked and kept aligned through small adjustments to the TCVCXO control DAC only as needed.

The GPS Disciplined control loop enters Holdover any time the reference 1PPS pulse does not arrive as expected and the subsystem had previously achieved phase lock. During holdover the TCVCXO control DAC is held at the last/best setting that was determined during fine phase alignment/tracking.

The disciplining algorithm will strive to make the phase error zero as seen by the FPGA over time, so the final phase alignment can be much better than the +/- 25ns locking criteria. However, various factors such as quantization noise on the GPS receiver's 1PPS output can make the phases of the reference 1PPS and the generated 1PPS appear to jitter slightly with respect to each other if viewed on an oscilloscope. As a specific example: the Trimble Acutime Gold™ GPS Smart Antenna's 1PPS output will appear to jitter within a 40ns window surrounding the 'true' 1PPS since its quantization error is +/- 20ns. This jitter is clearly visible to the VTCLOCK's fine phase detector, and steps are taken to minimize the effect of this jitter on overall clocking operation. The generated 1PPS alignment algorithm effectively attempts to find the center of this quantization noise over time. So the generated 1PPS will typically be closer to the 'true' GPS 1PPS than the actual GPS receiver's 1PPS output and will have less jitter. Still it is better to have as little quantization noise as possible on the reference 1PPS input. Please refer to the 'PPS accuracy' or 'PPS Quantization Error' specification of your particular GPS receiver to determine its 1PPS quality. The better the

quality of the GPS receiver's reference 1PPS, the better the quality of the VTCLOCK TCVCXO frequency and 1PPS phase derived from it.

The 1PPS phase error is zeroed out at the point of the FPGA. However, if sub-microsecond level accuracy is required for the generated 1PPS phase, there are various signal propagation delays before the FPGA (GPS receiver cable, SMA/SMB input stage, FPGA internal circuitry, etc) and after the FPGA (M-LVDS output stage, backplane traces to the AMCs, etc) which should be compensated for. Most GPS receivers have an option for advancing or delaying the 1PPS to compensate for 'cable delay'. This setting should also be used to cancel out the additional delay through the VTCLOCK sub-system (if desired). The calibration measurement should be made from the GPS receiver's 1PPS output port to the destination AMC (where the 1PPS will be consumed) and should include the full length of cabling to be used in the installation). Please refer to your particular GPS receiver's documentation for how to make this calibration. The frequency accuracy of the TCVCXO output is not affected by this optional calibration of the 1PPS phase.

The GPS Disciplined mode status changes are reflected on the front panel LEDs, are logged to **`/var/log/messages`**, can be viewed with **`vc status`**, and are also reflected in IPMI sensors.

### 4.2.6 GPS Configuration File Options

Both the GPS Freerun and Disciplined modes share one configuration file section. It is noted if a given option is applicable to only one mode or the other.

#### 4.2.6.1 GPS_MODE – GPS Operating Mode

This option sets the specific GPS operating mode whenever the GPS VCTCXO ordering option is in effect.

Available settings:

| Setting | Description |
|---|---|
| **DISCIPLINED** | Discipline the oscillator/1PPS to an external 1PPS reference |
| **FREERUN** | Freerun the oscillator/1PPS without an external 1PPS reference (usually during system development only) |

Table 25: GPS_MODE Settings

EXAMPLE CONFIGURATION FILE ENTRY:

```
GPS_MODE=DISCIPLINED
```

#### 4.2.6.2 GPS_FREERUN_CAL – GPS Freerun DAC Calibration

This option sets the fixed DAC level during Freerun mode. This can be used to manually calibrate the frequency of the oscillator if desired.

NOTE: This option applies to GPS Freerun mode only.

Available settings:

| Setting | Description |
|---|---|
| **-32768** (slower) to **32767** (faster) | Set the DAC level within a 16 bit signed range. |

Table 26: GPS_FREERUN_CAL Settings

EXAMPLE CONFIGURATION FILE ENTRY:

```
GPS_FREERUN_CAL=12345
```

### 4.2.6.3 GPS_1PPS_GEN_WIDTH – GPS 1PPS Generated Pulse Width

This option sets the desired width of the internally generated 1PPS positive pulse.

Available settings:

| Setting | Description |
|---|---|
| **0** to **TCXO_FREQ**-1 | Set the width of the HIGH portion of the 1PPS signal in units of TCVCXO ticks. |

Table 27: GPS_1PPS_GEN_WIDTH Settings

EXAMPLE CONFIGURATION FILE ENTRY:

**GPS_1PPS_GEN_WIDTH=3072** (100us with a 30.72 MHz TCVCXO)

### 4.2.6.4 GPS_1PPS_TURN_ON – GPS 1PPS Turn On Criteria

Since the internally generated 1PPS signal must be phase aligned before it truly corresponds to the start of the second, customers may find it desirable to control when this clock output is seen by the rest of the system. This option gives four different settings to control when the internal 1PPS will be provided. The higher on the list, the faster the 1PPS will be seen by the system during acquisition. The lower on the list, the more accurate the 1PPS will be during the time it is seen by the rest of the system.

NOTE: This option applies to GPS Disciplined mode only. The 1PPS output is always on in GPS Freerun mode.

Available settings:

| Setting | Description |
|---|---|
| **ALWAYS** | Always output the generated 1PPS pulse |
| **AFTER_FREQLOCK** | Output the generated 1PPS pulse only after the frequency is locked (but the 1PPS pulses might not align yet) or during holdover |
| **AFTER_1PPS_ALIGN** | Output the generated 1PPS pulse only after the 1PPS pulses are roughly aligned (within +/- 315ns) or during holdover |
| **AFTER_PHASELOCK** | Output the generated 1PPS pulse only when phase is locked or during holdover |

Table 28: GPS_1PPS_TURN_ON Settings

EXAMPLE CONFIGURATION FILE ENTRY:

**GPS_1PPS_TURN_ON=AFTER_PHASELOCK**

### 4.2.7 Clock Routing Only Operating Mode

This operating mode is used when neither the Zarlink or GPS mount options are present but the Clock Routing Only option is present. In this mode, front panel and backplane clock routing may still be performed. The clock routes are setup and Clock E-Keying is performed but otherwise no monitoring of status or LED updates are performed.

This mode is pre-selected at the factory by setting the oscillator selection switches to the NONE setting.

# 5 Appendix A: UTC001/UTC002 Clocking Pin-out

The **UTC001/UTC002 MCH Tongue 2** connector carries all of the backplane clock signals. The MCH supports both the *default* and the *Alternate Connector 2 – 3 Clock, partial Fabric* pin-outs from the uTCA specification depending on the 'Fabric B' ordering option. The 3-clock pinout is shown below since this is the maximum configuration. The portion which changes based on ordering option is highlighted in blue:

| MCH TX & TX Enable (VTCLOCK) | MCH RX (VTCLOCK) | uTCA Spec | Pin Numbers |
|---|---|---|---|
| CLKA (ENABLE_TX_CLKA1) | AMC_A1 | CLK1-1 | 50/51 |
| CLKA (ENABLE_TX_CLKA2) | AMC_A2 | CLK1-2 | 53/54 |
| CLKA (ENABLE_TX_CLKA3) | AMC_A3 | CLK1-3 | 56/57 |
| CLKA (ENABLE_TX_CLKA4) | AMC_A4 | CLK1-4 | 59/60 |
| CLKA (ENABLE_TX_CLKA5) | AMC_A5 | CLK1-5 | 62/63 |
| CLKA (ENABLE_TX_CLKA6) | AMC_A6 | CLK1-6 | 65/66 |
| CLKA (ENABLE_TX_CLKA7) | AMC_A7 | CLK1-7 | 68/69 |
| CLKA (ENABLE_TX_CLKA8) | AMC_A8 | CLK1-8 | 71/72 |
| CLKA (ENABLE_TX_CLKA9) | AMC_A9 | CLK1-9 | 74/75 |
| CLKA (ENABLE_TX_CLKA10) | AMC_A10 | CLK1-10 | 77/78 |
| CLKA (ENABLE_TX_CLKA11) | AMC_A11 | CLK1-11 | 80/81 |
| CLKA (ENABLE_TX_CLKA12) | AMC_A12 | CLK1-12 | 83/84 |
| CLKB (ENABLE_TX_CLKB1) | AMC_B1 | CLK2-1 | 120/121 |
| CLKB (ENABLE_TX_CLKB2) | AMC_B2 | CLK2-2 | 117/118 |
| CLKB (ENABLE_TX_CLKB3) | AMC_B3 | CLK2-3 | 114/115 |
| CLKB (ENABLE_TX_CLKB4) | AMC_B4 | CLK2-4 | 111/112 |
| CLKB (ENABLE_TX_CLKB5) | AMC_B5 | CLK2-5 | 108/109 |
| CLKB (ENABLE_TX_CLKB6) | AMC_B6 | CLK2-6 | 105/106 |
| CLKB (ENABLE_TX_CLKB7) | AMC_B7 | CLK2-7 | 102/103 |
| CLKB (ENABLE_TX_CLKB8) | AMC_B8 | CLK2-8 | 99/100 |
| CLKB (ENABLE_TX_CLKB9) | AMC_B9 | CLK2-9 | 96/97 |
| CLKB (ENABLE_TX_CLKB10) | AMC_B10 | CLK2-10 | 93/94 |
| CLKB (ENABLE_TX_CLKB11) | AMC_B11 | CLK2-11 | 90/91 |
| CLKB (ENABLE_TX_CLKB12) | AMC_B12 | CLK2-12 | 87/88 |
| CLKC (ENABLE_TX_CLKC1) | AMC_C1 | CLK3-1 | 32/33 |
| CLKC (ENABLE_TX_CLKC2) | AMC_C2 | CLK3-2 | 35/36 |
| CLKC (ENABLE_TX_CLKC3) | AMC_C3 | CLK3-3 | 38/39 |
| CLKC (ENABLE_TX_CLKC4) | AMC_C4 | CLK3-4 | 41/42 |
| CLKC (ENABLE_TX_CLKC5) | AMC_C5 | CLK3-5 | 44/45 |
| CLKC (ENABLE_TX_CLKC6) | AMC_C6 | CLK3-6 | 47/48 |
| CLKC (ENABLE_TX_CLKC7) | AMC_C7 | CLK3-7 | 138/139 |
| CLKC (ENABLE_TX_CLKC8) | AMC_C8 | CLK3-8 | 135/136 |
| CLKC (ENABLE_TX_CLKC9) | AMC_C9 | CLK3-9 | 132/133 |
| CLKC (ENABLE_TX_CLKC10) | AMC_C10 | CLK3-10 | 129/130 |
| CLKC (ENABLE_TX_CLKC11) | AMC_C11 | CLK3-11 | 126/127 |
| CLKC (ENABLE_TX_CLKC12) | AMC_C12 | CLK3-12 | 123/124 |
| MCH_UPDATE0 (ENABLE_TX_MCH_UPDATE0) | MCH_UPDATE0 | CLK1_Tx | 11/12 |
| MCH_UPDATE1 (ENABLE_TX_MCH_UPDATE1) | MCH_UPDATE1 | CLK1_Rx | 159/160 |

Table 29: UTC001/UTC002 Clocking Pin-out

# 6 Appendix B: Configuration Samples

The following examples show the key settings needed in order to achieve the desired result for some theoretical configurations. Additional settings are present in the configuration file and all settings should be specified as needed for your particular system.

GPS VCTCXO ordering option: GPS receiver attached to front panel input with 30.72 MHz and internal 1PPS distributed to AMC v2 cards as CLKA and CLKC relying on Clock E-Keying for output enables:

```
GPS_MODE=DISCIPLINED
ROUTE_REF1_FROM=CLOCK_IN
ROUTE_CLKA_FROM=TCXO
ROUTE_CLKC_FROM=1PPS_GEN
```

Telcom TCXO ordering option: Two telco line card AMCs being used as redundant references for the Zarlink PLL chip using their CLKB outputs with a Zarlink output clock and framing pulse being distributed to AMC v2 cards as CLKA and CLKC relying on Clock E-Keying for output enables:

```
TELCO_MODESEL=AUTOMATIC
ROUTE_REF0_FROM=AMC_B3
ROUTE_REF1_FROM=AMC_B4
ROUTE_CLKA_FROM=CLK1.544
ROUTE_CLKC_FROM=F8
```

Either ordering option: An AMC v1 clock module providing CLK1 and CLK2 output to all other AMC v1 modules on their CLK1 and CLK2 inputs (no Zarlink or GPS involvement, clock routing only) NOT relying on Clock E-Keying for output enables:

```
ROUTE_CLKA_FROM=AMC_A3          (AMC v1 CLK1)
ROUTE_CLKB_FROM=AMC_B3          (AMC v1 CLK2)
ENABLE_TX_CLKA1=ON
ENABLE_TX_CLKA2=ON
ENABLE_TX_CLKA3=AUTO            (effectively OFF in this case, this is an RX channel)
ENABLE_TX_CLKA4=ON
ENABLE_TX_CLKA5=ON
ENABLE_TX_CLKA6=ON
ENABLE_TX_CLKA7=ON
ENABLE_TX_CLKA8=ON
ENABLE_TX_CLKA9=ON
ENABLE_TX_CLKA10=ON
ENABLE_TX_CLKA11=ON
ENABLE_TX_CLKA12=ON
ENABLE_TX_CLKB1=ON
ENABLE_TX_CLKB2=ON
ENABLE_TX_CLKB3=AUTO            (effectively OFF in this case, this is an RX channel)
ENABLE_TX_CLKB4=ON
ENABLE_TX_CLKB5=ON
ENABLE_TX_CLKB6=ON
ENABLE_TX_CLKB7=ON
ENABLE_TX_CLKB8=ON
ENABLE_TX_CLKB9=ON
ENABLE_TX_CLKB10=ON
ENABLE_TX_CLKB11=ON
ENABLE_TX_CLKB12=ON
```