Lab 6 EC413

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In this lab, we create the 4-stage pipeline datapath. We modified and used the following modules: Stage1_register, n-bit register to read and write R0-R6, Stage2_register, Mux to select between immediate and register 2, our ALU, and Stage3_register to return the ALU output to overwrite the n-bit register.

In this lab, we reused the ALU from Lab 5. So we don't need to test the testbench but we have to add mux to select if that instruction requires immediate or register value. And, the register files are all from the zip file; so we didn't do the testbench.

This is the waveform of our data pipeline testbench. We set the time for each test case as 30 ns while setting the clock as 5 ns. So, the result from each instruction should be updated before proceeding to the next one after 3 stages of the data pipeline cycle.