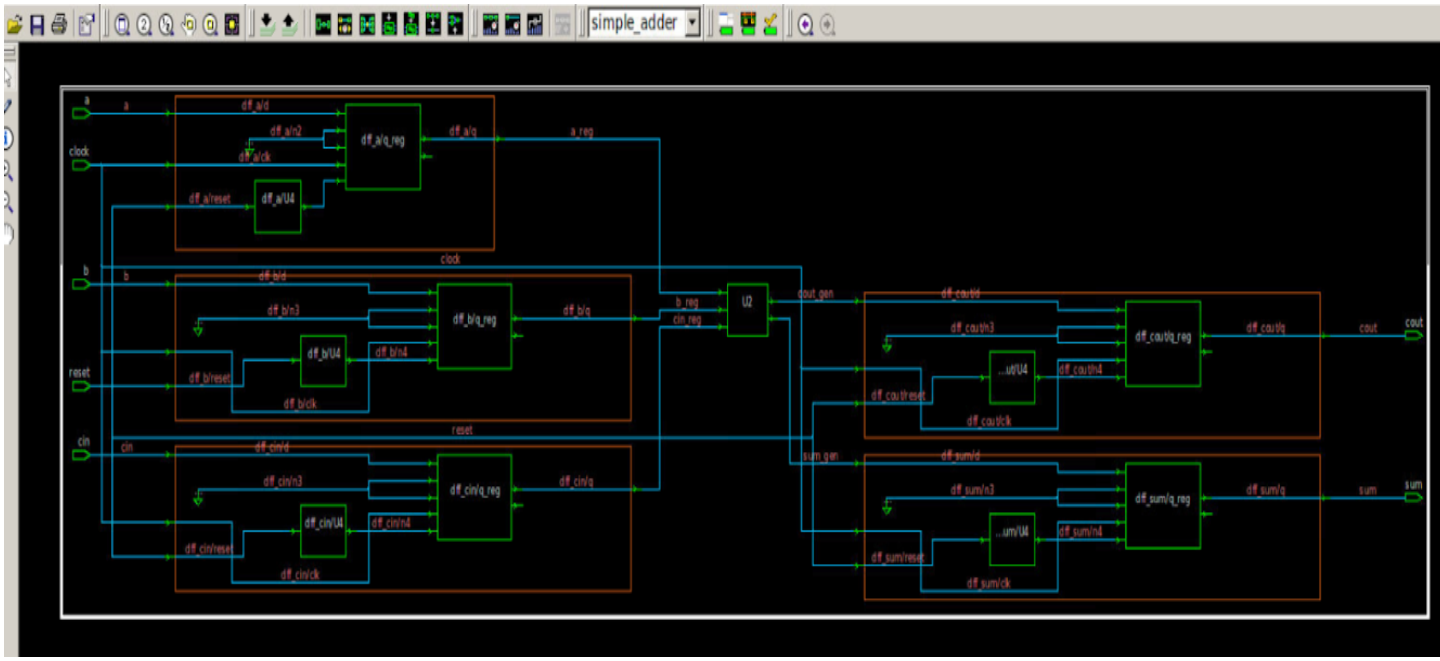
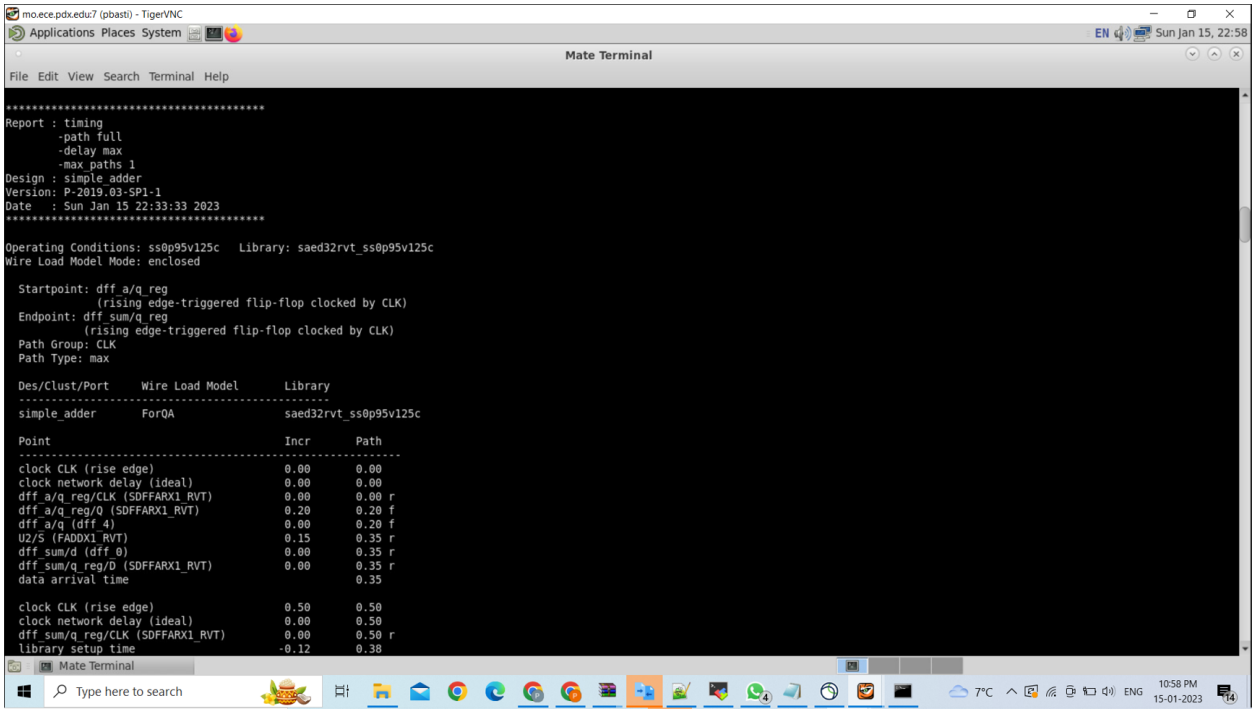
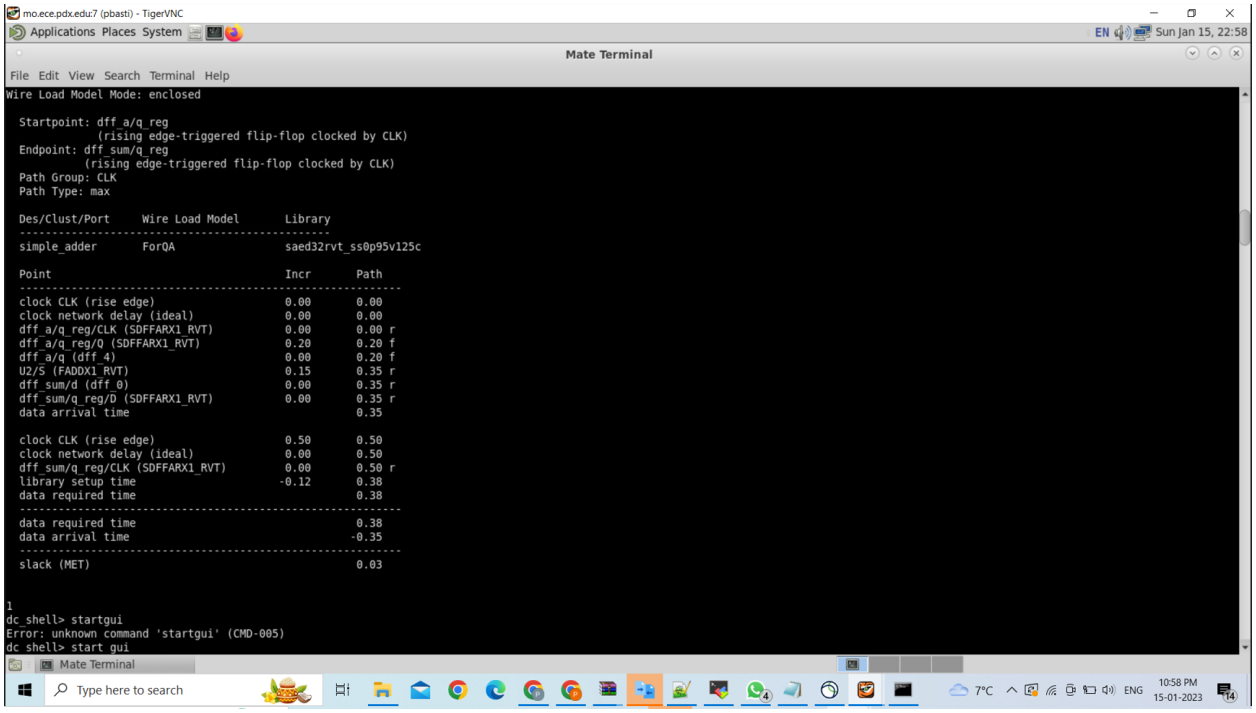
HW_LAB_1_A:

Schematic Circuit of simple adder



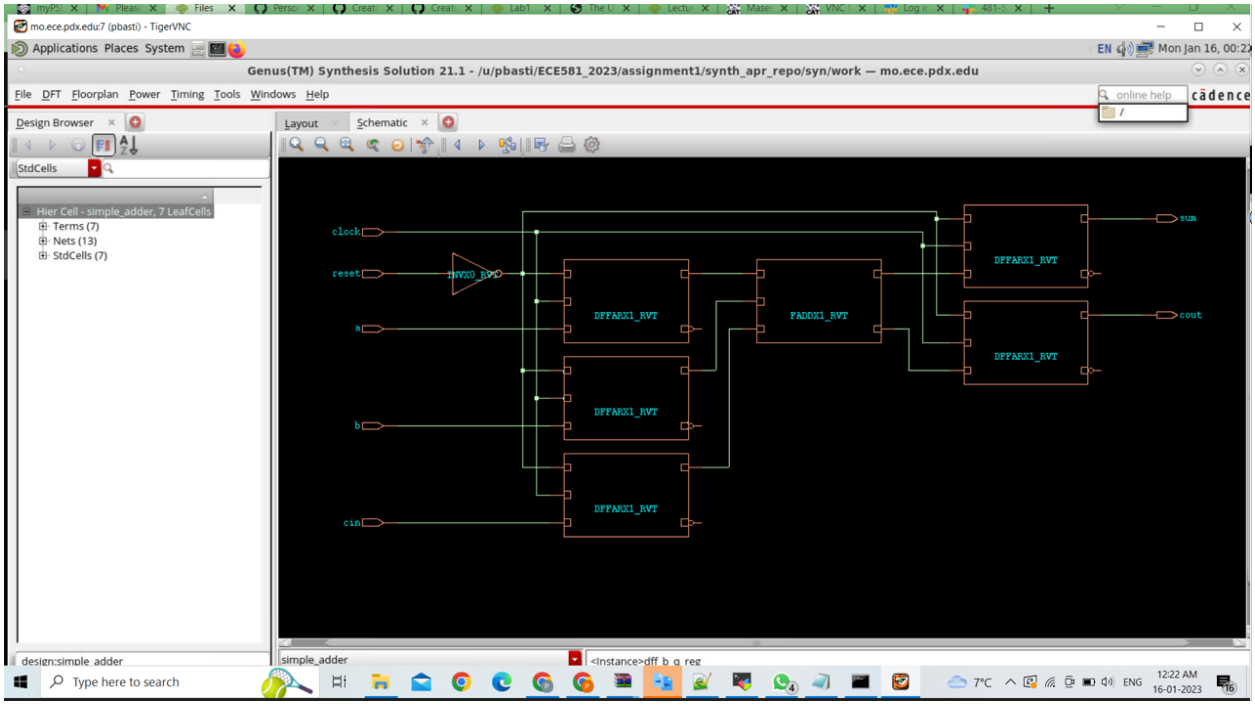
Report timing output



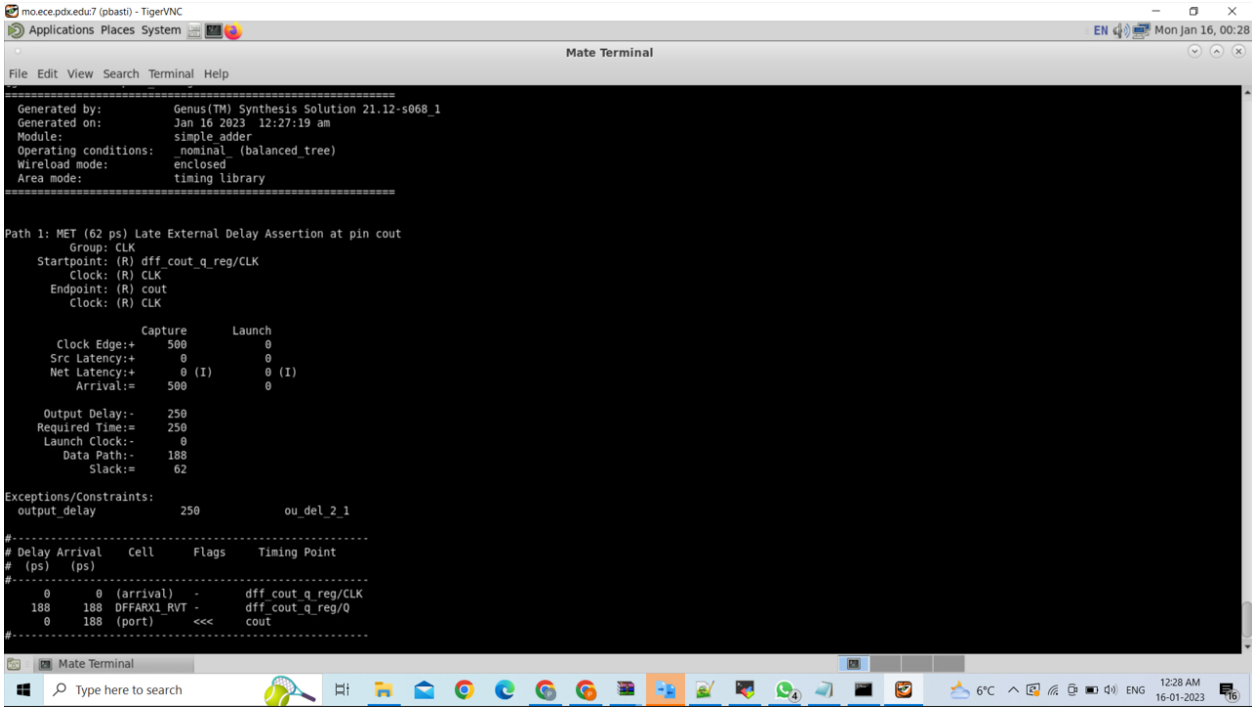


HW_LAB_1_B:

Schematic circuit in Genus



Report timing output in Genus

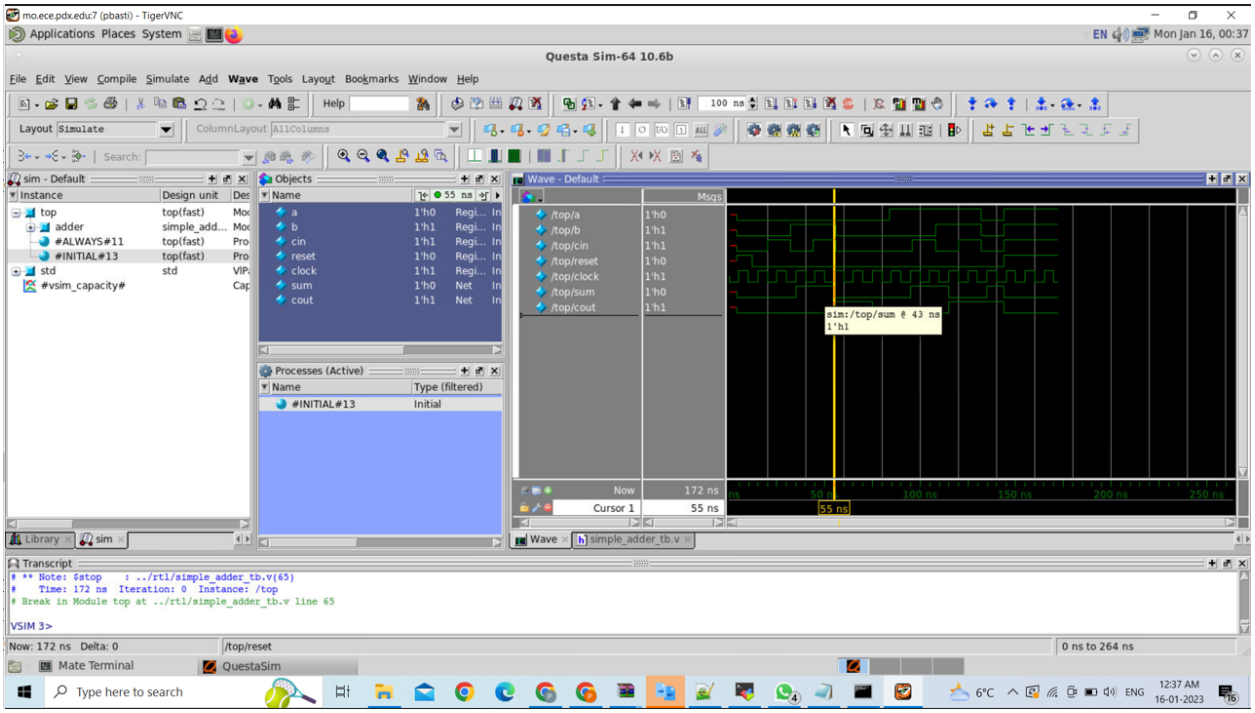


Comparison

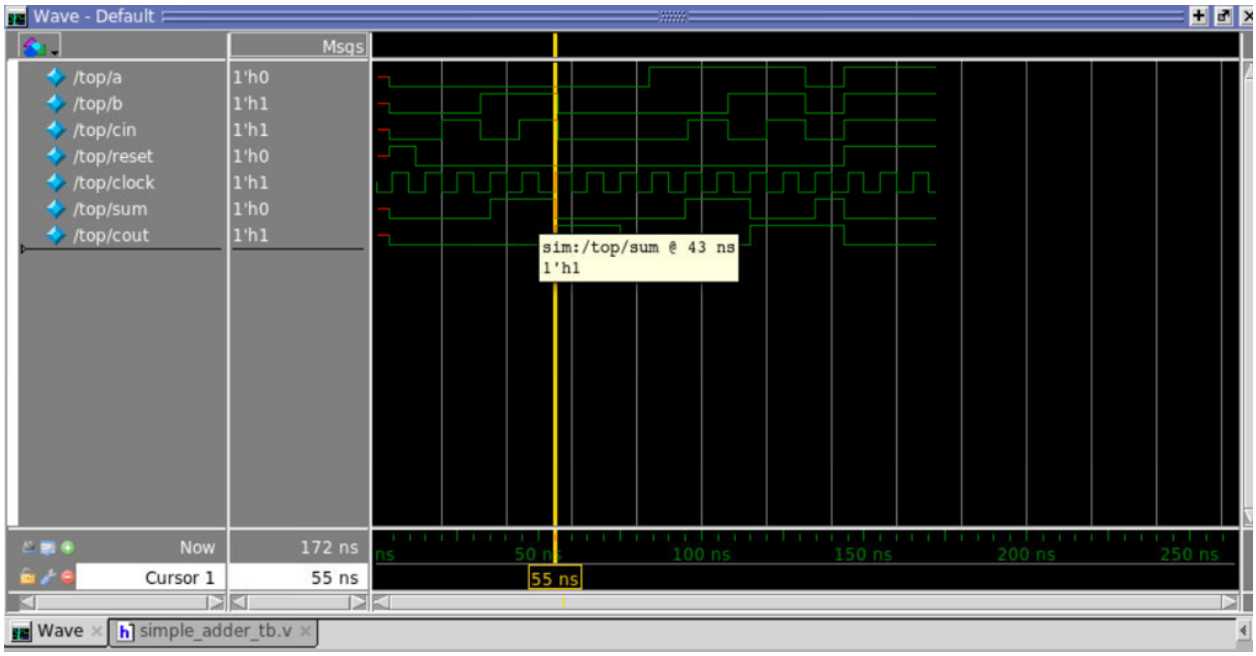
	DC	Genus
Cell count	11	7
Combinational cell count	6	2
Sequential cell count	5	5
area	56.928257	41.680
WNS	0	0
TNS	0	0
Violation count	0	0

HW_LAB_1_C:

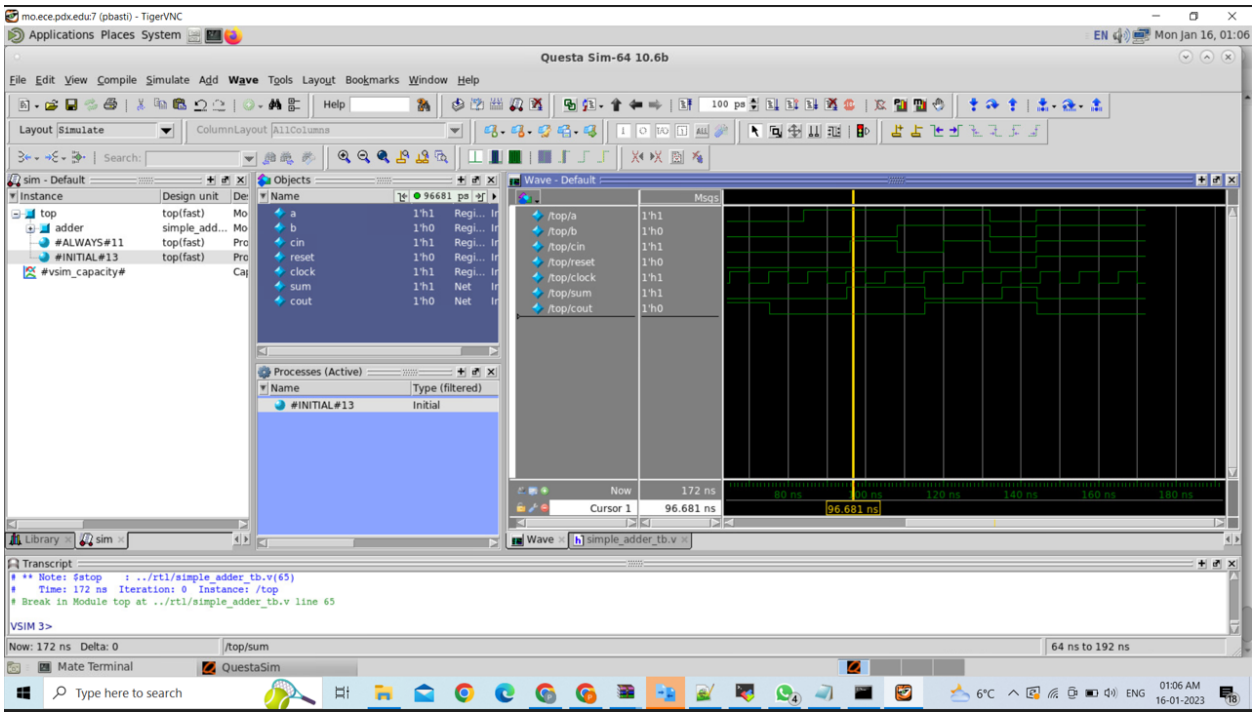
FE RTL Waveform



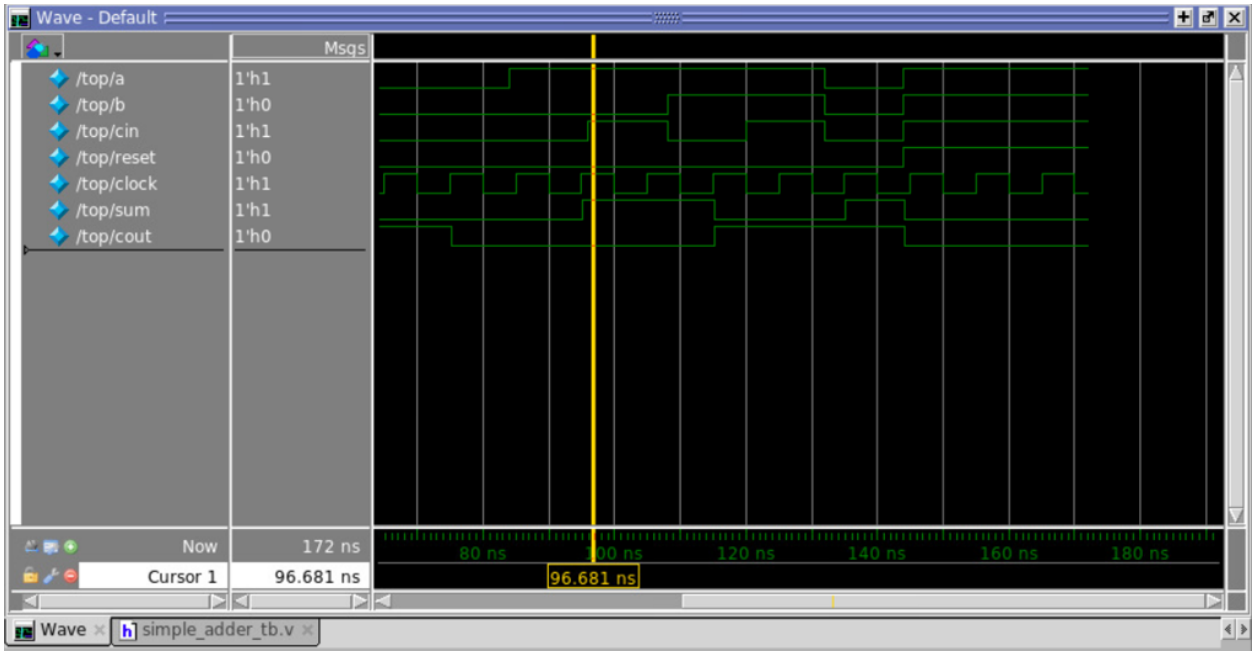
Zoomed view of the same



BE Netlist Waveform



Zoomed view of the same



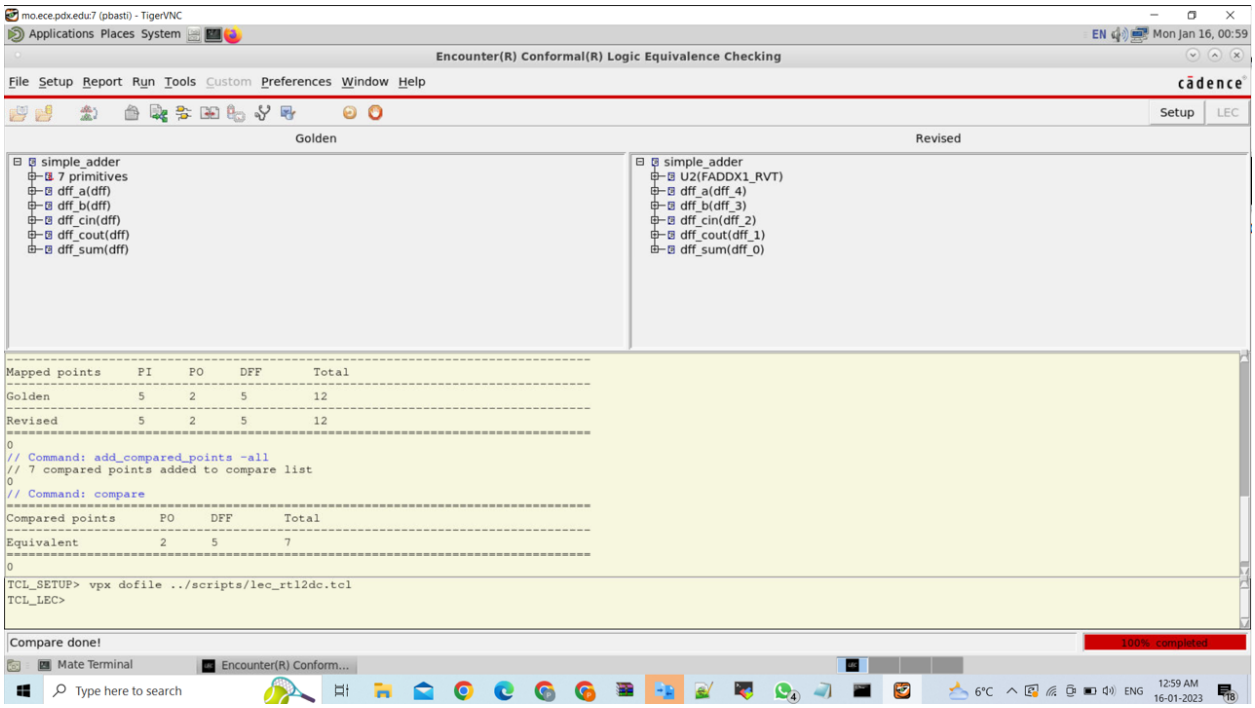
Comparison statement between FE RTL and BE NETLIST
There is no change in the RTL and generated netlist as it has same functionality because waveforms are same for both

Important Questa commands:

vlib - It is used to create a design library
vmap - It defines the mapping between a logical library name and a directory
vlog - Compiles all the verilog files
vsim - starts the VHDL/Questa simulator

HW_LAB_1_D:

LEC equivalency



LEC command description

read_design - This reads the RTL/netlist or the library files required for the lec run
set_system_mode - For switching of system modes
add_compared_files - To specify which mapped points conformal compares
Compare - compares the points in the list and checks if key points are equivalent or not

HW_LAB_1_E:

https://github.com/preetambasti/ECE-581-winter-2023