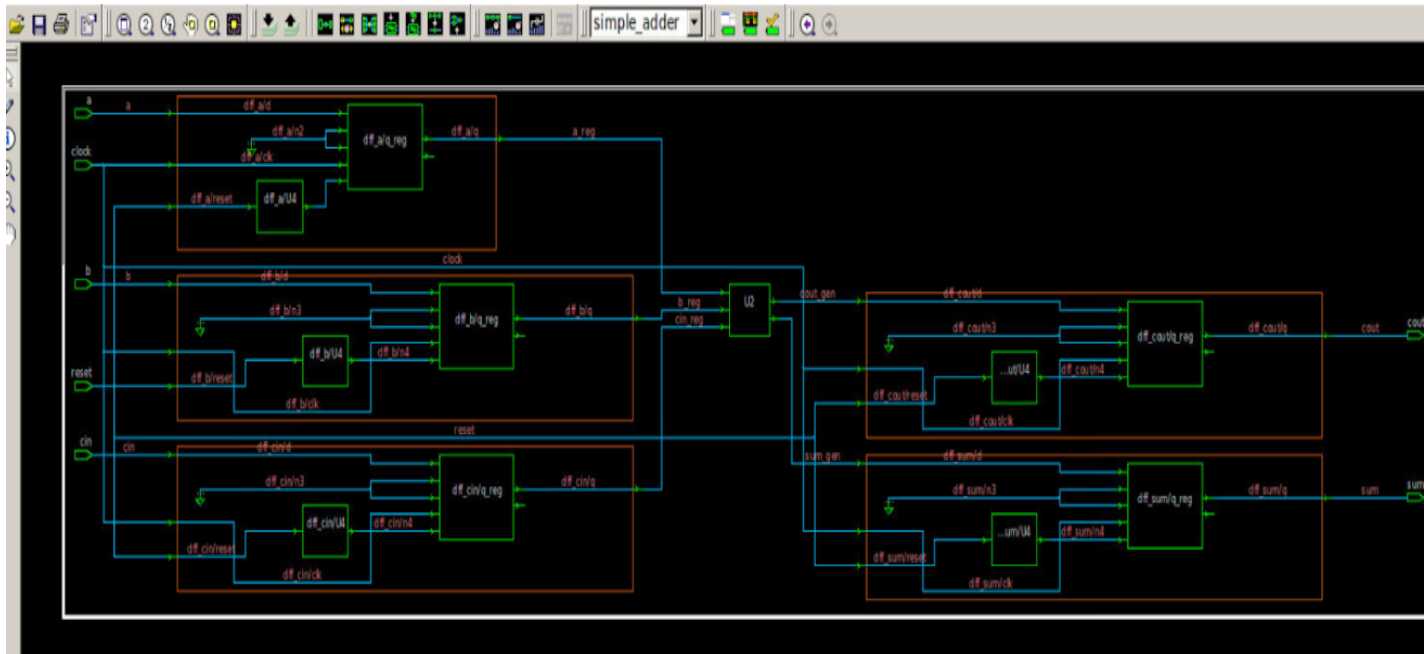


## HW\_LAB\_1\_A:

## Schematic Circuit of simple adder



## Report timing output

```

mo.ece.pdx.edu7 (pbasti) - TigerVNC
Applications Places System
Mate Terminal

File Edit View Search Terminal Help

*****
Report : timing
-path full
-delay max
-max paths 1
Design : simple_adder
Version : P-2019.03-SP1-1
Date : Sun Jan 15 22:33:33 2023
*****

Operating Conditions: ss0p95v125c Library: saed32rvt_ss0p95v125c
Wire Load Model Mode: enclosed

Startpoint: dff_a/q_reg
(rising edge-triggered flip-flop clocked by CLK)
Endpoint: dff_sum/q_reg
(rising edge-triggered flip-flop clocked by CLK)
Path Group: CLK
Path Type: max

Des/Clust/Port Wire Load Model Library
-----
simple_adder ForQA saed32rvt_ss0p95v125c

Point Incr Path
-----
clock CLK (rise edge) 0.00 0.00
clock network delay (ideal) 0.00 0.00
dff_a/q_reg/CLK (SDFFARX1_RVT) 0.00 0.00 r
dff_a/q_reg/Q (SDFFARX1_RVT) 0.20 0.20 f
dff_a/q (dff 4) 0.00 0.20 f
U2/S (FADDX1_RVT) 0.15 0.35 r
dff_sum/d (dff 0) 0.00 0.35 r
dff_sum/q_reg/D (SDFFARX1_RVT) 0.00 0.35 r
data arrival time 0.35

clock CLK (rise edge) 0.50 0.50
clock network delay (ideal) 0.00 0.50
dff_sum/q_reg/CLK (SDFFARX1_RVT) 0.00 0.50 r
library setup time -0.12 0.38

```

```

mo.ece.pdx.edu7 (pbasti) - TigerVNC
Applications Places System
Mate Terminal

File Edit View Search Terminal Help

Wire Load Model Mode: enclosed

Startpoint: dff_a/q_reg
(rising edge-triggered flip-flop clocked by CLK)
Endpoint: dff_sum/q_reg
(rising edge-triggered flip-flop clocked by CLK)
Path Group: CLK
Path Type: max

Des/Clust/Port Wire Load Model Library
-----
simple_adder ForQA saed32rvt_ss0p95v125c

Point Incr Path
-----
clock CLK (rise edge) 0.00 0.00
clock network delay (ideal) 0.00 0.00
dff_a/q_reg/CLK (SDFFARX1_RVT) 0.00 0.00 r
dff_a/q_reg/Q (SDFFARX1_RVT) 0.20 0.20 f
dff_a/q (dff 4) 0.00 0.20 f
U2/S (FADDX1_RVT) 0.15 0.35 r
dff_sum/d (dff 0) 0.00 0.35 r
dff_sum/q_reg/D (SDFFARX1_RVT) 0.00 0.35 r
data arrival time 0.35

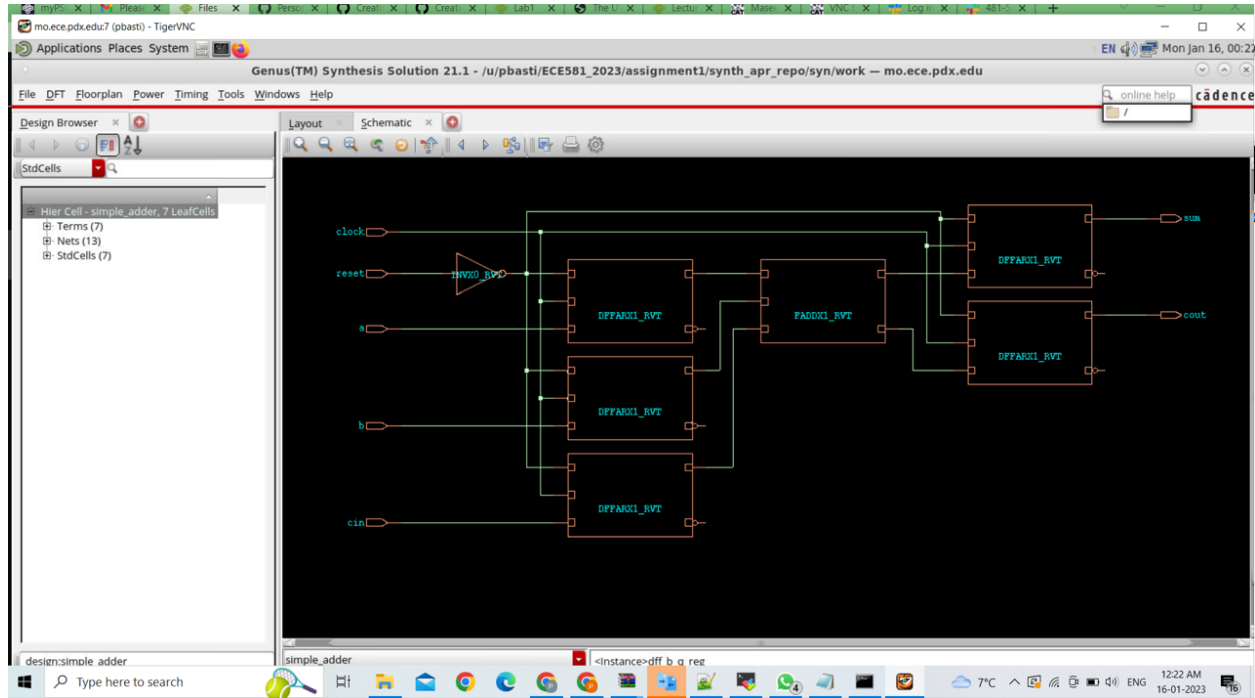
clock CLK (rise edge) 0.50 0.50
clock network delay (ideal) 0.00 0.50
dff_sum/q_reg/CLK (SDFFARX1_RVT) 0.00 0.50 r
library setup time -0.12 0.38
data required time 0.38
-----
data required time 0.38
data arrival time -0.35
-----
slack (MET) 0.03

1
dc shell> startgui
Error: unknown command 'startgui' (CMD-005)
dc shell> start gui

```

## HW\_LAB\_1\_B:

## Schematic circuit in Genus



## Report timing output in Genus

Generated by: Genus(TM) Synthesis Solution 21.12:s068\_1  
Generated on: Jan 16 2023 12:27:19 am  
Module: simple\_adder  
Operating conditions: nominal (balanced tree)  
Wireload mode: enclosed  
Area mode: timing library

Path 1: MET (62 ps) Late External Delay Assertion at pin cout  
Group: CLK  
Startpoint: (R) dff\_cout\_q\_reg/CLK  
Clock: (R) CLK  
Endpoint: (R) cout  
Clock: (R) CLK

	Capture	Launch
Clock Edge:+	500	0
Src Latency:+	0	0
Net Latency:+	0 (I)	0 (I)
Arrival:=-	500	0
Output Delay:-	250	
Required Time:=-	250	
Launch Clock:-	0	
Data Path:-	188	
Slack:=-	62	

Exceptions/Constraints:  
output\_delay 250 ou\_del\_2\_1

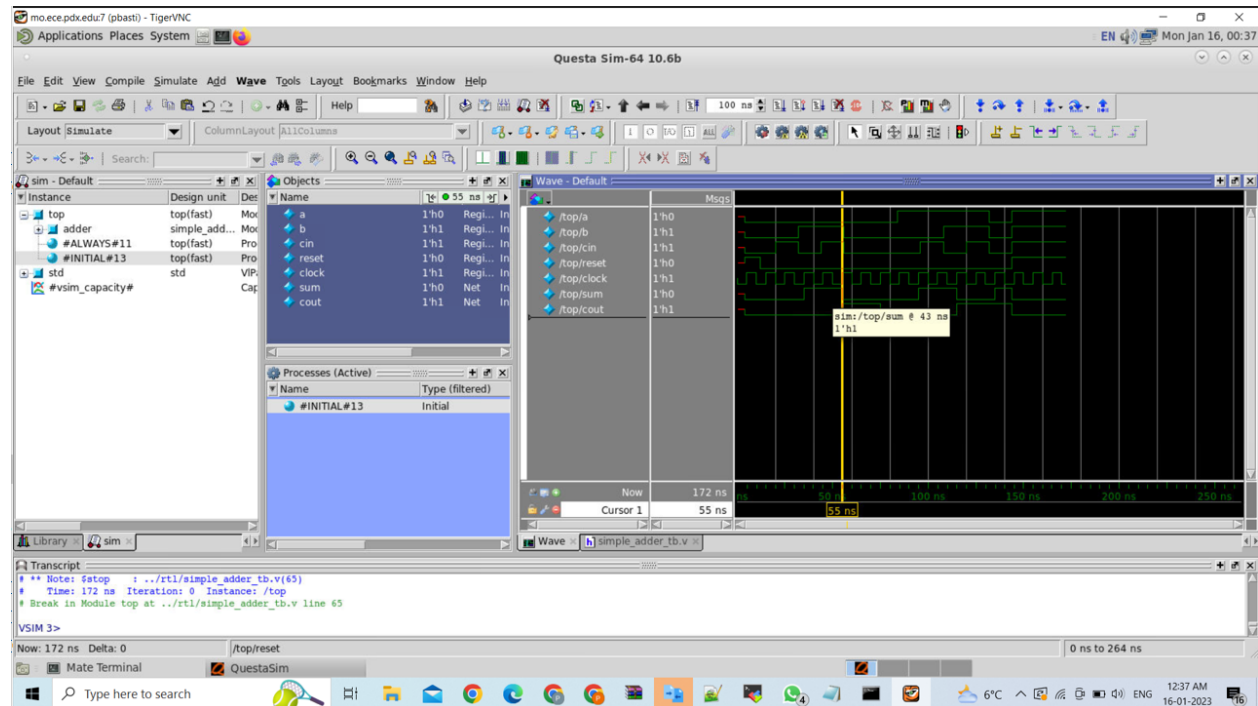
#	Delay Arrival (ps)	Cell	Flags	Timing Point
#	0	0 (arrival)	-	dff_cout_q_reg/CLK
#	188	DFFARX1_RVT	-	dff_cout_q_reg/Q
#	0	188 (port)	<<<	cout

## Comparison

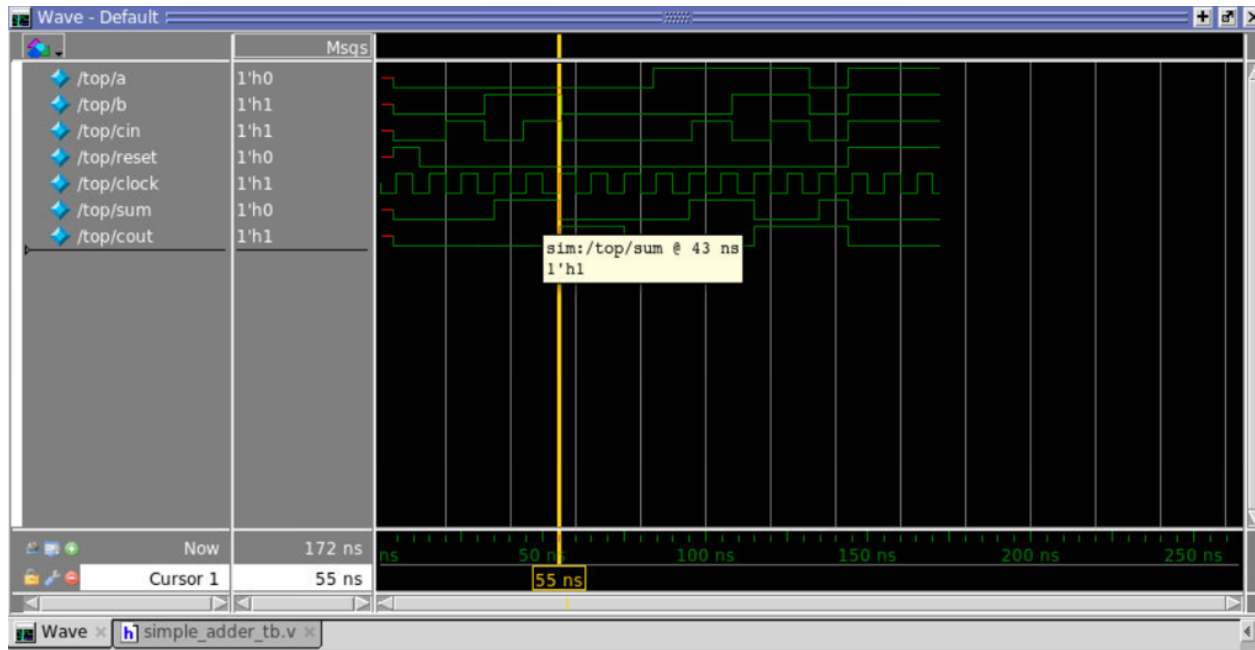
	DC	Genus
Cell count	11	7
Combinational cell count	6	2
Sequential cell count	5	5
area	56.928257	41.680
WNS	0	0
TNS	0	0
Violation count	0	0

## HW\_LAB\_1\_C:

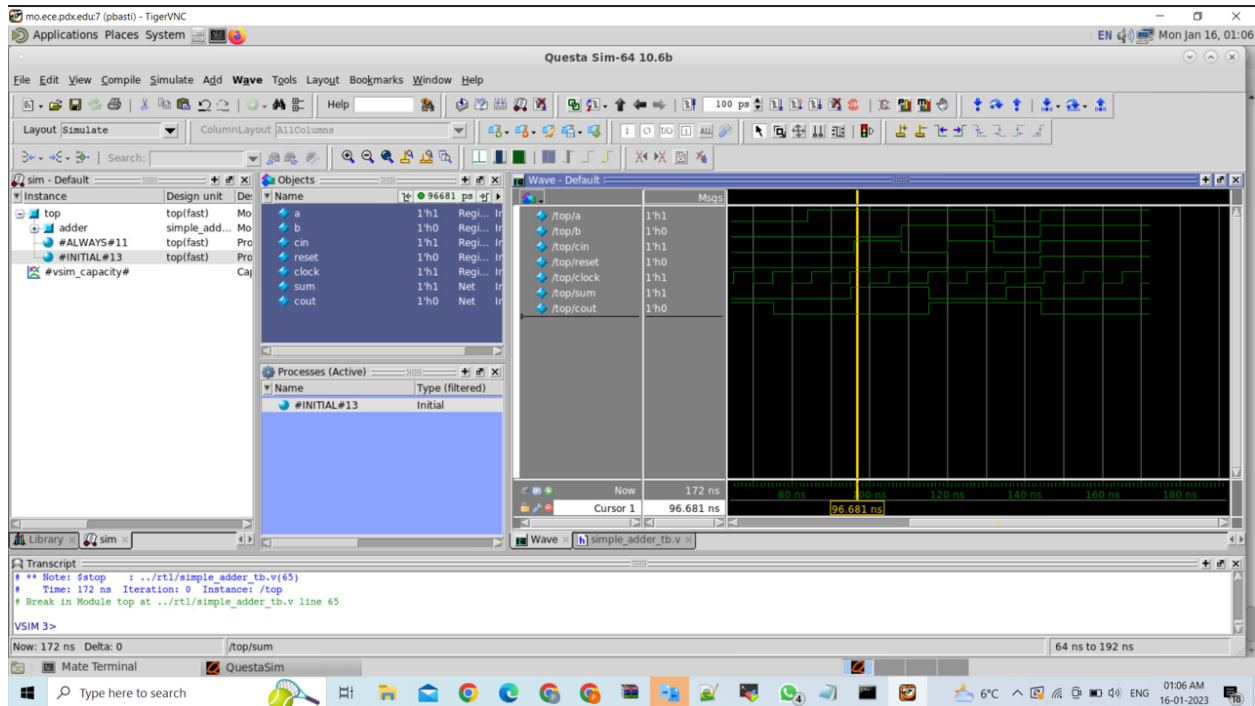
## FE RTL Waveform



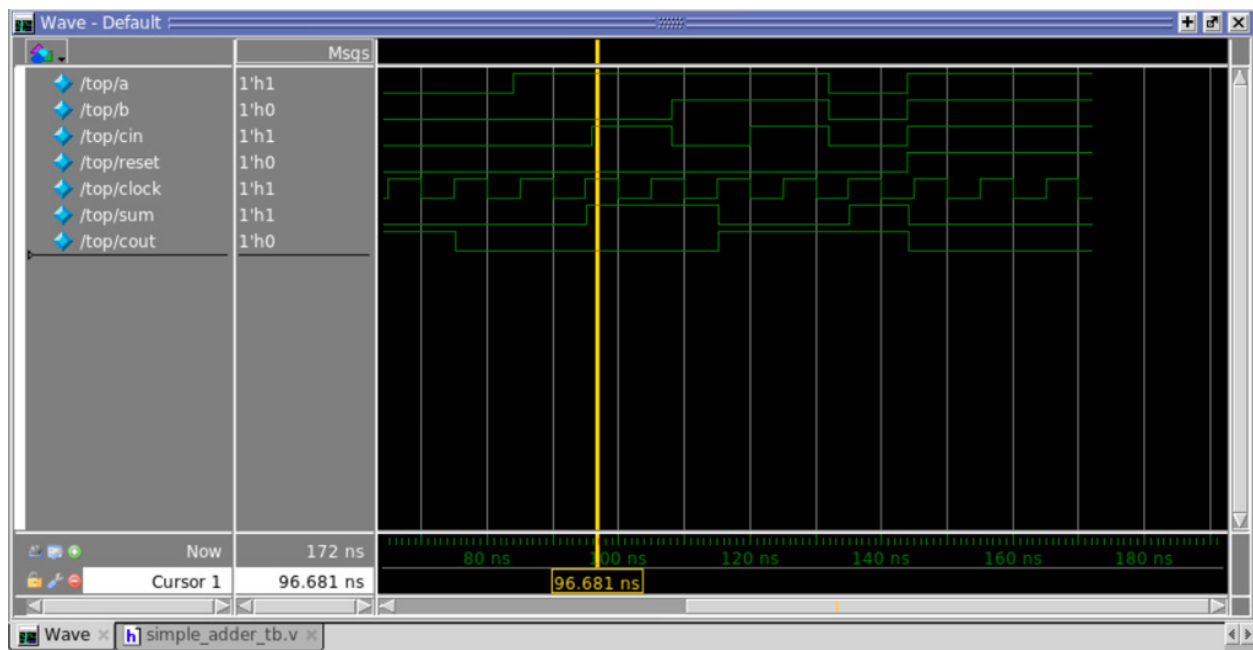
Zoomed view of the same



## BE Netlist Waveform



Zoomed view of the same



### Comparison statement between FE RTL and BE NETLIST

There is no change in the RTL and generated netlist as it has same functionality because waveforms are same for both

### Important Questa commands:

vlib - It is used to create a design library

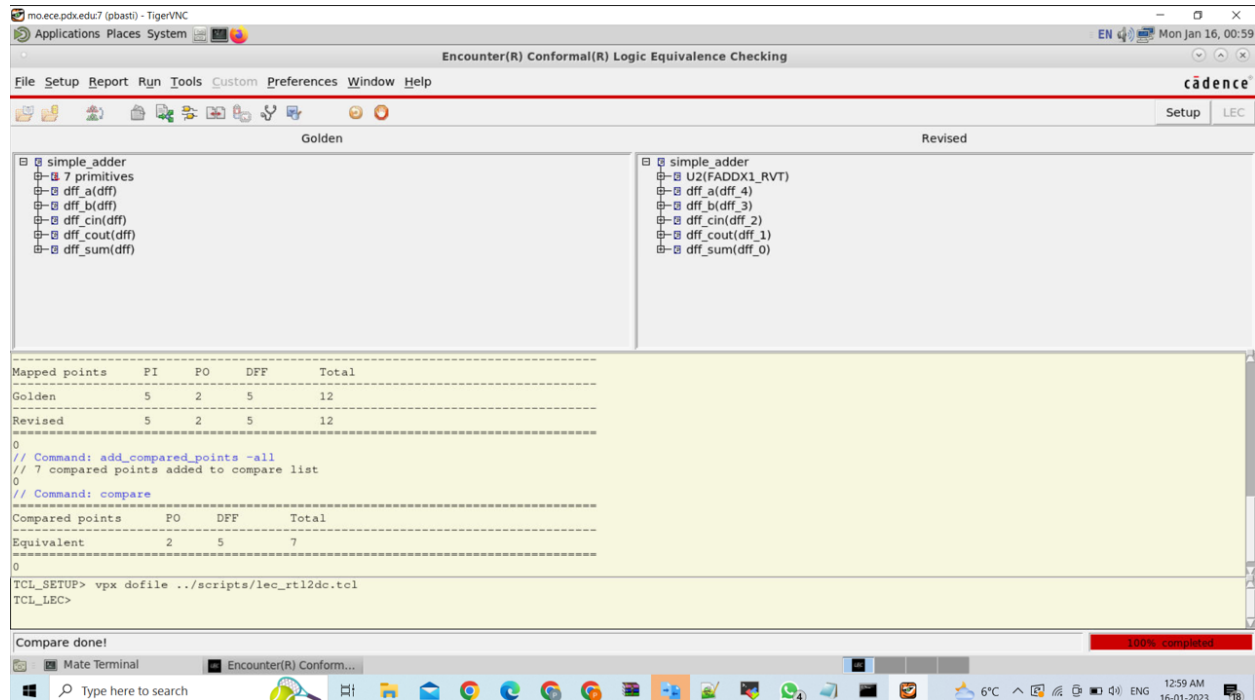
vmap - It defines the mapping between a logical library name and a directory

vlog - Compiles all the verilog files

vsim - starts the VHDL/Questa simulator

## HW\_LAB\_1\_D:

## LEC equivalency



## LEC command description

read\_design - This reads the RTL/netlist or the library files required for the lec run

set\_system\_mode - For switching of system modes

add\_compared\_files - To specify which mapped points conformal compares

Compare - compares the points in the list and checks if key points are equivalent or not

## HW\_LAB\_1\_E:

<https://github.com/preetambasti/ECE-581-winter-2023>

