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Dr. M. S. Sheshgiri Campus, Belagavi

A Digital System Design using Verilog Open ended Project Report on

"*Railway gateway system*"

in

ELECTRONICS AND COMMUNICATION ENGINEERING

By

1 Preeti Paschapuri	**SRN: 02FE22BEC053**
2 Priyanka Budihal	**SRN: 02FE22BEC054**
3 Priyanka Patil	**SRN: 02FE22BEC055**
4 Priyanshu Porwal	**SRN: 02FE22BEC056**

UNDER THE GUIDANCE OF

Prof. Pooja Mahajan

DEPARTMENT OF
ELECTRONICS AND COMMUNICATION ENGINEERING

K. L. E. Dr. M. S. SHESHGIRI
COLLEGE OF ENGINEERING AND TECHNOLOGY,
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Chapter 1

Problem statement

Implementation of a model using Verilog coding for railway gateway system with the help of stepper motor and DIP switch control input.

Chapter 2

Objectives

1. To implement the Railway gateway system using Verilog coding, understanding the rotation of the stepper motor, output and input pins.
2. Implementing the Verilog coding techniques learnt during the academic semester to gain a better understanding of the code flow and the peripherals.
3. Controlling the stepper motor according to the result action required by the gate.

Chapter 3

Introduction

The project is all about creating a smart railway gate system using Verilog. We wanted to make railway crossings using the peripherals present on the Xilinx Spartan 3 board. So, we used the logic to control important parts like the gate motor, switches, and lights.The aim is to make the system understand commands from switches and show what's happening with lights, while moving the gate precisely.

We have used tools such as ISE Design Software for coding and dumping the code on the board.

Chapter 4

Methodology

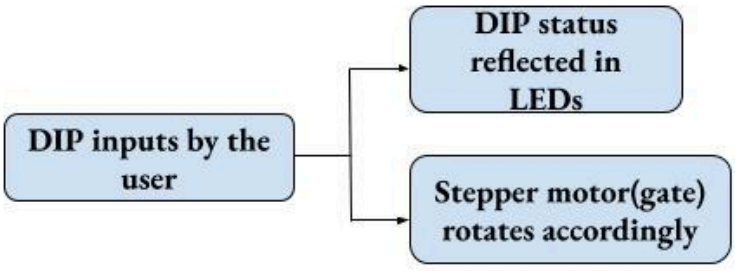
The Railway gateway system mainly operates in such a way that the arrival of the train is known prior. Here, in this virtual implementation of the railway system we are making use of 2 indicators indicating the status of the train whether it is passing, has passed, just passed or not arrived at all.

Here these indicators are input by the user through the DIP switches present on the Xilinx Spartan 3 board, which are then connected to external LEDs to reflect the input given by the user, the stepper motor then rotates to close or open the gate based on the condition input, considering the 2 LEDs as LED1 and LED2 the following flow is maintained

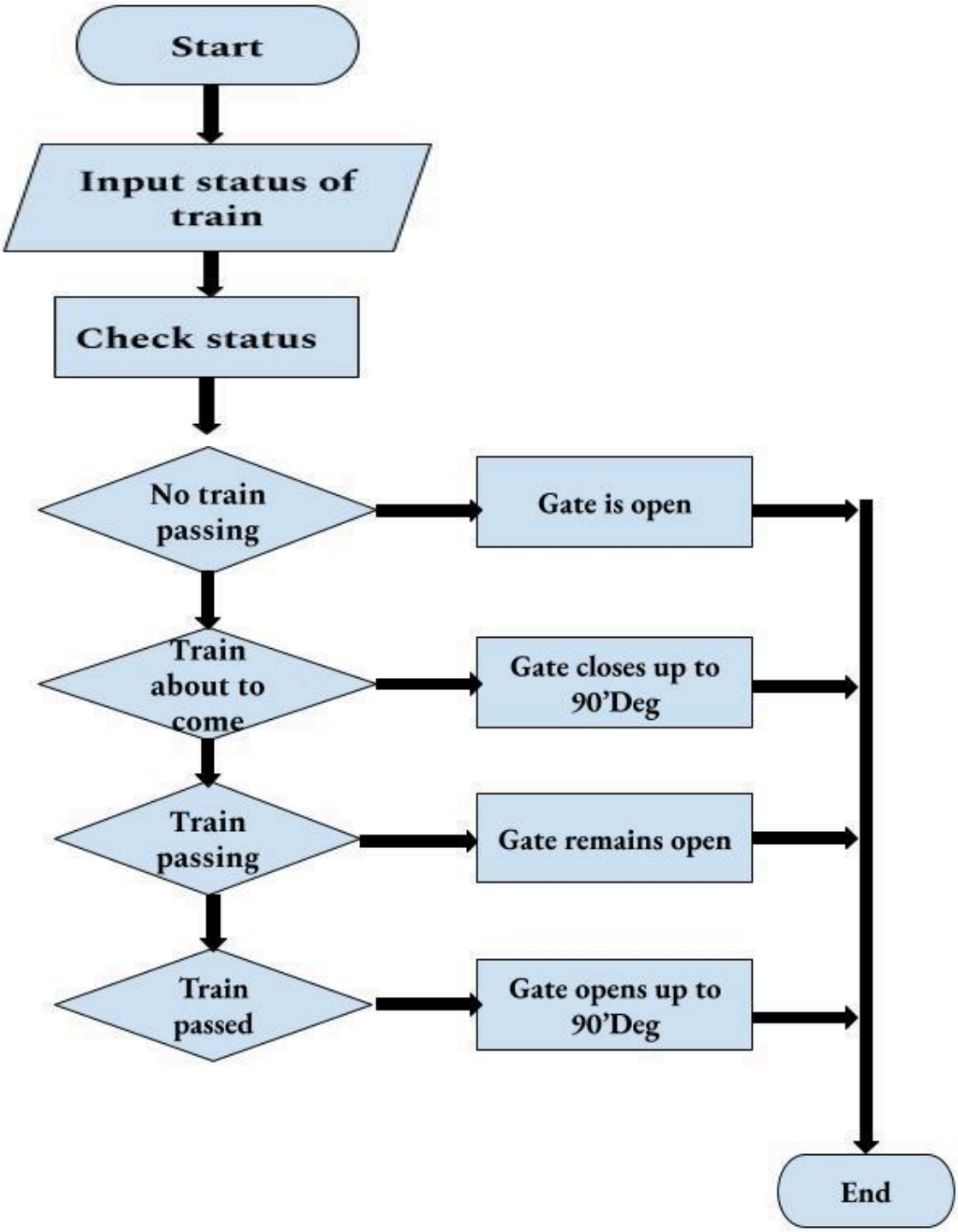
- LED1 off LED2 off: Stepper motor rotates anticlockwise 90’Deg.
- LED1 off LED2 on: Stepper motor remains as it is.
- LED1 on LED2 on: Stepper motor rotates clockwise 90’Deg.
- LED1 on LED2 off: Stepper motor remains as it is.

The work flow of the system is pictorially represented by the following ways:

Block diagram



Flowchart


Start
Input status of train
Check status
No train passing
Gate is open
Train about to come
Gate closes up to 90'Deg
Train passing
Gate remains open
Train passed
Gate opens up to 90'Deg
End

Chapter 4

Implementation

1. Function table:

LED1	LED2	Action
0	0	OPEN
0	1	HOLD
1	0	CLOSE
1	1	HOLD

2. Verilog code:

```
module openEndedmon(out, pins, clk, dir);
output [3:0]out;
output [1:0]pins;

input clk;
input [1:0]dir;
reg [3:0]out;
reg [3:0]t = 4'b0111;
reg [19:0]temp=20'd0;
reg [1:0]pins;

wire clk1;

clk_divider x(clk1, clk);

always@(posedge clk1 )
begin
    temp=temp+1;

    if (temp > 20'd50)begin
        temp = 20'd0;
```

```
    end

    case(dir)
    2'b10: begin
                pins = dir;
                if (temp < 20'd50 )begin
                        t = {t[2], t[1], t[0], t[3]};end// Rotate
clockwise by 90 degree
                else
                        t=4'b0000;
            end
    2'b11: begin pins = dir;    t=4'b0111;  temp=20'd0;end
    2'b01: begin
            pins = dir;
                if (temp < 20'd50 ) begin
                        t = {t[0], t[3], t[2], t[1]};end// Rotate
counterclockwise by 90 degree
                else
                    t=4'b0000;
            end
    2'b00: begin pins = dir;    t=4'b0111;  temp=20'd0; end
    endcase
    out =t;
end
endmodule


module clk_divider(clk1, clk);
input clk;
output clk1;
reg [25:0]temp;
initial begin
temp = 26'd0;
end

always@ (posedge clk)
begin temp= temp+1'b1; end
assign clk1 = temp[18];
endmodule
```

3. UCF File:

```
# PlanAhead Generated physical constraints

NET "clk" LOC = P79;
NET "dir[1]" LOC = P21;
NET "dir[0]" LOC = P27;
NET "out[3]" LOC = P178;
NET "out[2]" LOC = P176;
NET "out[1]" LOC = P175;
NET "out[0]" LOC = P169;
NET "pins[1]" LOC = P57;
NET "pins[0]" LOC = P61;
```

Variable Description:

1. ‘dir’ has the status input by the user via DIP pins, dir[1] represents LED1, dir[0] represents LED2.

2. ‘out’ activates the coils of the stepper motor , out is a vector of 4 bit for each coil of the stepper motor.

3. ‘pins’ this vector is used to simply copy the value of ‘dir’ which is input through DIP pins, this is done so that the values entered through DIPs can be reflected by the LEDs, therefore depicting the train arrival status.

Chapter 5

Results

1. Synthesis report:

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Sat 8. Jun 12:33:30 2024	0	7 Warnings (0 new, 0 filtered)	5 Infos (0 new, 0 filtered)
Translation Report	Current	Sat 8. Jun 12:33:34 2024	0	0	0
Map Report	Current	Sat 8. Jun 12:33:36 2024	0	0	2 Infos (0 new, 0 filtered)
Place and Route Report	Current	Sat 8. Jun 12:33:41 2024	0	0	2 Infos (0 new, 0 filtered)
Power Report					
Post-PAR Static Timing Report	Current	Sat 8. Jun 12:33:43 2024	0	0	6 Infos (0 new, 0 filtered)
Bitgen Report	Current	Sat 8. Jun 12:33:46 2024	0	0	1 Info (0 new, 0 filtered)

2. Timing report:

```
Timing Summary:
---------------
Speed Grade: -5

   Minimum period: 11.013ns (Maximum Frequency: 90.801MHz)
   Minimum input arrival time before clock: 3.206ns
   Maximum output required time after clock: 6.306ns
   Maximum combinational path delay: No path found

Timing Detail:
--------------
All values displayed in nanoseconds (ns)
```

Chapter 6

Conclusion

Implementation of the railway gateway system was successfully carried out by precisely controlling the rotating angle of stepper motor to open or close the railway gate based on the condition and LEDs to indicate the train arrival and departure.