SAURAV RANJAN NAYAK

Electrical and Electronics Engineering

Test Engineer, Tessolve Semiconductors

Male, 23 years

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PROFESSIONAL SYNOPSIS

- TESSOLVE SEMICONDUCTOR as **Post Silicon Validation Engineer** from DEC 2016
- INFOSYS LIMITED as SYSTEMS ENGINEER

EDUCATIONAL QUALIFICATIONS

Qualification	School/College	Board/ University	Year of Passing	Percentage/ CGPA
B-Tech	IIIT BHUBNESWAR	IIIT	2016	8.14
XII	CHINMAYA VIDYALAYA ENGLISH MEDIUM SCHOOL, ROURKELA	ISC	2012	88.16
X	ISPAT ENGLISH MEDIUM SCHOOL,ROURKELA	ICSE	2010	84.14

INTERNSHIP / PROJECTS

- **Vacational Training in SAIL, ROURKELA STEEL PLANT from 12th may 2014 to 11th june 2014 in Electrical and Repair shop.**
- **Worked on back end devlopment of BIKE RENTAL service website (Training Project at Infosys)**
- **Worked on FEEROLITE_CAT6 for QUALCOMM for GIONEE S10(SNAP DRAGON 427)**
- **WORKING ON NAZGUL FOR QUALCOMM (SNAPDRAGON 835)**

ACADEMIC ACHIEVEMENTS

- I have secured 44.01 marks in GATE 2016

SKILLS

Verigy 93K
ATPG pattern generator
Built-in Memory testing
JTAG/BSDL
PYTHON
PLSQL/SQL
RDBMS

PROJECT DETAILS

- Worked on Testing of SnapDragon 427(MSM8920). Testing was focused on Memory testing, ATPG and TDF patterns. SnapDragon 427 is currently being used in Gionee S10C.
  - In this Project we have focused on Test Time reduction of each wafer and finding failures. We were doing failure analysis with help of Qualcomm Tools.
  - Yield analysis and comparison with different wafers was done for each revision of Program we release
  - Yield debug was done on the blocks which has seen fallouts.
  - Quality analysis of each program has to be done by us. We ensure that each level of core testing has been done on entire wafer.

D/47,SECTOR-9 ROURKELA-9 ODISHA