

Chapter 1 Introduction

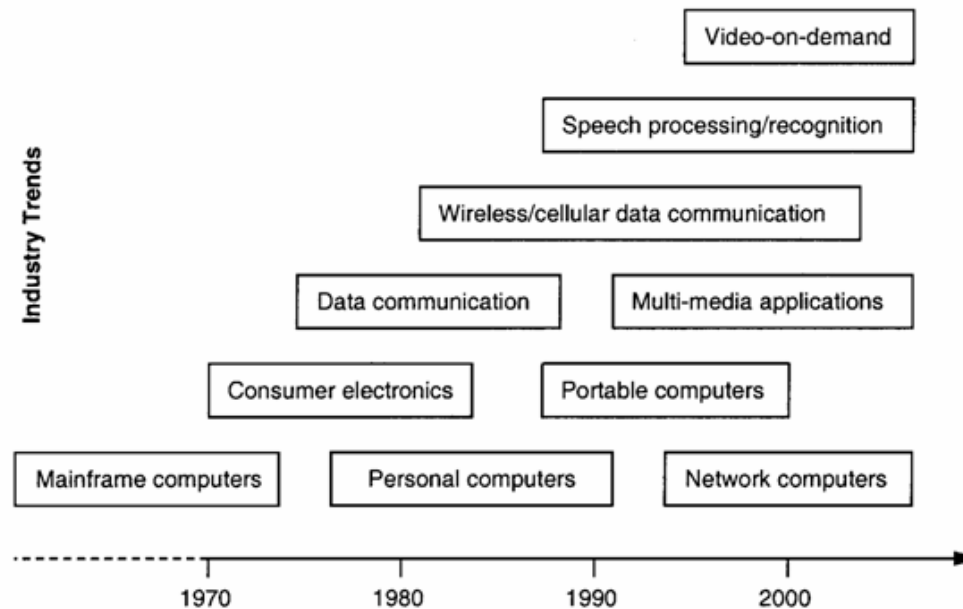
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1.1 Historical Perspective

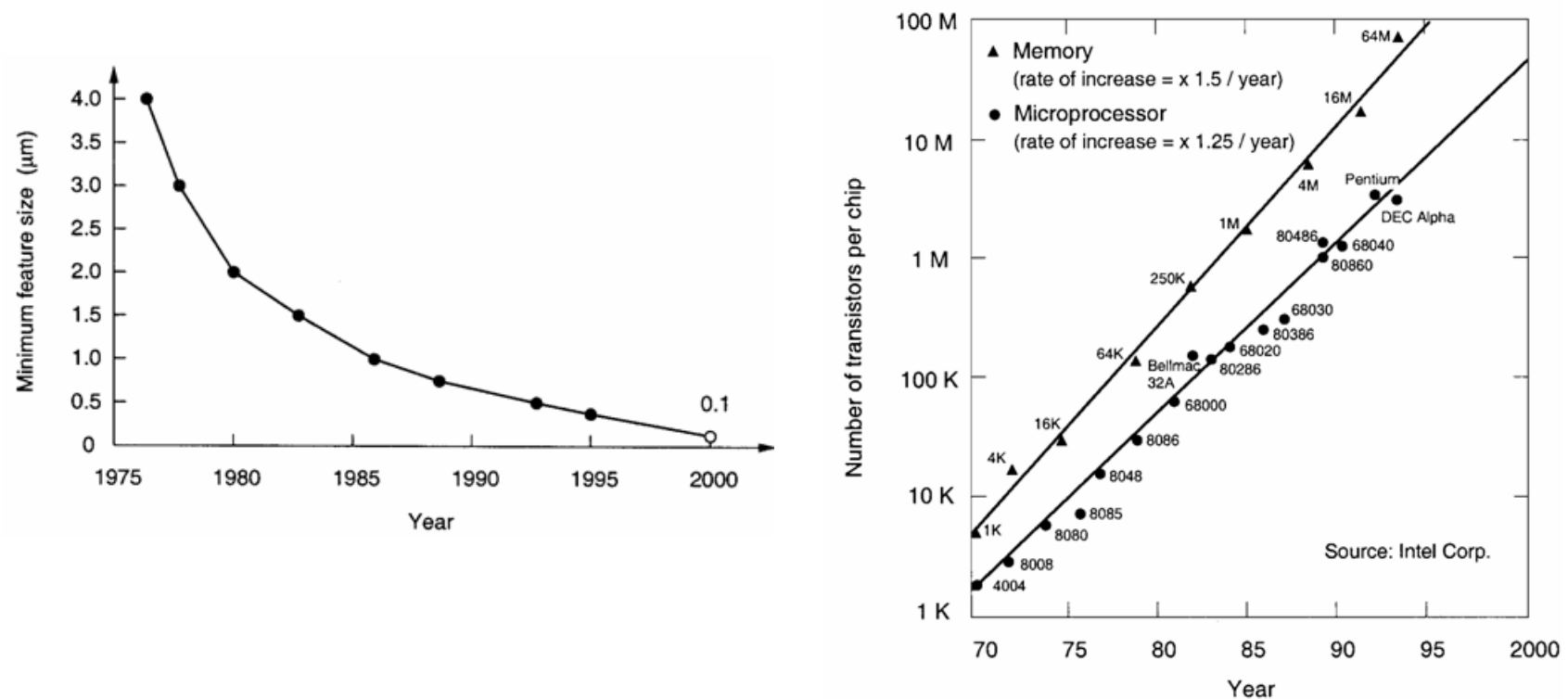
- Evolution of logic complexity in integrated circuits

Era	Date	# of logic blocks
MSI	1967	20-200
LSI	1972	200-2000
VLSI	1978	2000-20000
ULSI	1989	> 200000

- Prominent driving trends in information service technologies



- ❑ CMOS technology advances
 - ❑ Device scaling with smaller transistor feature size
 - ❑ Increasing operating speeds and packing density
 - ❑ Increasing process complexity and fabrication cost
- ❑ Evolution of minimum feature size and level of integration

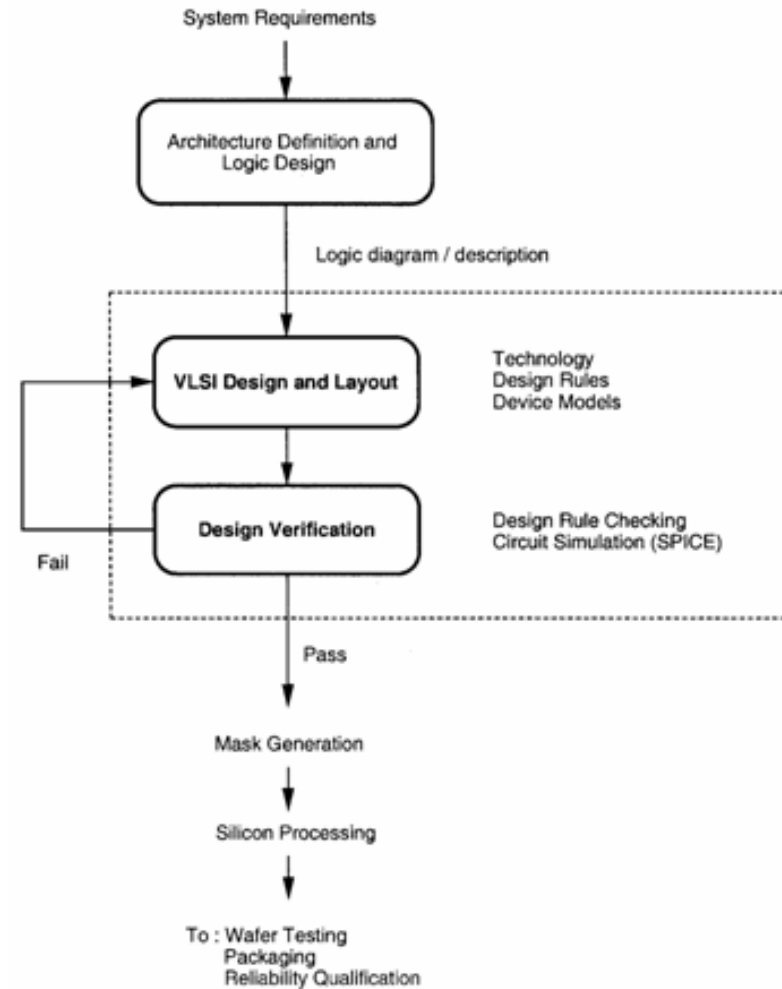


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- Classifications of digital integrated circuits
 - NMOS logics
 - NMOS logic with resistive load
 - NMOS logic with depletion-mode load
 - NMOS logic with enhancement-mode load
 - CMOS logics
 - Static circuits
 - Classical CMOS
 - Transmission-gate CMOS
 - Cascade voltage switch logic (CVSL)
 - Dynamic circuits
 - Domino logic
 - NORA logic
 - TSPC logic

A Digital Circuit Design Example

□ Design flow for digital integrated circuits

- Define the logic functionality
- Required specifications include:
 - Operating speed
 - Chip area
 - Power consumption
 - Noise margins
- Circuit performance is verified during design and layout phases
- Design iteration may be needed during design and layout phases
- Tradeoff is typically involved in circuit designs



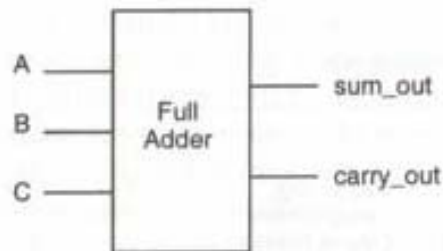
❑ One-bit binary full-adder with 0.8- μm CMOS

❑ Specifications:

- ❑ Propagation delay of sum and carry_out signals < 1.2 ns (worst case)
- ❑ Transition delay of sum and carry_out signals < 1.2 ns (worst case)
- ❑ Circuit area < 1500 μm^2
- ❑ Dynamic power dissipation (@ $V_{\text{DD}} = 5 \text{ V}$ and $f_{\text{max}} = 20 \text{ MHz}$) < 1 mW

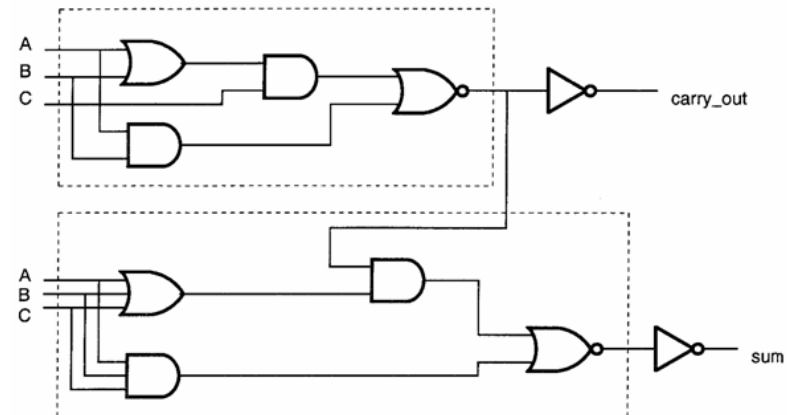
❑ Boolean description:

- ❑ Input: A, B and C
- ❑ Output: sum_out, carry_out

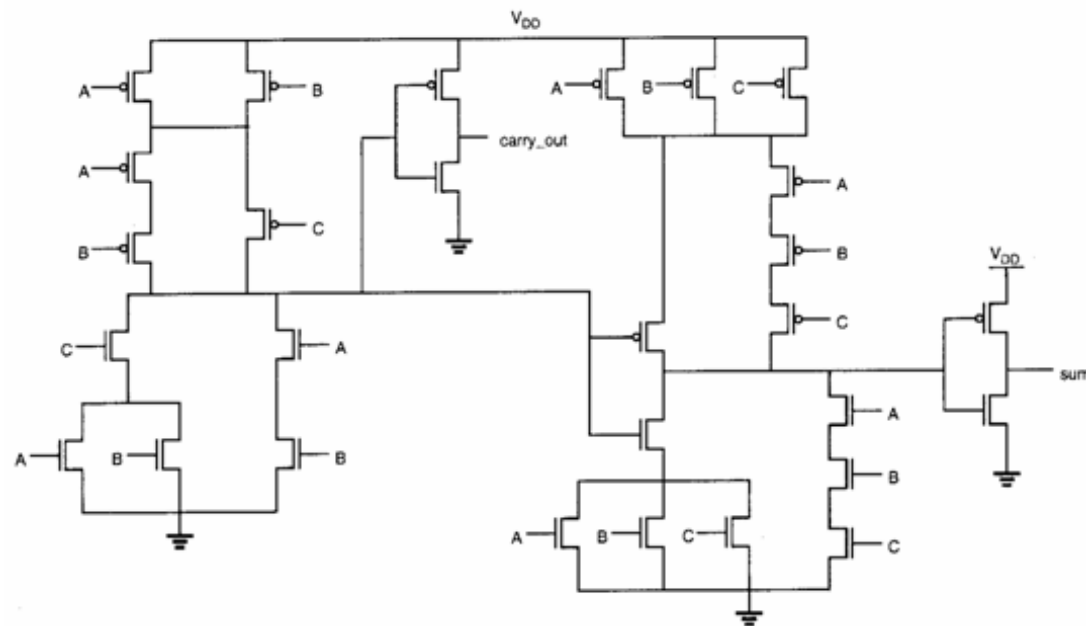


A	B	C	sum_out	carry_out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

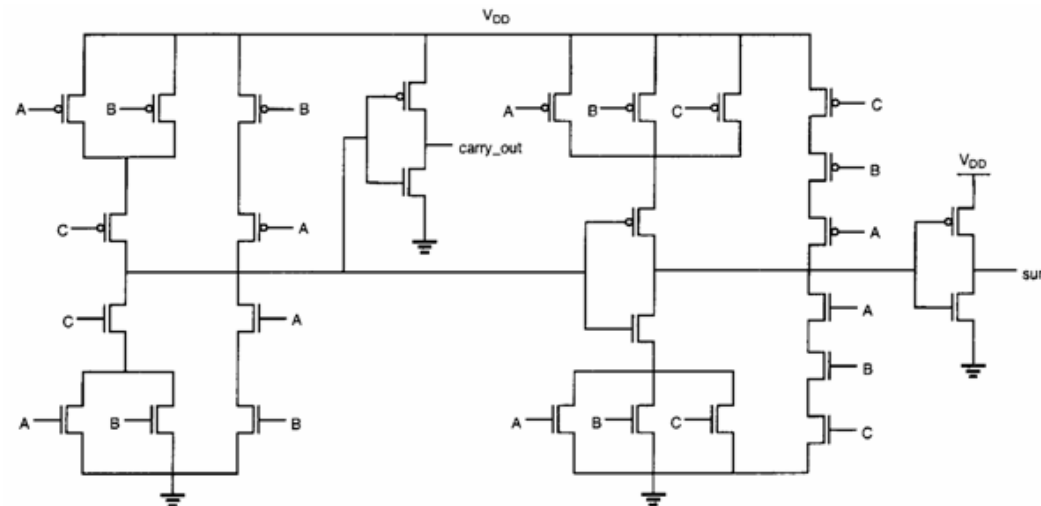
□ Gate-level schematic



□ Transistor-level schematic



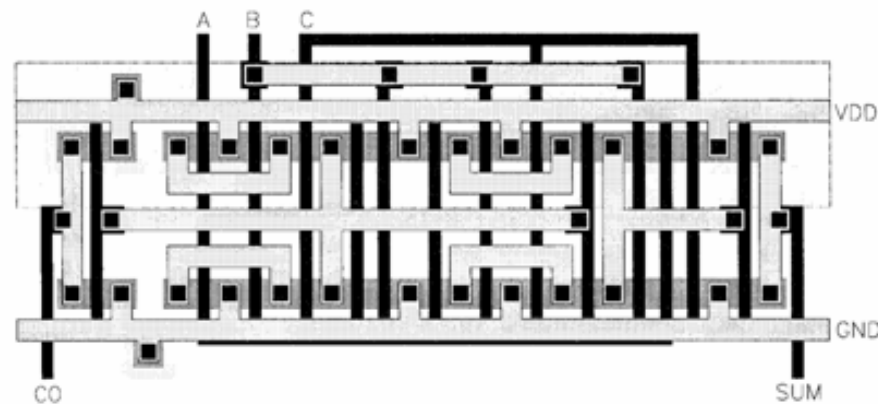
□ Alternative transistor-level schematic



□ Preliminary layout

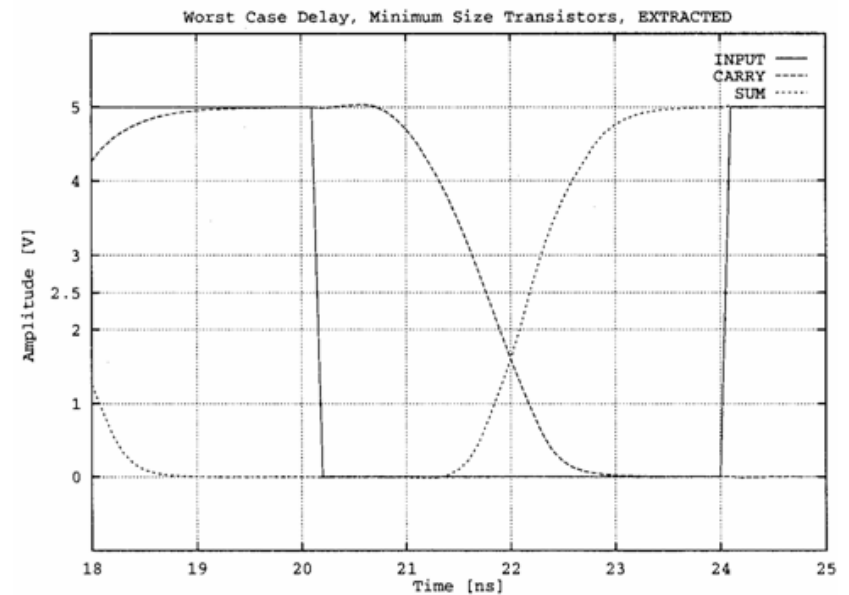
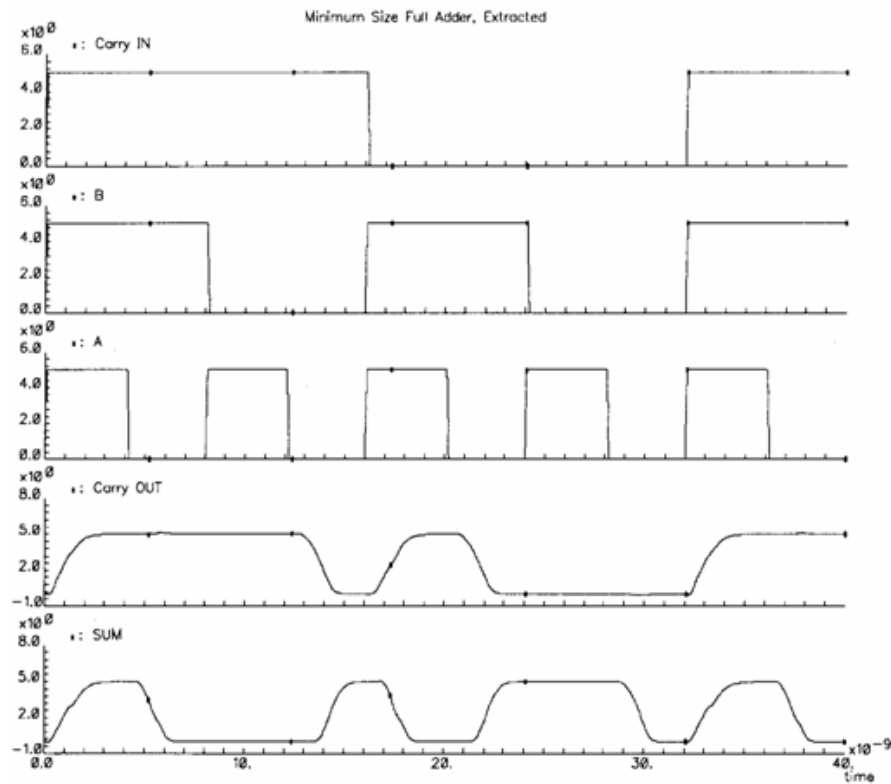
□ Minimum device size ($2\text{ }\mu\text{m}/0.8\text{ }\mu\text{m}$) for NMOS and PMOS

□ Total Si area = $1134\text{ }\mu\text{m}^2$

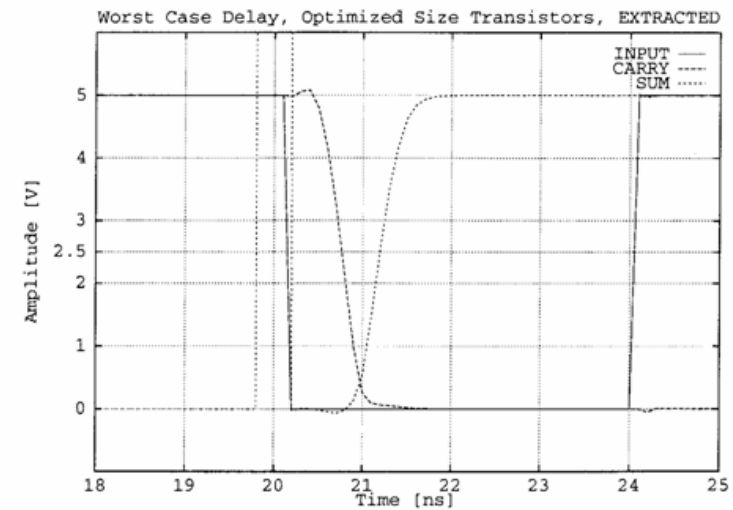
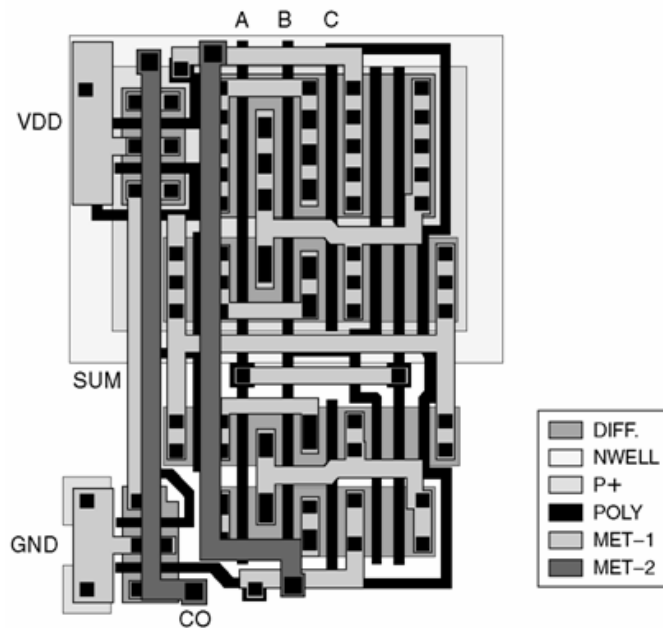


□ Post-layout simulation

- Parasitics extracted from the layout are included in the simulation
- Worst-case delay = 2.0 ns > 1.2 ns
- The carry_out is used to generate sum output (critical path)

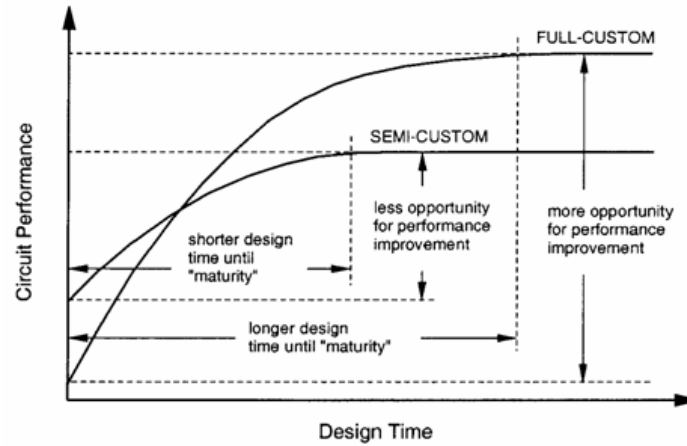


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- Modified full-adder design
 - Resize PMOS and NMOS devices
 - Chip area = $1290 \mu\text{m}^2$
 - Worst-case delay = 1.0 ns
 - Dynamic power dissipation = $460 \mu\text{W}$

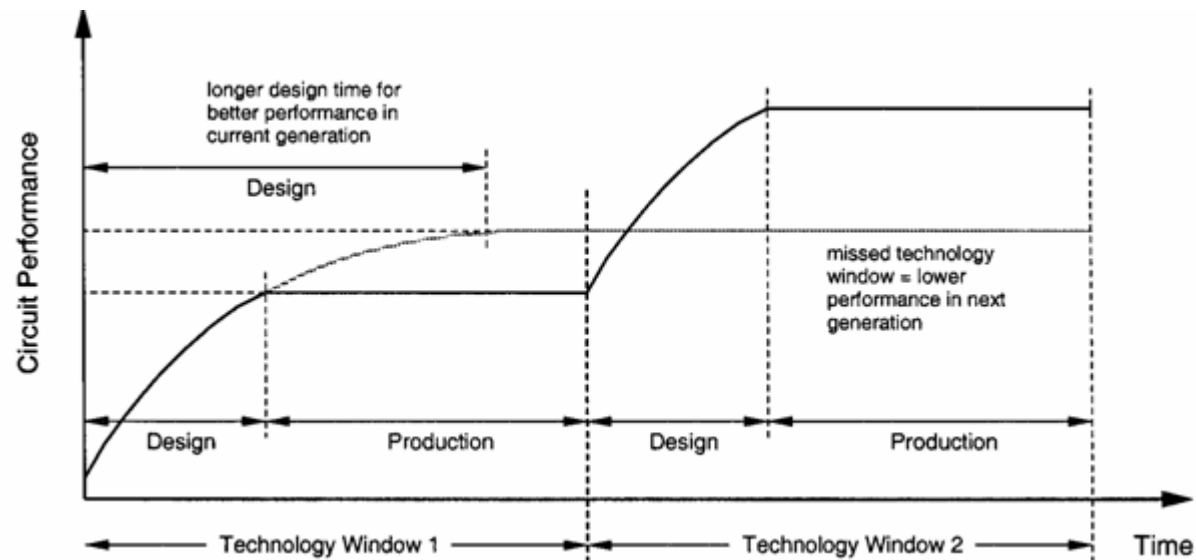


1.3 VLSI Design Methodologies

□ Performance versus design cycle



□ Technology window

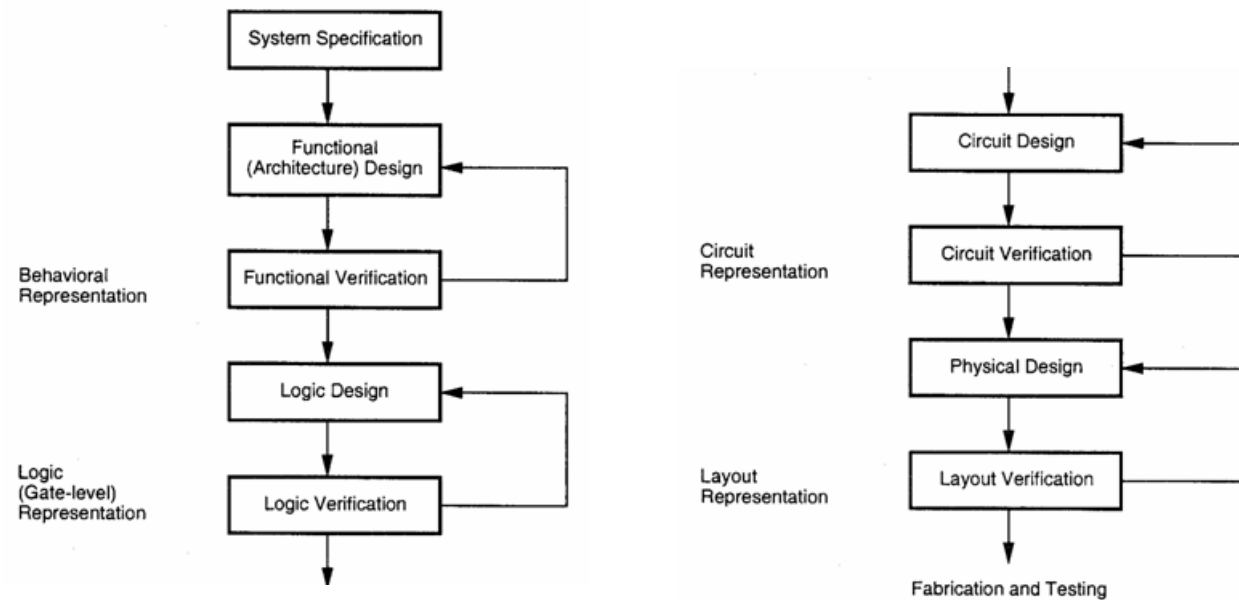


□ VLSI design flow

□ Representations or abstractions:

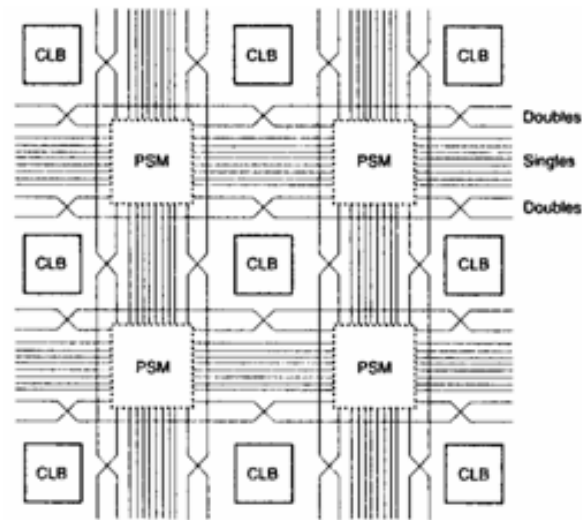
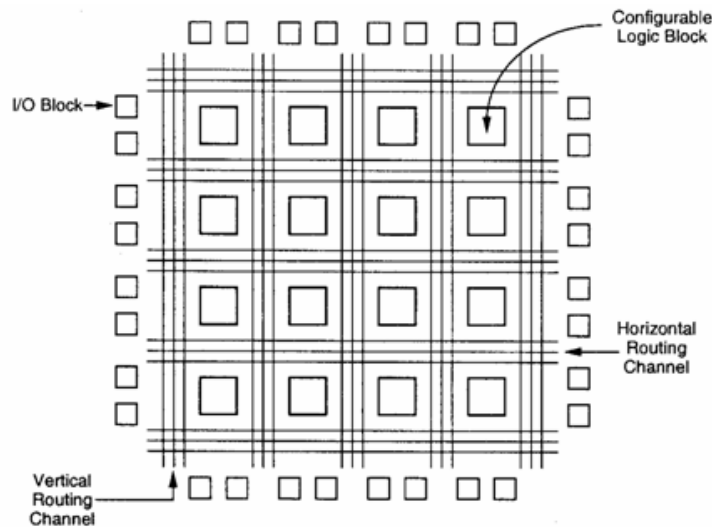
- Behavior representation
- Logic representation
- Circuit representation
- Layout representation

□ Verification is essential in every step during the process

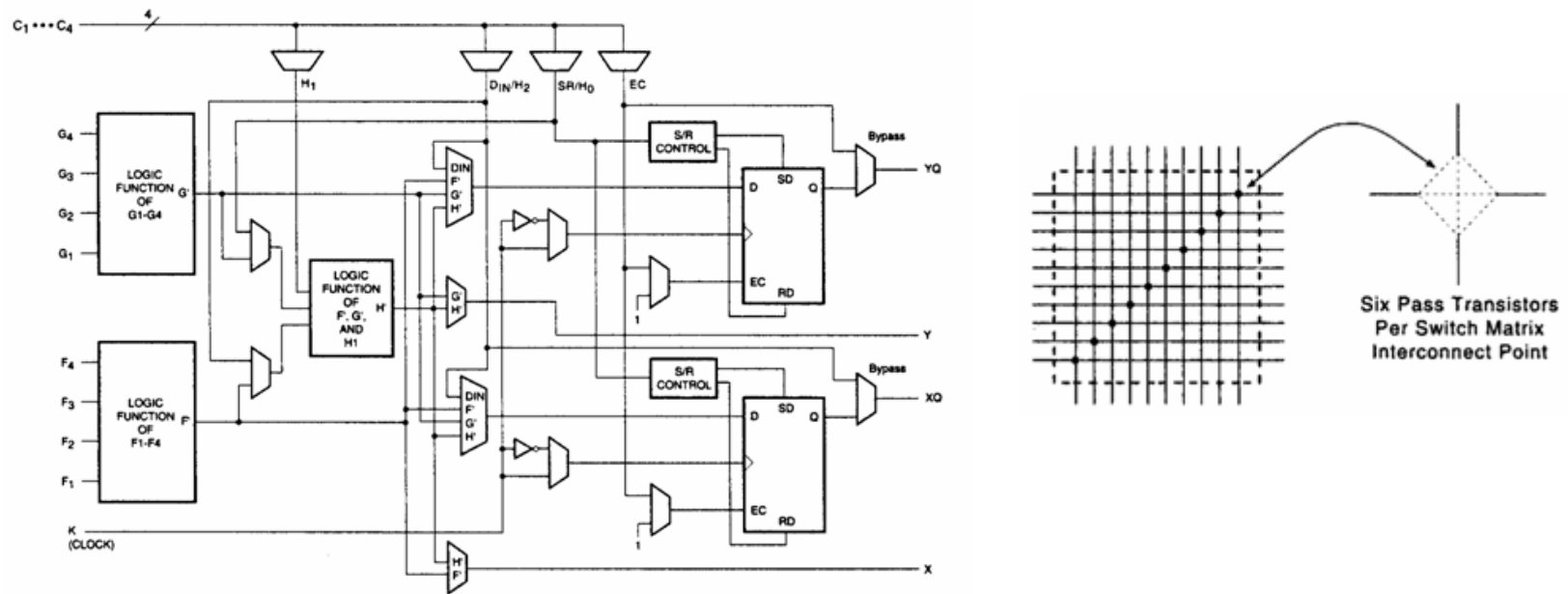


1.4 VLSI Design Styles

- ❑ Field programmable gate array (FPGA)
 - ❑ Logic gates with programmable interconnects
 - ❑ I/O buffers, configurable logic blocks (CLBs) and programmable interconnect structures
 - ❑ Requires no process steps for logic realization
 - ❑ For fast prototyping and small-volume ASIC production (short turn-around time)
 - ❑ Design flow of FPGA:
 - ❑ Behavioral description of its functionality
 - ❑ Technology-mapped into circuits or logic cells
 - ❑ Assigns logic cells to FPGA CLBs and determines the routing pattern



- Configurable logic blocks (CLBs)
 - Independent combinational function generators (memory look-up table)
 - Clock signal terminal
 - User-programmable multiplexers
 - Flip-flops
- Programmable interconnect
 - Six pass transistors per switch matrix interconnect point
 - Accomplished by data in RAM cells



- Gate array design

- Uncommitted transistors separated by routing channels

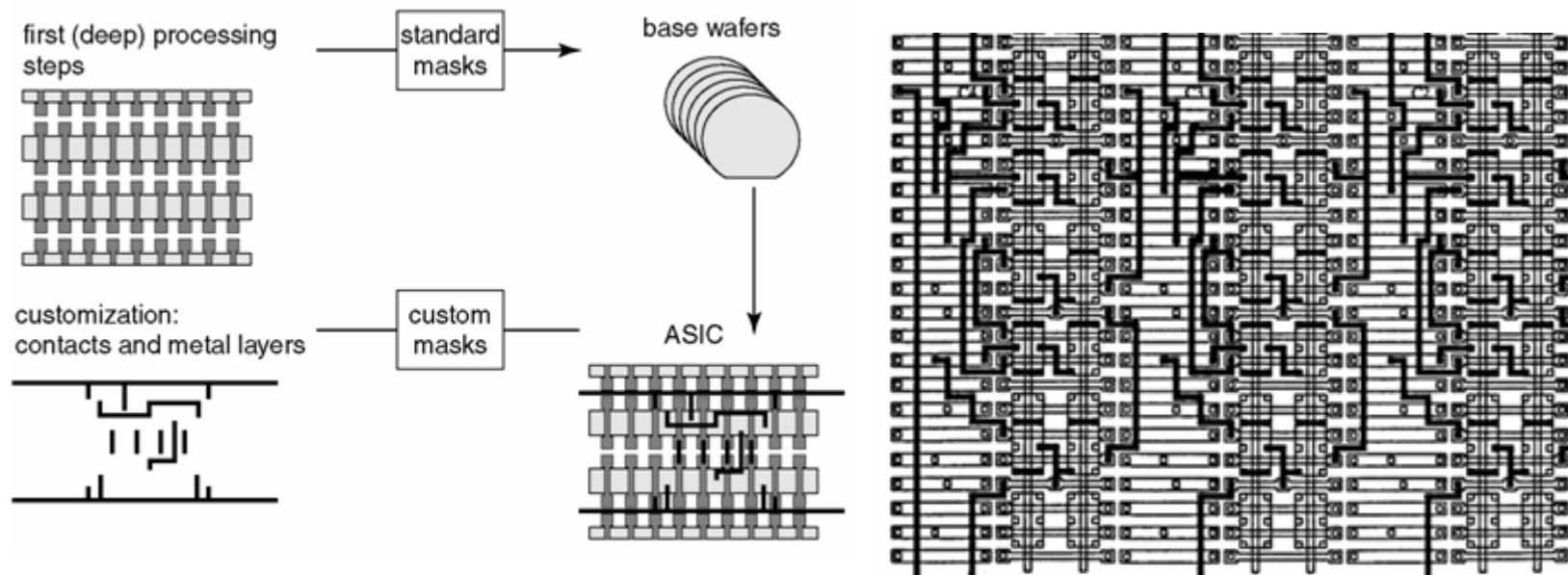
- Circuit implementation:

- 1st phase: generic masks for uncommitted transistors on each GA chip (stored)

- 2nd phase: Customization by (multiple) metal fabrication process

- Ranks second after FPGA with a turn-around time of a few days

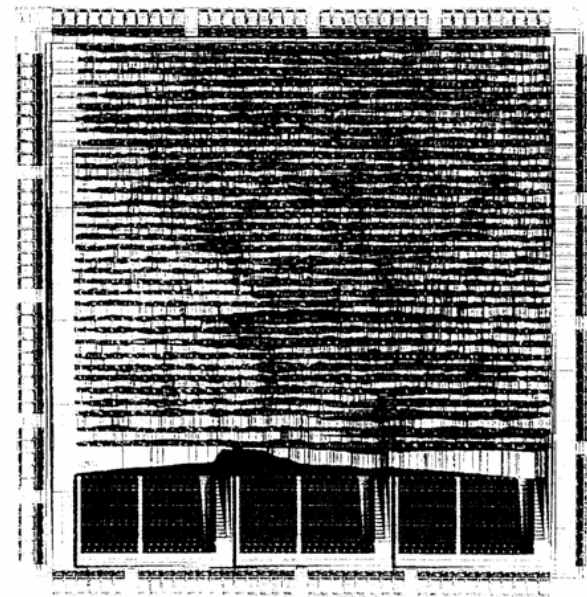
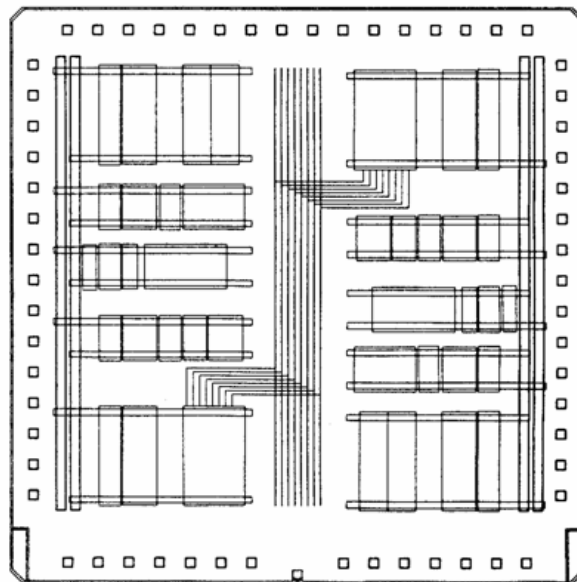
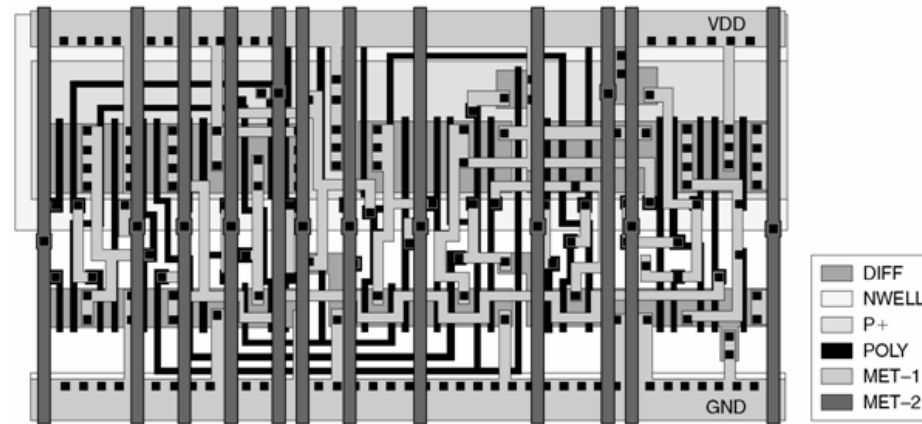
- Chip utilization factor is higher than that of the FPGA



- ❑ Standard-cell based design

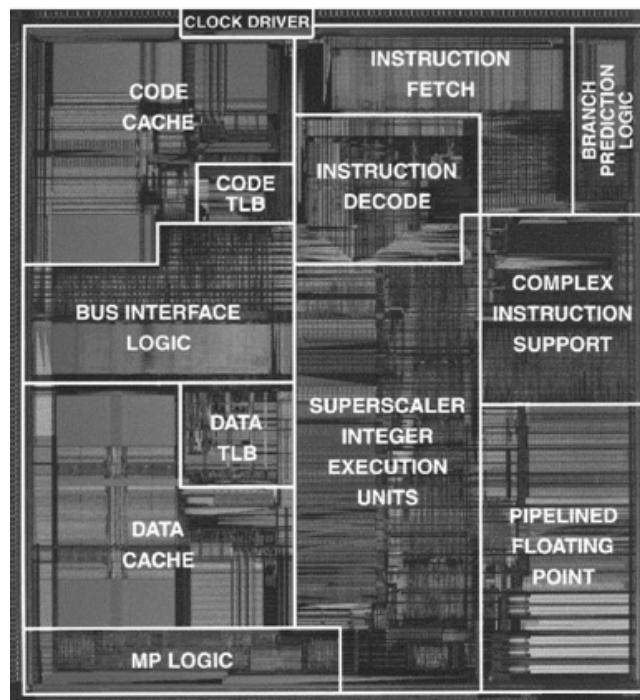
- ❑ Commonly used logics are developed, characterized and stored in a standard cell library
- ❑ Cell library includes:
 - ❑ Delay time versus load capacitance
 - ❑ Circuit simulation model
 - ❑ Timing simulation model
 - ❑ Fault simulation model
 - ❑ Cell data for place-and-route
 - ❑ Mask data
- ❑ Standard cell arrangement:
 - ❑ Fixed cell height
 - ❑ Parallel power and ground rails
 - ❑ Input and output pins are located on the upper and lower boundaries
 - ❑ Cells are placed side by side in standard-cell based design
- ❑ The required logic circuits are realized using the cells in the library
- ❑ Complete mask sets are developed for chip fabrication
- ❑ One of the most prevalent design style for ASIC applications

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- Layout of a standard cell and floorplan of a standard-cell based design



❑ Full custom design

- ❑ Design and develop the IC from scratch
- ❑ Possibly to achieve the highest performance compared with other design styles
- ❑ Highest development cost and design cycle time
- ❑ Design reuse is coming popular to alleviate the design effort
- ❑ Suitable for design of high-performance processors, FPGAs and memory chips



1.5 Design Quality

☐ Testability

- ☐ Time and effort for chip test increase exponentially with design complexity
- ☐ The test task requires
 - ☐ Generation of good test vectors
 - ☐ Availability of reliable test fixture at speed
 - ☐ Design of testable chip

☐ Yield and manufacturability

- ☐ The ratio of good tested chips to total tested chips
- ☐ Functionality yield:
 - ☐ Testing the chips at lower speed
 - ☐ Identify problems of shorts, opens and leakage current
 - ☐ Detect logic and circuit design failure
- ☐ Parametric yield
 - ☐ Test at the required speed
 - ☐ Delay testing is performed at this stage
- ☐ Consider manufacturability of the chip in the design phase
- ☐ Sufficient tolerance to device fluctuations and margin for measurement uncertainty

☐ Reliability

- ☐ Depends on the design and process conditions
- ☐ Reliability problems:
 - ☐ Electrostatic discharge (ESD) and electrical overstress (EOS)
 - ☐ Electromigration
 - ☐ Latch-up in CMOS I/O and internal circuits
 - ☐ Hot-carrier induced aging
 - ☐ Oxide breakdown
 - ☐ Single event upset
 - ☐ Power and ground bouncing
 - ☐ On-chip noise and crosstalk

☐ Technology updateability

- ☐ Be technology-updated to new design rules
- ☐ Fast migration to new process technology
- ☐ “Dumb shrink” method with uniform scaling is rarely practiced
- ☐ Silicon compilation: generate physical layout from high-level specifications

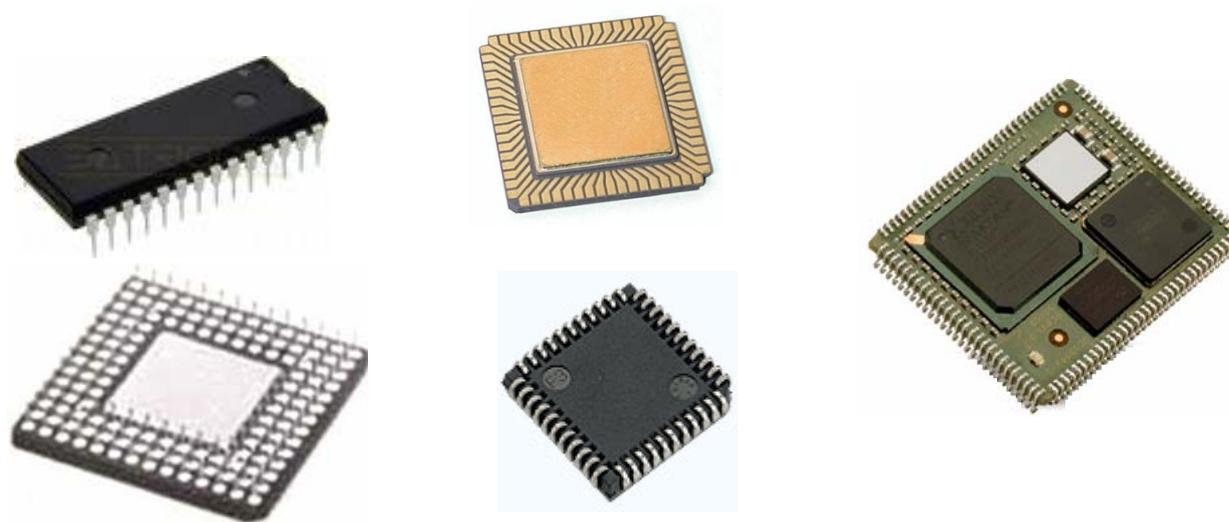
1.6 Packaging Technology

- ❑ Packaging for integrated circuits
 - ❑ Proper packaging technology is critical to the success of the chip development
 - ❑ Package issues have to be taken into consideration in early stages of chip development
 - ❑ Ensure sufficient design margins to accommodate the parasitics of the package
 - ❑ Important packaging concerns:
 - ❑ Hermetic seals to prevent the penetration of moisture
 - ❑ Thermal conductivity
 - ❑ Thermal expansion coefficient
 - ❑ Pin density
 - ❑ Parasitic inductance and capacitance
 - ❑ α -particle protection
 - ❑ Cost
 - ❑ Types of packaging technology
 - ❑ Classified by the method used to solder the package on the printed PCB
 - ❑ Pin-through-hole (PTH)
 - ❑ Surface-mounted technology (SMT)

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- ☐ Dual in-line packages (DIP)
 - ☐ Advantage of low cost
 - ☐ Not applicable for high-speed operations due to the inductance of the bond wires
 - ☐ Maximum pin count is typically limited to 64
 - ☐ Pin grid array (PGA) packages
 - ☐ Offers a higher pin count (several hundreds)
 - ☐ High thermal conductivity especially with a passive or active heat sink
 - ☐ Requires large PCB area
 - ☐ Cost is higher than DIP
 - ☐ Chip carrier packages (CCP)
 - ☐ Leadless chip carrier:
 - ☐ Chip mounted on PCB directly
 - ☐ Supports higher pin count
 - ☐ Problem with difference in thermal coefficient
 - ☐ Leaded chip carrier:
 - ☐ Quad flat packages (QFP)
 - ☐ Similar to leaded chip carrier with leads extending outward
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❑ Multi-chip modules (MCM)

- ❑ Used for very high performance in special applications
- ❑ Multiple chips are assembled on a common substrate in a single package
- ❑ A large number of critical interconnects among the chips are made within the package
- ❑ Important features:
 - ❑ Significant reduction in the overall system size
 - ❑ Reduced package lead counts
 - ❑ Faster operation allowed
 - ❑ Higher implementation cost



1.7 CAD Technology

- ❑ Categories of CAD tools for VLSI chip design
 - ❑ Synthesis tools:
 - ❑ High-level synthesis tools with hardware description language
 - ❑ Address automation of the design phase in the top level
 - ❑ Layout tools:
 - ❑ Floorplanning
 - ❑ Place-and-route
 - ❑ Module generation
 - ❑ Simulation and verification tools
 - ❑ Behavior simulation
 - ❑ Logic level simulation
 - A number of test vectors are applied
 - Verify logic functionality
 - ❑ Timing level simulation
 - ❑ Circuit-level simulation
 - Determine nominal and worst-case delays
 - High computational cost