



Contents

- What is VLSI?
- · An Preview.
- VLSI World.
- Moore Law.
- VLSI Industry.
- Objective for VLSI Design.
- Applications.
- Future of VLSI.

Indentify the Image



This is Called VLSI Advancement!

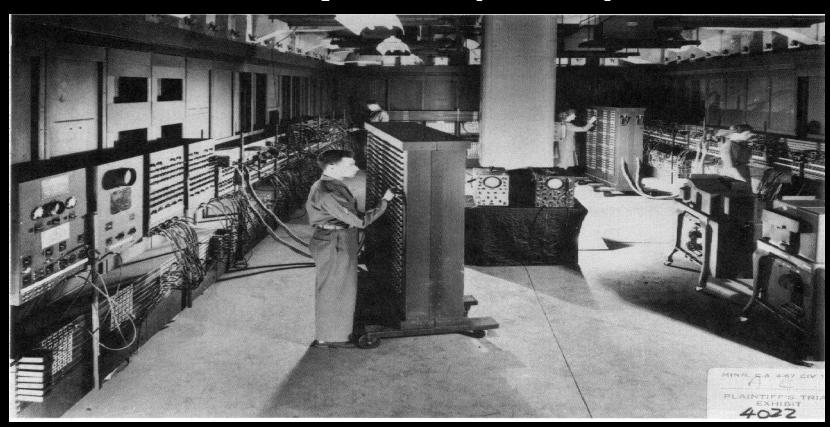


5MB (IBM)-1956, Cost - \$10,000/ 1 MB

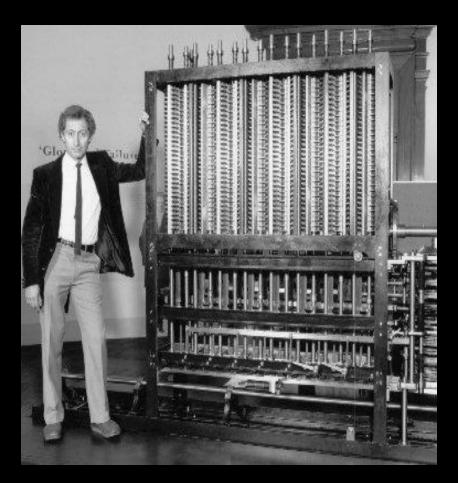


4TB (WB)-2013

ENIAC - The first electronic computer (1946)



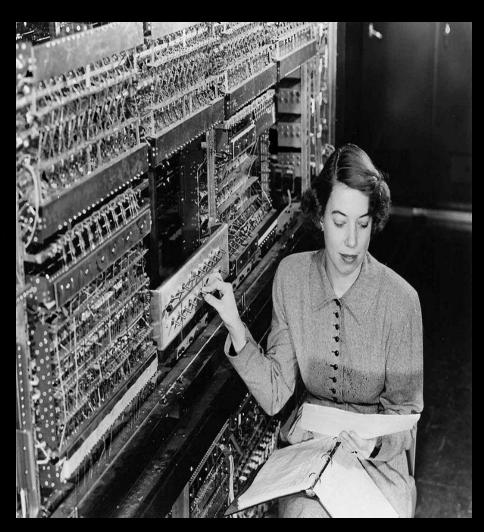
This achieved because of VLSI





Charles Babbage designed the first computer, starting in 1823

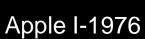
Unbelievable facts

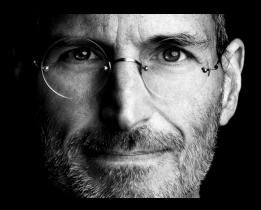


AVIDAC was the first digital computer at Argonne National Laboratory, and began operating in 1953. It was built by the Physics Division for \$250,000. Pictured shown AVIDAC, is pioneer Argonne computer scientist Jean F. Hall. AVIDAC stands for "Argonne Version of the Institute's Digital Automatic Computer" and was based on architecture developed by mathematician John von Neumann.

Apple Development









Apple- 2011

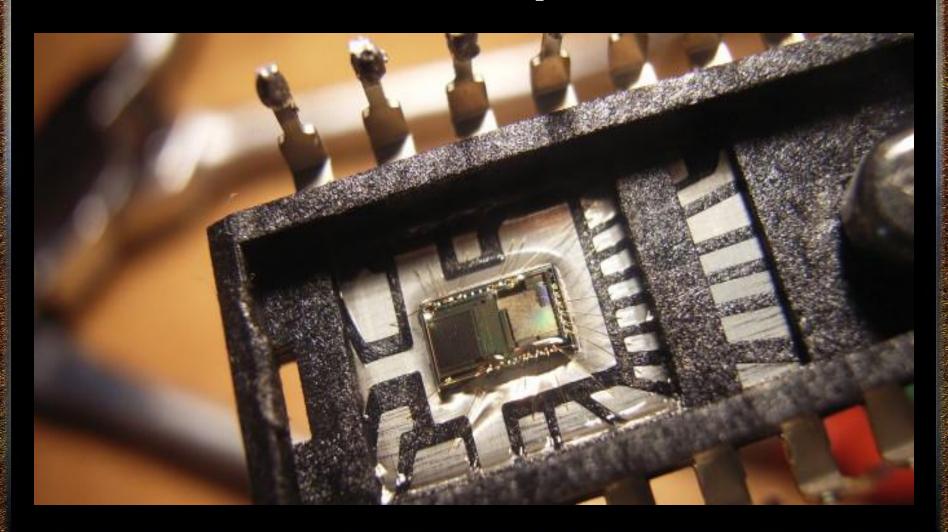
VLSI

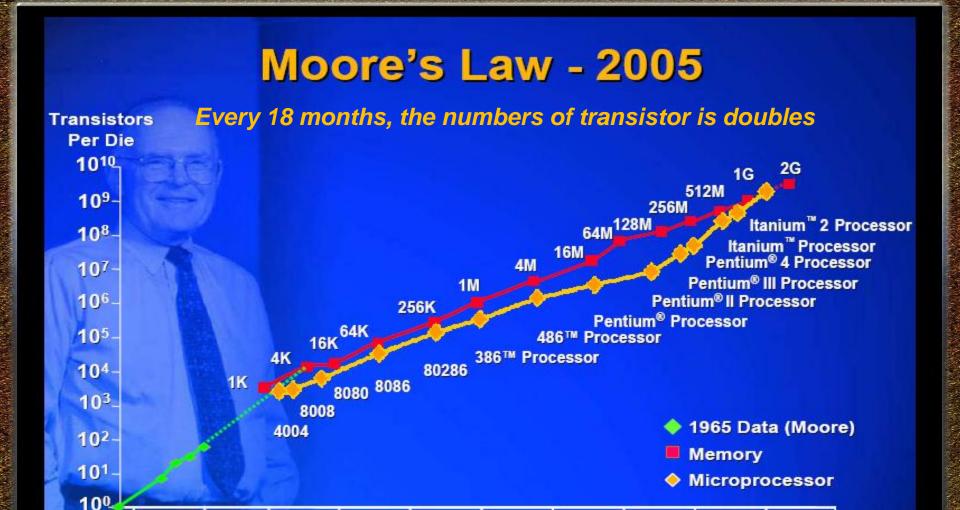
- Very Large Scale Integration (within IC)
- How large is Very Large?
 - √SSI (small scale integration)
 - √ 7400 series, 10-100 transistors
 - ✓ MSI (medium scale)
 - √74000 series 100-1000
 - ✓ LSI 1,000-10,000 transistors
 - ✓VLSI > 10,000 transistors
 - ✓ULSI/SLSI (Not so popular)

Introduction to VLSI

- MOS / CMOS Transistor
- CMOS-Complementary Metal oxide Semiconductor
- Design circuits using MOS/CMOS
 - Understand MOS transistor operation, design eqns.
 - Understand parasitic & perform simple calculations
 - Understand static & dynamic CMOS logic
 - Estimate delay of CMOS gates, networks, & long wires
 - Estimate power consumption
 - Understand design and operation of latches & flip/flops

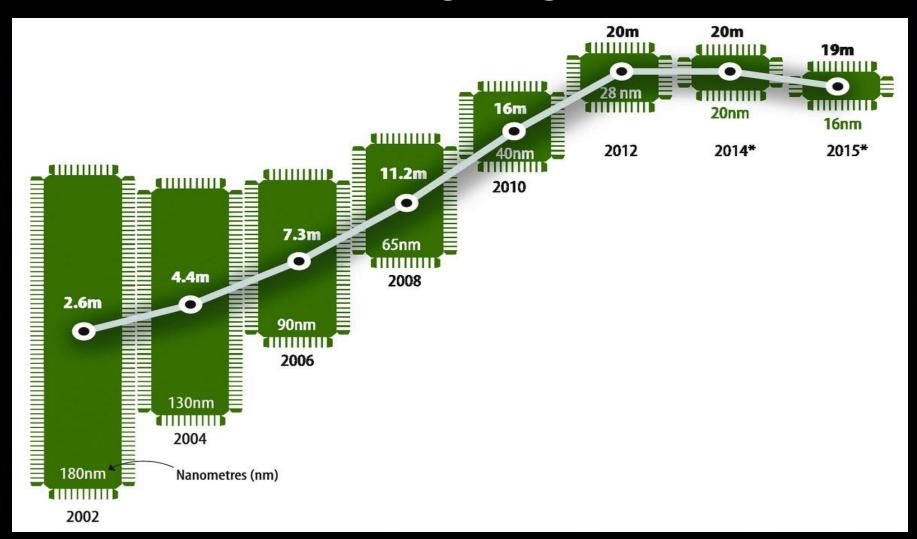
IC Chip



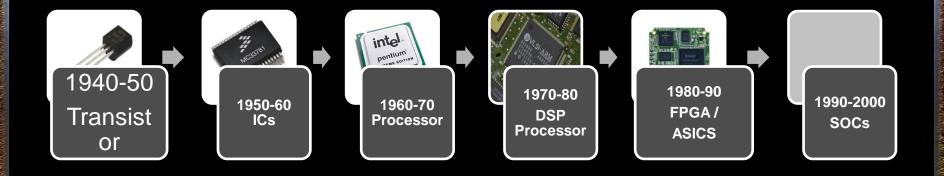


Source: Intel

Timeline



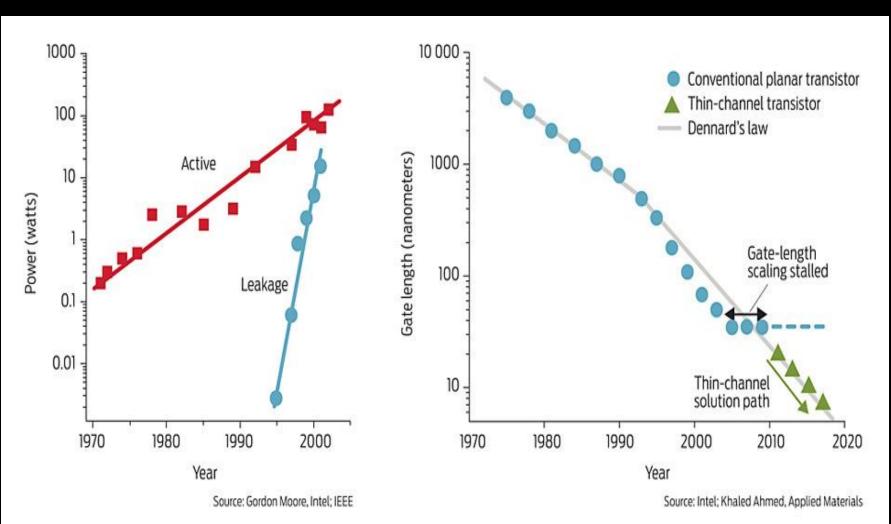
Timeline of Electronic Devices



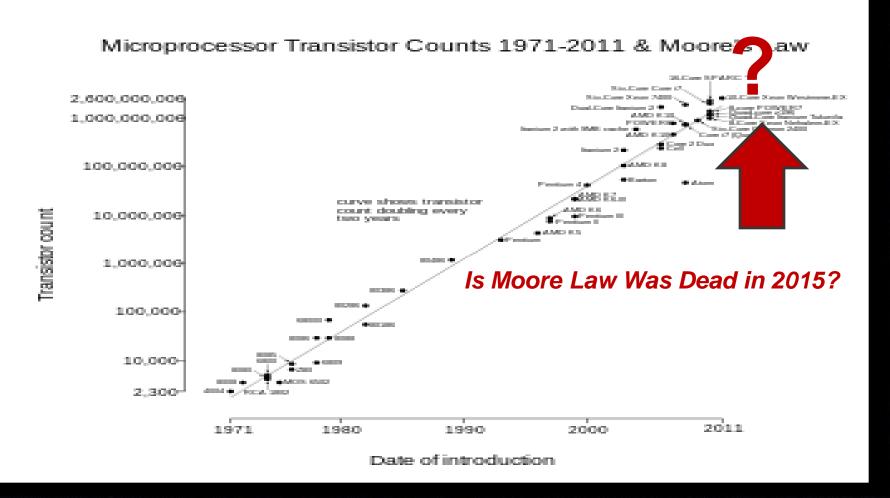
Now a Days 2000-2016>> Sensor, Transducer integrated on SOCs

Entered to Nanotechnology

Power and Size



Remember Moore Law!



Sizes of VLSI Chip

 In 20nm transistors, you can fit around 250 billion of them on a silicon wafer around the size of a fingernail.



 iPad Air 2 has a custom tri-core ARM CPU and custom octa-core PowerFX GPU, for a total of 3 billion transistors on-die.

Cost of VLSI Chips

Transistor is almost free

AIR



3 Billion Transistors+ INR 40K

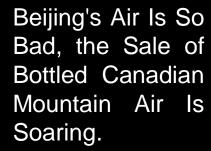


INR 20



I KG-INR 70 Total nos of Grains











One MOS Transistor

Factors consider –VLSI Design

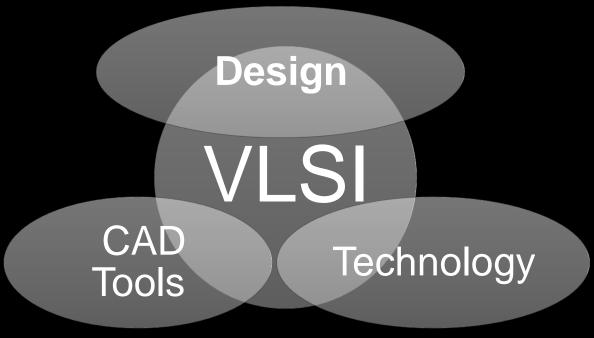
Why Integration

- >Integration improves
 - Size
 - >Speed
 - **≻**Power

- ✓ Power
- ✓ Speed
- √Size
- ✓ Cost
- ➤ Integration reduce manufacturing costs
 - > (almost) no manual assembly

VLSI Domain

Circuit Design, Programming and Analysis



Tools use to Design for Circuits and Layout

IC Manufacturing

VLSI Companies In India

VLSI COMPANIES IN INDIA

- Analog Devices India Product Development Center Designs DSPs in Bangalore
- Bit Mapper Design, development & training
- <u>CG-CoreEl Programmable Solutions</u> Design services in telecommunications, networking and DSP
- <u>Calorex Institute of Technology</u> Courses in VLSI chip design, DSP and Verilog HDL
- ControlNet India VLSI design, network monitoring products and services
- <u>Cypress Semiconductor</u> US semiconductor major Cypress has set up a VLSI development center in Bangalore
- <u>Delsoft</u> Electronic design automation, digital video technology and VLSI design services
- E Infochips ASIC chip design, embedded systems and software development
- EDAIndia Resource on VLSI design centres and tutorials
- Horizon Semiconductors ASIC, VLSI and IC design training
- <u>Microchip Technology</u> Offers VLSI CMOS semiconductor components for embedded systems
- Motorola India IC design center
- <u>Sandeepani</u> VLSI design training courses
- Sanyo LSI Technology Semiconductor design centre of Sanyo Electronics
- <u>Semiconductor Complex</u> Manufacturer of microelectronics equipment like VLSIs & VLSI based systems & sub systems

Syllabus

Unit-1: MOS, CMOS Inverter

Unit-2: Layout and Simulation

Unit-3: Combinational MOS Design

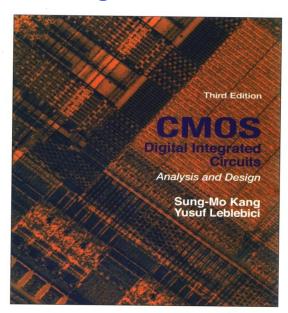
Unit-4: Sequential MOS Design and Clock Distribution

Unit-5: BiCMOS, ASICs

Text Books

Unit 1, 2 & 3

Kang VLSI -TMH



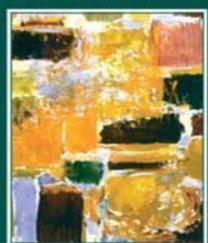
INDIAN EDITION





Rabey, VLSI -PHI DIGITAL INTEGRATED CIRCUITS

A DESIGN PERSPECTIVE SECOND EDITION



Unit 4, 5

JAN M. RABAEY ANANTHA CHANDRAKASAN BORIVOJE NIKOLIC

Lecture Plan: Available at Slideshare

JAIPUR NATIONAL UNIVERSITY, JAIPUR DEPT. OF ELECTRONICS AND COMMUNICATION ENGINEERING

Lecture Plan: 6EC 6.1 VLSI DESIGN

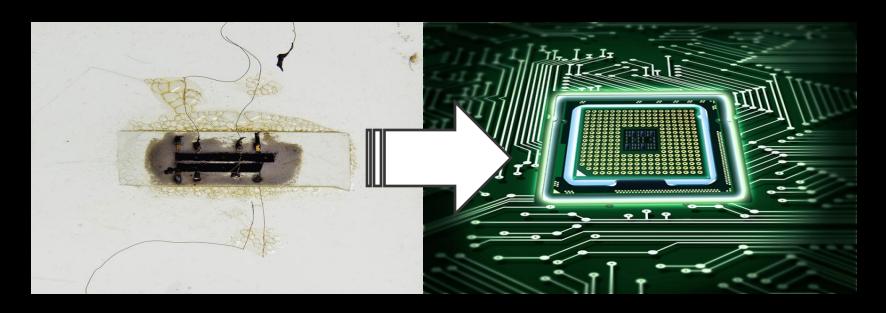
Name of Faculty: Kalyan Acharjya

Month	Unit	Topic	Lecture's No.
Jan	Unit-I	Introduction to VLSI	L1
Test 1		VLSI Industry	L2
		Transistor	L3
		MOS Transistorcontd	L4
		MOS Transistor	L5
		Large Signal MOS Models	L6
		MOS Inverter	L7
		MOS Inverter contd	L8
		MOS Inverter	L9
		Dynamic Behaviors	L10
		Conclusion of Unit I and Discussion	L11
Feb Mid Term	Unit-II	MOS Spice Model	L12
		Simulation	L13
	l	Device Characterization	L14
		Inverter Layout	L15
		CMOS Layout and Simulation	L16

Earn Your Internal Marks Calculation (Maximum 30)

- •Minimum: Test (10)+Mid-I(7.5)+Mid-II (7.5)+ Attendance(5)+K (Added to Top Scorer)
- Suppose topper(A) will score maximum 24
- Least score by B will score 10.
- If A will get 24+5=29, then B will also get 10+5=15
- •If topper will score good marks, your internal marks will be less.

Thank You for your Attention!



IC Technology Development Journey

Please feedback at: <u>kalyan.acharjya@gmail.com</u> kalyan5.blogspot.com