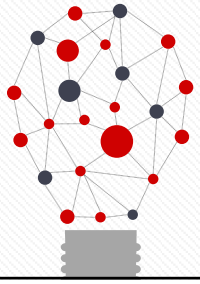
CMOS Process, transistor cross section and passive devices

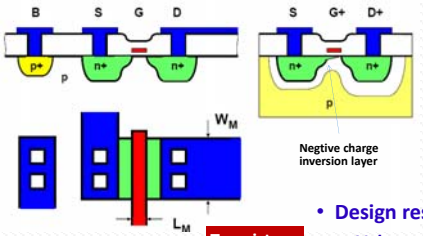
CMOS Process



Active
- NMOS, PMOS
- NPN and PNP
- Diodes

Passive
- Resistor
- Capacitor
- Inductor

CMOS process: Active transistors

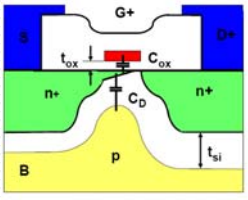


Transistor Cross-section

Transistor Layout

- Design resource you can offer
  - Voltage and Current
  - Device dimension: W/L

CMOS process: Active transistors(zoom in)



$C_D = \frac{\varepsilon_{si}}{t_{si}}$

$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$

$\frac{C_D}{C_{ox}} = n - 1$ n=1.2

t_{si}: pn junction depletion layer thickness

t_{ox}: oxide layer thickness

- Channel inversion layer is coupled to gate through Cox, coupled to bulk through C_D
- Change gate and bulk will change the device conductivity JFET operation (controlled by junction capacitance).
- Transistor: parallel of MOSFET, JFET, and bipolar devices

Active Devices: Cox and C_D values

$C_D = \frac{\varepsilon_{si}}{t_{si}}$ $t_{si} = \sqrt{\frac{2\varepsilon_{si}(\phi - V_{BD})}{qN_B}}$

$\varepsilon_{si} = 1$ pF/cm
$\varepsilon_{ox} = 0.34$ pF/cm
$\phi \approx 0.6$ V
$q = 1.6\ 10^{-19}$ C
$N_B \approx 4\ 10^{17}$ cm^{-3}

Example : L = 0.35 μm; W/L = 8

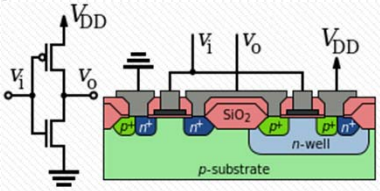
V_{BD} = -3.3 V : $t_{si} = 0.1$ μm
$C_D \approx 10^{-7}$ F/cm^2

$t_{ox} = \frac{L_{min}}{50}$ $t_{ox} = 7$ nm
$C_{ox} \approx 5\ 10^{-7}$ F/cm^2

$\frac{C_D}{C_{ox}} = n - 1 \approx 0.2$

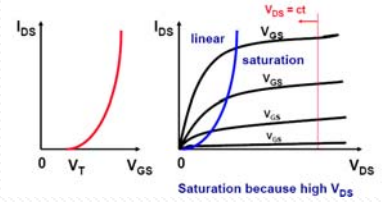
- Depletion layer thickness tsi depends on biasing voltage and doping level
- ε_{si} dielectric constant, φ junction built-in voltage
- n depends on biasing voltage, 1.2-1.5, never well known

CMOS process: Active transistors



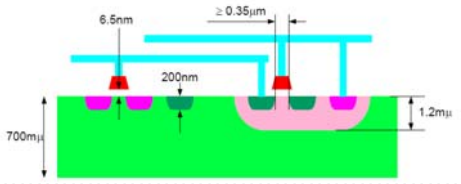
- Transistor is more than 3 terminals:
  - NMOS (npn transitor): Gate, drain, source, body
  - PMOS (pnp transitor) : Gate, drain, source, body
- Diode: PN junction
- N-well process: vertical and lateral PNP and NPN
  - Low beta, bandgap circuits

MOSFET I_{DS} Vs. V_{GS} and V_{DS}



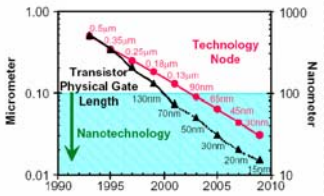
- Current starts to flow when Vgs> V_T
- V_T threshold voltage
- How much current→Vgs- V_T, overdrive voltage
  - the most important design parameter
  - Linearity, offset , gain, speed, etc.

CMOS process: dimensions



- Important to know, give you intuitive feeling of device size.
- Very good for design decision.

Moore Law Scaling



Moore law: transistor number double every 2 years

- Transistor feature size is now 10nm with FinFET process. Samsung announced that it can reach 3.25nm (beyond 5nm)
- IBM nanotube will redefine the Moore law

Resistors

- No provisions in standard CMOS
- Resistors are bad for digital circuits →
  - Minimized in standard CMOS
- Sheet resistance of available layers:

Layer	Sheet resistance
Aluminum	60 mΩ/□
Polysilicon	5 Ω/□
N+/P+ diffusion	5 Ω/□
N-well	1 kΩ/□

- Example: 100kΩ poly resistor
  → 1μm wide by 20,000μm long

Process option

- Available for many processes
- Add features to "baseline process"
- E.g.
  - Capacitor option (2 level poly, channel implant)
  - Low V_{TH} devices
  - "High voltage" devices (3.3V)
  - EEPROM
  - Silicide stop option
  - …

Resistors silicide block option

Layer	R/□ [Ω/□]	T_C [ppm/°C] @ T = 25 °C	V_C [ppm/V]	B_C [ppm/V]
N+ poly	100	-800	50	50
P+ poly	180	200	50	50
N+ diffusion	50	1500	500	-500
P+ diffusion	100	1600	500	-500
N-well	1000	-1500	20,000	30,000

- Non-silicided layers have significantly larger sheet resistance
- Resistor nonidealities:
  - Temperature coefficient: R = f(T)
  - Voltage coefficient: R = f(V)

Resistors example

Goal: R = 100 kΩ, T_C = 1/R x dR/dT = 0

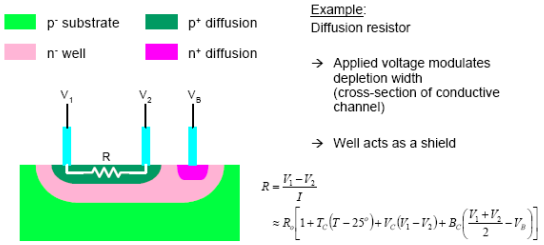
Solution: combination of N+ and P+ poly resistors in series

$$R = R_N(1+T_{CN}\Delta T)+R_P(1+T_{CP}\Delta T)$$
$$= \underbrace{R_N+R_P}_{R}+\underbrace{(R_N T_{CN}+R_P T_{CP})}_{0}\Delta T \quad \Rightarrow$$

$$R_N = R\frac{1}{1-\frac{T_{CN}}{T_{CP}}} = 20\text{k}\Omega = 200 \text{ squares}$$

$$R_P = R\frac{1}{1-\frac{T_{CP}}{T_{CN}}} = 80\text{k}\Omega = 444.4 \text{ squares}$$

Resistors voltage coefficient



Example:
Diffusion resistor

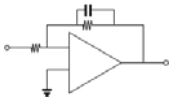
→ Applied voltage modulates depletion width (cross-section of conductive channel)

→ Well acts as a shield

$$R = \frac{V_1 - V_2}{I}$$
$$\approx R_0\left[1+T_C(T-25^\circ)+V_C(V_1-V_2)+B_C\left(\frac{V_1+V_2}{2}-V_B\right)\right]$$

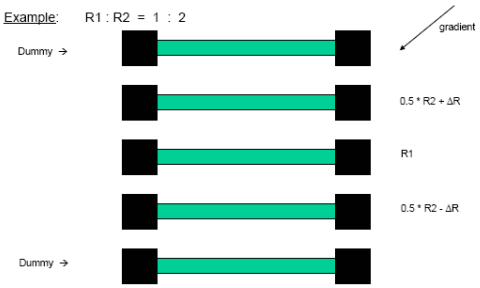
Resistors matching and layout

- Types of mismatch
  - Systematic (e.g. contacts)
  - Run-to-run variations
  - Random variations between devices
- Absolute resistor value
  - E.g. filter time constant, bias current (BG reference)
  - ~ 15 percent variations (or more)
- Resistor ratios
  - E.g. opamp feedback network
  - Insensitive to absolute resistor value
  - "unit-element" approach rejects systematic variations (large area for non-integer ratios)
  - Process gradients
  - 0.1 … 1 percent matching possible with careful layout



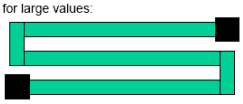
Resistors matching and layout

Example: R1 : R2 = 1 : 2



Resistors matching and layout

Serpentine layout for large values:



Better layout (mitigates offset due to thermoelectric effects):

See Hastings, "The art of analog layout," Prentice Hall, 2001.

Resistors summary

- No or limited support in standard CMOS
  - Costly: large area (compared to FETs)
  - Nonidealities:
    - Large run-to-run variations
    - Temperature coefficient
    - Voltage coefficients (nonlinear)
- Avoid them when you can
  - Especially in critical areas, e.g.
    - Amplifier feedback networks
    - Electronic filters
    - A/D converters
  - We will get back to this point

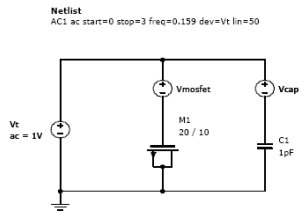
Capacitance

- **Applications**
  - Large value
    - Bypass capacitors
    - Frequency compensation
  - High accuracy, linearity
    - Feedback & sampling networks
    - Filters

Capacitance option

Type	C [aF/μm²]	V_C [ppm/V]	T_C [ppm/°C]
Gate	5300	Huge	Big
Poly-poly (option)	1000	10	25
Metal-metal	50	20	30
Metal-substrate	30		
Metal-poly	50		
Poly-substrate	120		
Junction capacitors	~ 1000	Big	Big

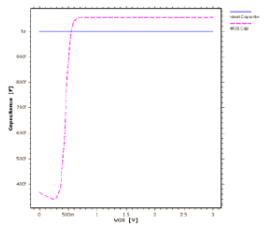
MOS Capacitance



- **High capacitance in inversion:**
  - **Linear region**
  - **Strong inversion**
- **SPICE**

$$C = \frac{I}{\omega V}$$
$$V = 1V$$
$$\omega = 1/2\pi$$
$$\rightarrow C = I$$

MOS Capacitance



- **High non-linearity, temperature coefficient**
- **Useful only for non-critical applications, e.g.**
  - **(Miller) compensation capacitor**
  - **Bypass capacitor (supply, bias)**

Poly-Poly Capacitance

- **Applications**
  - **Feedback networks**
  - **Filters(SC and continuous time)**
  - **Charge redistribution DACs & ADCs**
- **Cross-section**
- **Bottom-and top-plate parasitics**
- **Shields**

Poly-Poly Capacitance Layout

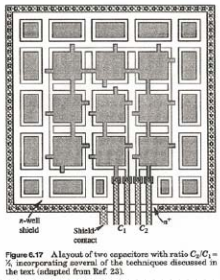


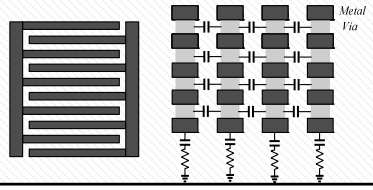
Figure 6.17 A layout of two capacitors with ratio $C_2/C_1 = 5$, incorporating several of the techniques discussed in the text (adapted from Ref. 23).

- **Unit elements**
- **Shields:**
  - **Etching**
  - **Fringing fields**
- **"Common-centroid"**
- **Wiring and interconnect parasitics**

Ref.: Y. Tsividis, "Mixed Analog-Digital VLSI Design and Technology," McGraw-Hill, 1996.

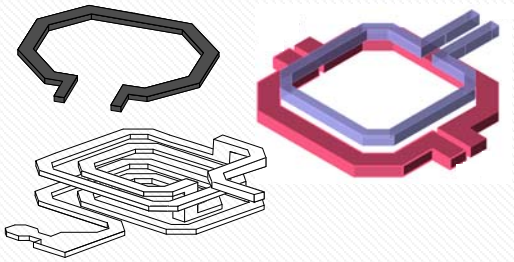
Metal Oxide Metal (MOM) Capacitance

- Metal fringing effect:
- Available in all CMOS Process (2 levels of metals)
- Parastics: Via, Bottom- and top-plate parasitics
  - Often loads amplifer
  - Increase load adds power dissipation



Inductor and transformer

- Magnetic effect



Thanks!