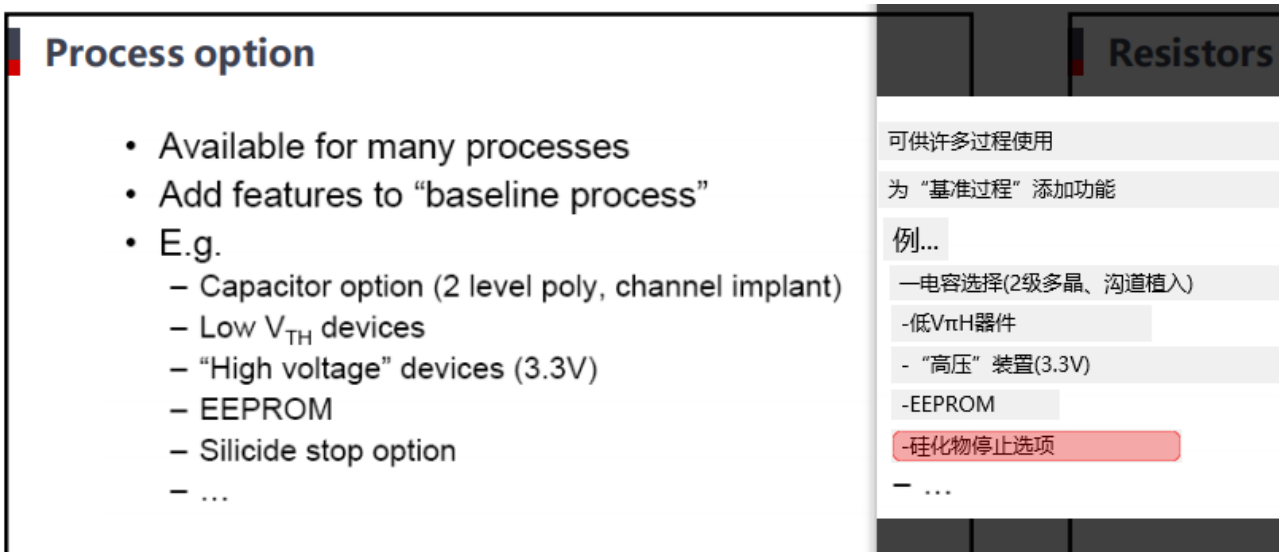
CMOS(Complementary Metal Oxide Semiconductor) 互补金属氧化物半导体
CMOS process 互补金属氧化物半导体工艺
Transistor Cross Section 晶体管截面
Passive devices 无源器件
Diode 二极管
resistor 电阻
capacitor 电容器
inductor 感应器
Layout 布局
Device dimension 设备尺寸
Zoom in 放大
Tsi（pn junction depletion layer thickness） pn 结耗尽层厚度
Tox（oxide layer thickness ） 氧化物层厚度
Inversion 倒置
Channel gate and bulk will change the device conductivity JFET operation
栅极和基底将改变器件的导电性 JFET 操作
Transister 晶体管
Parallel of MOSFET,JFET and bipolar devices MOSFET、JFET 和双极器件的并联
Depletion layer thickness tsi depends on biasing voltage and doping level
耗尽层厚度 tsi 取决于偏置电压和掺杂水平
Esi dielectric constant , Φ junction built-in voltage
Esi 介电常数，ϕ 结内置电压
N depends on biasing voltage ,1.2-1.5,never well known
N 取决于偏置电压，1.2-1.5，从未为人所知
Terminals 终端
N-well process: Vertical and lateral PNP and NPN
N 井工艺：垂直和横向 PNP 和 NPN
Low beta,bandgap circuits 低β，带隙电路
Threshold voltage 门电压
Overdrive voltage 过驱动电压
The most important design Parameter 最重要的设计参数
Linearity，offset，gain , speed 线性、偏移、增益、速度
Intuitive 直觉的
Moore law scaling 摩尔定律标度
Transistor feature size 晶体管特征尺寸
Nanotube 纳米管
Provision 提供
Sheet resistance of available layers 可用层的薄层电阻
Aluminum 铝
Polysilicon 多晶硅
N+/P+ diffusion N+/P+扩散电阻
Poly resistor 多晶硅电阻



N+ ploy	N+多晶硅
P+ ploy	P+多晶硅
N+diffusion	N+扩散电阻
P+diffusion	P+扩散电阻
N-well	N 型井

Non-silicided layers have significantly larger sheet resistance
非硅化层具有显著更大的薄层电阻

Resistor nonidealities:
电阻非理想性：
- Temperature coefficient: R= f(T)　温度系数：r=f(T)
- Voltage coefficient: R = f(V)　电压系数：r=f(V)

Resistors voltage coefficient	电阻电压系数
p- substrate	p 衬底
Applied voltage modulates depletion width	外加电压调制耗尽宽度
Cross-section of conductive channel	导电沟道横截面

Resistors matching and layout	电阻匹配与布局
Types of mismatch	不匹配类型
Systematic (e.g. contacts)	系统(例如接触)
Run-to-run variations	Run-to-run 的变化
Random variations between devices	器件间的随机变化

Resistors matching and layout

- Types of mismatch
  - Systematic (e.g. contacts)
  - Run-to-run variations
  - Random variations between devices
- Absolute resistor value
  - E.g. filter time constant, bias current (BG reference)
  - ~ 15 percent variations (or more)
- Resistor ratios
  - E.g. opamp feedback network
  - Insensitive to absolute resistor value
  - "unit-element" approach rejects systematic variations (large area for non-integer ratios)
  - Process gradients
  - 0.1 … 1 percent matching possible with careful layout

电阻匹配与布局

失配类型

— 系统(例如接触)

—Run-to-run variations

器件间的—随机变化

绝对电阻值

-例如滤波器时间常数，偏置电流(BG参考)

—~15%的变化(或更多)

电阻比

—，例如运放反馈网络

-对绝对电阻值不敏感

— "单元元素" 方法拒绝系统变化
(非整数比率的大面积)

—过程梯度

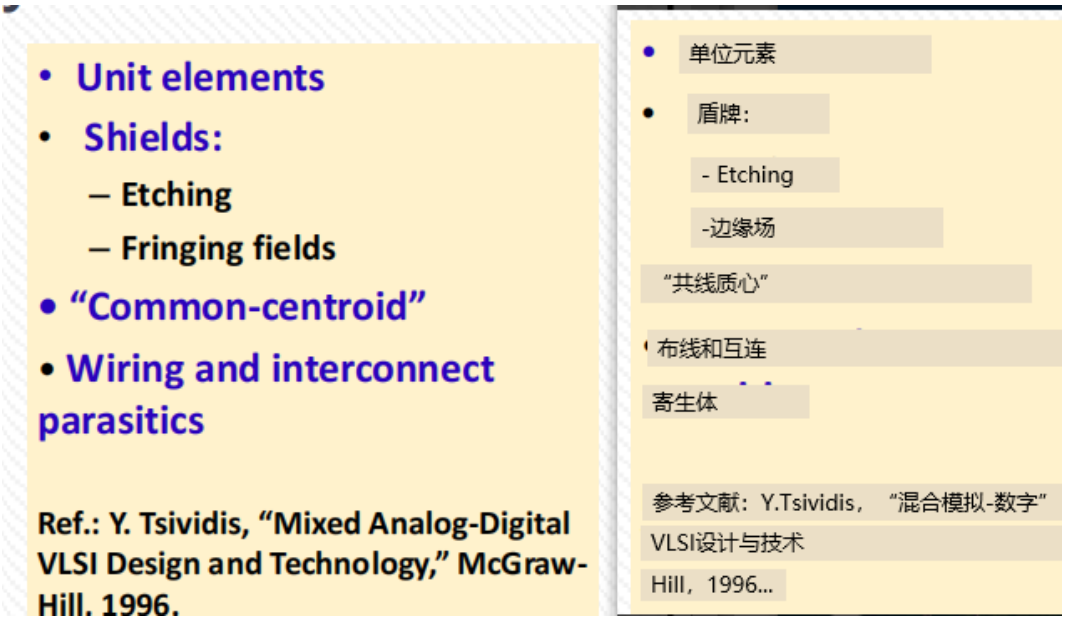
—0.1.1%的匹配可能与仔细的布局

Serpentine layout for large value 数值大的蛇形布局
Mitigates offset due to thermoelectric effects 缓解热电效应引起的偏移

Resistors summary 电阻汇总
No or limited support in standard CMOS 标准 CMOS 中无支持或支持有限
Costly ： large area
Nonidealities 非理想性
Large run-to-run variations 很大的 run-to-run 变化
Temperature coefficient 温度系数
Voltage coefficients（nonlinear） 电压系数(非线性)
Avoid them when you can 尽可能避免他们
Especially in critical networks 尤其是在关键网络中
Amplifier 放大器
Electronic filters 电子滤波器
A/D converters A/D 转换器

Capacitance 电容
Applications 应用
Bypass capacitor 旁路电容
Frequency compensation 频率补偿
Sampling 采样
Substrate 基底

MOS Capacitance MOS 电容
High capacitance in inversion 逆变电路中的高电容
Linear region 线性区域
Strong inversion 强反转



SPICE

电子电路仿真;电路模拟;集成电路专用模拟程序

Useful only for noncritical application	仅适用于非关键应用
(Miller)compensation capacitor	（米勒）补偿电容器
Bypass capacitor(supply, bias)	旁路电容器（电源、偏置）
Charge redistribution	电荷再分配
Plate	板
Parasitic	寄生

Shield	防护
Fringing	边缘
Common-centroid	共质心；共质心基本理论
Wiring	线路
Metal fringing effect	金属边缘效应
Available in all CMOS Process (2 levels of metals)	可在所有 CMOS 工艺中使用(2 级金属)
Parastics: Via, Bottom- and top-plate parasitics	寄生：通过，底部和顶板寄生
Often loads amplifer	常用来加载放大器
Increase load adds power dissipation	增加负载会增加功耗
Magnetic effect	磁效应