5-Transistor OTA Design
for LDO Buffer Application

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Figure 1: Schematic of the 5-transistor OTA implemented using SKY130A `g5v0d10v5` devices

1.1 Process and Device Selection

The OTA is designed using the **SKY130A PDK** with `g5v0d10v5` devices to allow operation under a 5 V supply.

1.2 Process and Device Selection

The OTA is designed using the **SKY130A PDK** with `g5v0d10v5` devices to allow operation under a 5 V supply.

- Process: SKY130A

- Device type: `pfet_g5v0d10v5`, `nfet_g5v0d10v5`

- Channel length: $L = 0.75~\mu$m

1.3 OTA Topology

A classical 5-transistor OTA topology is employed, consisting of:

- NMOS differential input pair

- PMOS current mirror active load

- Tail current source

This topology is selected for its simplicity, low power consumption, and sufficient gain for low-to-moderate bandwidth applications.

1.4 Design Targets

The primary design specifications are summarized in Table 1.

Parameter	Target
Load capacitance (C_L)	30 pF
Gain-Bandwidth Product (GBW)	10 MHz
Inversion region	Moderate
Supply voltage	5 V

Table 1: 5T-OTA Design Targets

2 Input Differential Pair Sizing

The differential pair is biased in **moderate inversion** to balance speed, gain, and power efficiency. The gm/Id methodology is used for systematic sizing.

- Target $g_m/I_D = 16$ V^{-1}

- Overdrive voltage: $V_{ov} = 12$ mV

- Gate-source voltage: $V_{GS} = 0.815$ V

- Tail current: $I_{tail} = 10$ μA

- Branch current: $I_D = I_{tail}/2 = 5$ μA

From gm/Id characterization:

- $g_m/g_{ds} = 152.5$

- $I_D/W = 0.589$ μA/μm

The required device width is calculated as:

$$W = \frac{I_D}{(I_D/W)} = \frac{5 \ \mu\text{A}}{0.589 \ \mu\text{A}/\mu\text{m}} \approx 8.5 \ \mu\text{m} \tag{1}$$

2.1 Transconductance and Bandwidth Estimation

The input-pair transconductance is obtained from:

$$g_m = \left(\frac{g_m}{I_D}\right) I_D = 16 \times 5 \ \mu\text{A} = 80 \ \mu\text{S} \tag{2}$$

Assuming a single-pole dominant response, the unity-gain bandwidth is estimated as:

$$\text{GBW} = \frac{g_m}{2\pi C_L} \tag{3}$$

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Substituting values:

$$\text{GBW} = \frac{80 \ \mu\text{S}}{2\pi \times 30 \ \text{pF}} \approx 0.42 \ \text{MHz} \tag{4}$$

This indicates that additional gain boosting, reduced load capacitance, or increased bias current is required to meet the 10 MHz GBW target.

2.2 Intrinsic Gain Consideration

The intrinsic gain of the input devices is estimated as:

$$A_v \approx \frac{g_m}{g_{ds}} = 152.5 \tag{5}$$

This value sets the upper bound for open-loop gain in the absence of cascoding and confirms that gain is primarily limited by the single-stage topology.

2.3 Small-Signal Parameter Extraction

From the gm/Id design point:

$$g_m = \left(\frac{g_m}{I_D}\right) I_D = 16 \times 5 \ \mu\text{A} = 80 \ \mu\text{S} \tag{6}$$

The output resistance is extracted from the intrinsic gain:

$$\frac{g_m}{g_{ds}} = g_m r_o = 152.5 \tag{7}$$

$$r_o = \frac{152.5}{80 \ \mu\text{S}} \approx 1.91 \ \text{M}\Omega \tag{8}$$

The resulting small-signal voltage gain is:

$$A_v = g_m r_o \approx 153 \ \text{V/V} \approx 43.7 \ \text{dB} \tag{9}$$

3 Tail Current Source Design

The tail transistor is designed as a high-output-resistance current source to improve common-mode rejection and power-supply rejection. A longer channel length is selected to suppress channel-length modulation and enhance current source stiffness.

- Target $g_m/I_D = 5 \ \text{V}^{-1}$

- Channel length: $L = 1.25 \ \mu\text{m}$

- Tail current: $I_{tail} = 10 \ \mu\text{A}$

- Gate-source voltage: $V_{GS} = 1.135$ V

- Overdrive voltage: $V_{ov} = 0.356$ V

The transconductance of the tail device is:

$$g_m = \left(\frac{g_m}{I_D} \right) I_{tail} = 5 \times 10 \ \mu\text{A} = 50 \ \mu\text{S} \tag{10}$$

From the extracted current density:

$$W = \frac{I_{tail}}{(I_D/W)} = \frac{10 \ \mu\text{A}}{6.323 \ \mu\text{A}/\mu\text{m}} \approx 1.58 \ \mu\text{m} \tag{11}$$

Its primary role is to maximize output resistance and minimize common-mode and supply-induced modulation of the tail current.

3.1 Theoretical CMRR Estimation

The common-mode rejection ratio (CMRR) of the 5T OTA is primarily limited by the finite output resistance of the tail current source. To first order, the CMRR can be approximated as:

$$\text{CMRR} \approx g_{m,\text{diff}} \cdot r_{o,\text{tail}} \tag{12}$$

From gm/Id extraction of the tail device:

$$r_{o,\text{tail}} = \frac{g_m/g_{ds}}{g_m} = \frac{235}{50 \ \mu\text{S}} \approx 4.7 \ \text{M}\Omega \tag{13}$$

With an input-pair transconductance of:

$$g_{m,\text{diff}} = 80 \ \mu\text{S} \tag{14}$$

The resulting CMRR is:

$$\text{CMRR} = 80 \ \mu\text{S} \times 4.7 \ \text{M}\Omega \approx 376 \ \text{V/V} \tag{15}$$

$$\text{CMRR}_{\text{dB}} \approx 51.5 \ \text{dB} \tag{16}$$

3.2 Active Load (PMOS Current Mirror)

The active load is implemented using a PMOS current mirror biased in the moderate-to-strong inversion region. A long channel length is selected to reduce channel-length modulation and improve PSRR.

For each PMOS load device:

- $g_m/I_D = 8 \ \text{V}^{-1}$

- $L = 1.25 \ \mu\text{m}$

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- $I_D = 5\ \mu\text{A}$

- $V_{GS} = 1.147$ V

- $V_{ov} = 233$ mV

The transconductance of the PMOS load device is:

$$g_{m,p} = \left(\frac{g_m}{I_D}\right) I_D = 8 \times 5\ \mu\text{A} = 40\ \mu\text{S} \tag{17}$$

From the extracted current density:

$$W_p = \frac{I_D}{(I_D/W)} = \frac{5\ \mu\text{A}}{1.03\ \mu\text{A}/\mu\text{m}} \approx 4.85\ \mu\text{m} \tag{18}$$

Using the extracted intrinsic gain:

$$r_{o,p} = \frac{g_m/g_{ds}}{g_m} = \frac{203}{40\ \mu\text{S}} \approx 5.08\ \text{M}\Omega \tag{19}$$

4 Final Dimensions and Parameters of the 5T OTA

Transistor	Role	W [μm]	L [μm]
M1, M2	NMOS differential pair	8.5	0.75
M3, M4	PMOS active load (mirror)	4.85	1.25
M5	NMOS tail current source	1.58	1.25

Table 2: Final transistor dimensions of the 5T OTA

Parameter	NMOS Diff Pair	PMOS Load	NMOS Tail
I_D [μA]	5 (per branch)	5 (per branch)	10
g_m/I_D [V^{-1}]	16	8	5
g_m [μS]	80	40	50
g_m/g_{ds} [$-$]	152.5	203	235
r_o [MΩ]	1.91	5.08	4.70
V_{GS} [V]	0.815	1.147	1.135
V_{ov} [mV]	12	233	356
I_D/W [μA/μm]	0.589	1.03	6.323
Inversion Region	Moderate	Mod–Strong	Strong

Table 3: Extracted device parameters from gm/Id lookup tables

5 Input and Output Swing Analysis

The input common-mode range (ICMR) and output swing are determined by maintaining all transistors in saturation. The supply rails are $V_{DD} = 5$ V and $V_{SS} = 0$ V.

5.1 Output Voltage Swing

Upper Output Limit The maximum output voltage is limited by the saturation requirement of the PMOS active load:

$$V_{SD,p} \geq V_{ov,p} \tag{20}$$

Thus,

$$V_{out,\text{max}} = V_{DD} - V_{ov,p} \tag{21}$$

With $V_{ov,p} = 233$ mV:

$$V_{out,\text{max}} = 5 - 0.233 = 4.77 \text{ V} \tag{22}$$

Lower Output Limit The minimum output voltage is limited by the saturation of the NMOS input transistor:

$$V_{DS,n} \geq V_{ov,n} \tag{23}$$

The source of the NMOS input pair is approximately the tail node voltage:

$$V_S \approx V_{GS,\text{tail}} = 1.135 \text{ V} \tag{24}$$

Thus,

$$V_{out,\text{min}} = V_S + V_{ov,n} \tag{25}$$

With $V_{ov,n} = 12$ mV:

$$V_{out,\text{min}} = 1.135 + 0.012 = 1.147 \text{ V} \tag{26}$$

Output Swing Summary

$$1.15 \text{ V} \leq V_{out} \leq 4.77 \text{ V} \tag{27}$$

The resulting peak-to-peak output swing is:

$$V_{out,pp} = 4.77 - 1.15 = 3.62 \text{ V} \tag{28}$$

5.2 Input Common-Mode Range (ICMR)

Minimum Input Common-Mode Voltage The lower ICMR limit is set by the saturation of the tail current source and the input NMOS devices:

$$V_{CM,\text{min}} = V_{GS,n} + V_{ov,\text{tail}} \tag{29}$$

With $V_{GS,n} = 0.815$ V and $V_{ov,\text{tail}} = 356$ mV:

$$V_{CM,\text{min}} = 0.815 + 0.356 = 1.17 \text{ V} \tag{30}$$

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Maximum Input Common-Mode Voltage   The upper ICMR limit is set by the saturation of the PMOS load devices:

$$V_{CM,\max} = V_{DD} - V_{ov,p} - V_{ov,n} \tag{31}$$

$$V_{CM,\max} = 5 - 0.233 - 0.012 = 4.76 \text{ V} \tag{32}$$

ICMR Summary

$$1.17 \text{ V} \leq V_{CM} \leq 4.76 \text{ V} \tag{33}$$

Quantity	Value
$V_{out,\min}$	1.15 V
$V_{out,\max}$	4.77 V
Output swing (pp)	3.62 V
$V_{CM,\min}$	1.17 V
$V_{CM,\max}$	4.76 V

Table 4: Input and output swing limits of the 5T OTA

5.3   Open-Loop Gain Estimation

The open-loop gain of the 5T OTA is approximated by:

$$A_{OL} \approx g_{m,n} \cdot R_{out} \tag{34}$$

where the output resistance is given by the parallel combination of the NMOS input transistor and the PMOS active load:

$$R_{out} = r_{o,n} \parallel r_{o,p} \tag{35}$$

From gm/Id extraction:

$$r_{o,n} = 1.91 \text{ M}\Omega, \quad r_{o,p} = 5.08 \text{ M}\Omega \tag{36}$$

Thus,

$$R_{out} = \frac{1.91 \times 5.08}{1.91 + 5.08} \approx 1.39 \text{ M}\Omega \tag{37}$$

With an input-pair transconductance of:

$$g_{m,n} = 80 \ \mu\text{S} \tag{38}$$

The resulting open-loop gain is:

$$A_{OL} = 80 \ \mu\text{S} \times 1.39 \text{ M}\Omega \approx 111 \text{ V/V} \tag{39}$$

Expressed in decibels:

$$A_{OL,\text{dB}} = 20 \log_{10}(111) \approx 40.9 \text{ dB} \tag{40}$$

6 Layout Strategy and Floorplanning

6.1 Layout Objectives

The layout strategy prioritizes:

- Device matching for gain, CMRR, and PSRR

- Compact floorplanning suitable for future integration in an LDO error amplifier

Fingerization and placement are chosen based on the electrical role of each device rather than uniform styling.

6.2 PMOS Active Load Layout

The PMOS current mirror load (M4, M5) is implemented with:

- Number of fingers: $n_f = 2$

- Interdigitated layout

The drains of the PMOS devices are routed symmetrically toward the output node to minimize systematic mismatch.

6.3 NMOS Differential Pair Layout

The NMOS input differential pair (M1, M2) employs:

- Number of fingers: $n_f = 4$

- Common-centroid placement

6.4 Tail Current Source and Bias Mirror

The tail current transistor (M3) uses:

- Number of fingers: $n_f = 1$

M3 is interdigitated with the bias reference transistor (M6) to form a compact and well-matched current mirror.

6.5 Floorplanning Considerations

The overall floorplan places:

- The differential pair at the geometric center

- PMOS loads symmetrically above the input devices

- Tail and bias devices below the differential pair

7 Final Layout Floorplanning
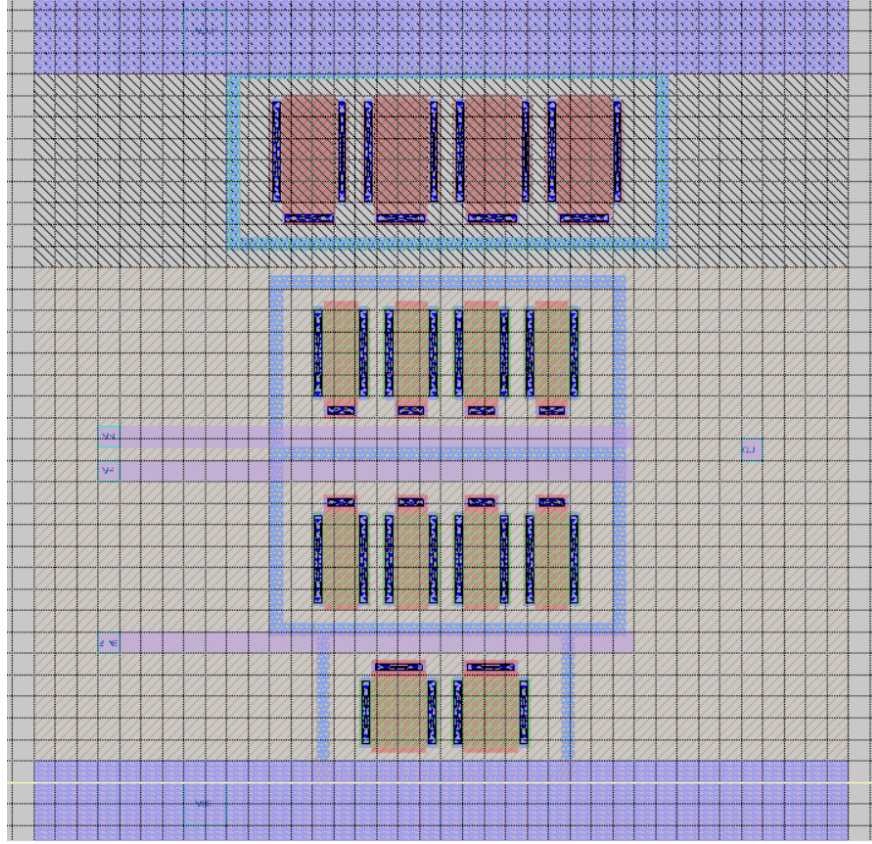
7.1 Layout Area

Figure 2: Floorplanning result of the 5-transistor OTA layout showing device placement, symmetry, and routing strategy

The finalized layout of the 5-transistor OTA occupies a compact core area of:

$$22 \ \mu\text{m} \times 19 \ \mu\text{m} \tag{41}$$

corresponding to a total silicon area of:

$$A_{\text{OTA}} = 418 \ \mu\text{m}^2 \tag{42}$$

8 SKY130: Metal Layer Current Density

Electromigration (EM) limits for on-chip metal determine the safe maximum DC current in a given metal track. A reproducible first-order method is:

$$J_\mu = J_{\text{limit}} \times 10^{-8} \quad (\text{A}/\mu\text{m}^2) \tag{43}$$

$$I_{\max} = J_\mu \cdot t \cdot W \tag{44}$$

where t is the metal thickness (µm) and W is the track width (µm).

PDK metal thickness (example, SKY130 assumptions)

- M1: $t_1 \approx 0.36~\mu\text{m}$

- M2: $t_2 \approx 0.36~\mu\text{m}$

- M3: $t_3 \approx 0.845~\mu\text{m}$

- M4: $t_4 \approx 0.845~\mu\text{m}$

- M5: $t_5 \approx 1.26~\mu\text{m}$

(Confirm exact thickness values from your local PDK; values above are from SkyWater public docs/slides. See references.)

Worked example (current per µm of width)   Using two representative EM limits:

$$J_{\text{high}} = 1 \times 10^6~\text{A/cm}^2 \quad \Rightarrow \quad J_\mu = 0.01~\text{A}/\mu\text{m}^2$$

$$J_{\text{cons}} = 5 \times 10^5~\text{A/cm}^2 \quad \Rightarrow \quad J_\mu = 0.005~\text{A}/\mu\text{m}^2$$

Layer	Thickness t (μm)	I/W @ 1×10^6 A/cm^2 (mA/μm)	I/W @ 5×10^5 A/cm^2 (mA/μm)
M1	0.36	3.6	1.8
M2	0.36	3.6	1.8
M3	0.845	8.45	4.225
M4	0.845	8.45	4.225
M5	1.26	12.6	6.3

Table 5: Example allowable DC current per µm of track width for SKY130 metal layers (two EM limits).

Item	Required for 100 mA
M1 width (min)	55.6 μm
M1 width (recommended)	70–80 μm
Current per licon	≈ 0.29 mA
Licons required (min)	≈ 345
Licons recommended	400–500

Table 6: Estimated M1 and licon requirements for 100 mA DC current in SKY130

Notes and recommended practice

- The computed numbers are first-order and assume uniform cross section, no current crowding at corners or vias, and room temperature operation.

- For production or long MTBF targets, use a lower J_{limit} or include a reliability margin ($2\times$–$5\times$), and run foundry EM checks (Calibre/ERC) on the power grid.

- Always verify via the foundry process manual or ask SkyWater/your mask house for recommended EM limits when moving beyond test chips.

Device	Role	n_f	W_f $[\mu m]$	W_{total} $[\mu m]$	L $[\mu m]$
M1, M2	NMOS diff. pair	4	2.125	8.5	0.75
M4, M5	PMOS active load	2	2.425	4.85	1.25
M3	NMOS tail source	1	1.58	1.58	1.25
M6	NMOS bias mirror	1	1.58	1.58	1.25

Table 7: Final transistor geometries and fingerization used in layout

A Simulation Results

A.1 Simulation Setup

All simulations were performed using the **SKY130A PDK** under typical process conditions (TT) at a temperature of 27°C. Unless otherwise stated, the following global conditions were applied:

- Process corner: Typical-Typical (TT)

- Temperature: 27°C

- Supply voltage: $V_{DD} = 5$ V, $V_{SS} = 0$ V

- Simulator: ngspice (via Xschem)

- Device models: `g5v0d10v5` NMOS and PMOS

Extracted simulation results will be cross-checked against hand calculations represented in the main text.

B Simulation Plots

B.1 Open-Loop Gain and Phase Margin

Figure 3 shows the simulated open-loop magnitude and phase response of the 5T OTA under typical process conditions (TT) at 27°C.
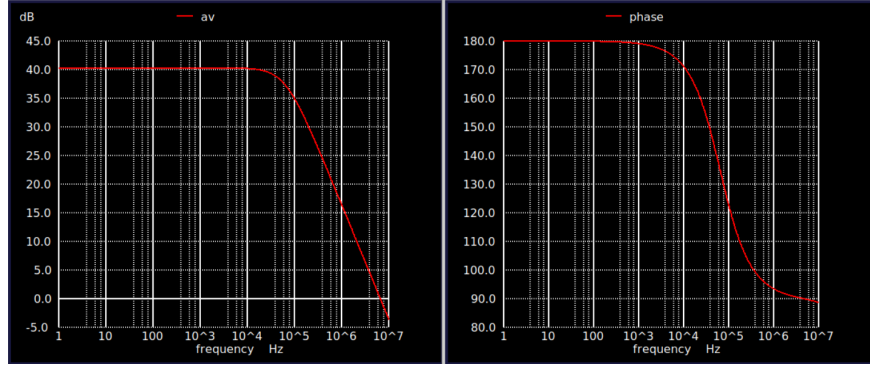

Figure 3: Simulated open-loop gain (magnitude) and phase response at TT, 27°C, $V_{DD} = 5$ V

B.2   Percentage Error Analysis

With the revised simulated open-loop gain of:

$$A_{OL,\text{sim}} = 40.3 \text{ dB} \approx 103.7 \text{ V/V} \tag{45}$$

and the hand-calculated value:

$$A_{OL,\text{calc}} = 111 \text{ V/V} \tag{46}$$

the percentage error evaluated in the linear domain is:

$$\% \text{ Error} = \frac{A_{OL,\text{sim}} - A_{OL,\text{calc}}}{A_{OL,\text{calc}}} \times 100\% \approx -6.6\% \tag{47}$$

B.3   Common-Mode Rejection Ratio (CMRR)

Figure 4 shows the simulated common-mode rejection ratio (CMRR) of the 5T OTA under typical process conditions (TT) at 27°C.
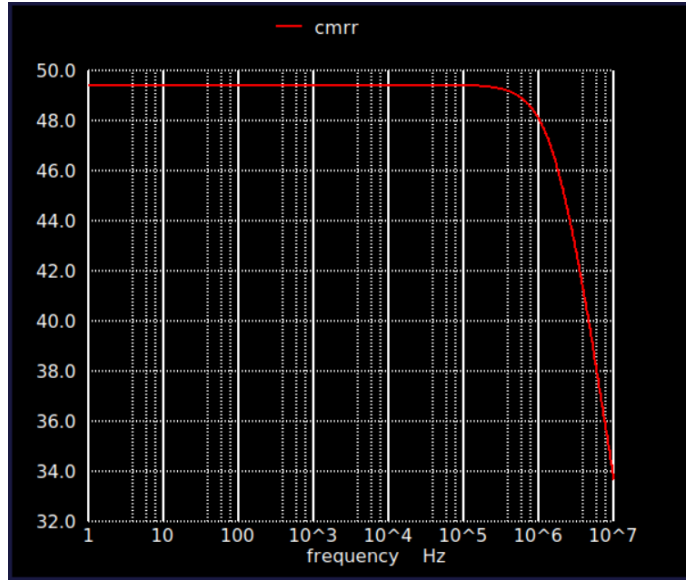

Figure 4: Simulated CMRR versus frequency at TT, 27°C, $V_{DD} = 5$ V

The low-frequency CMRR extracted from simulation is:

$$\text{CMRR}_{\text{sim}} = 49.43 \text{ dB} \tag{48}$$

B.4   CMRR Percentage Error Analysis

From theoretical analysis, the common-mode rejection ratio was estimated as:

$$\text{CMRR}_{\text{calc}} = 51.5 \text{ dB} \approx 376 \text{ V/V} \tag{49}$$

From simulation:

$$\text{CMRR}_{\text{sim}} = 49.43 \text{ dB} \approx 297 \text{ V/V} \tag{50}$$

The percentage error evaluated in the linear domain is:

$$\% \text{ Error} = \frac{\text{CMRR}_{\text{sim}} - \text{CMRR}_{\text{calc}}}{\text{CMRR}_{\text{calc}}} \times 100\% \approx -21.0\% \tag{51}$$

B.5 Power Supply Rejection Ratio (PSRR$^+$)

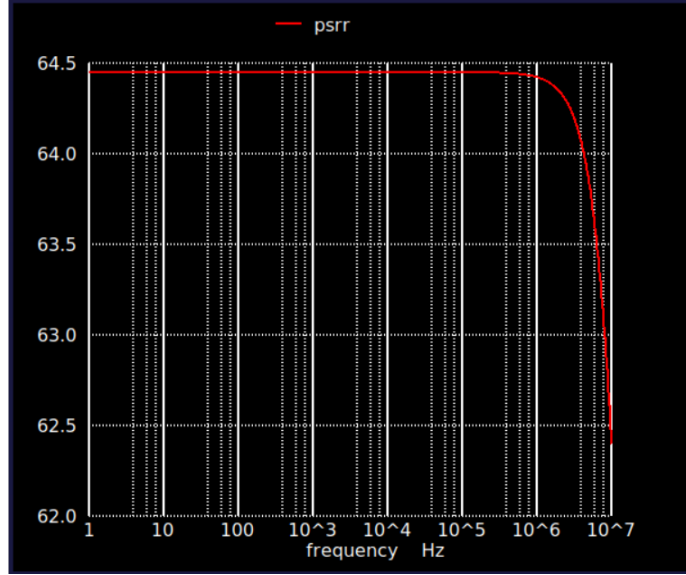Figure 5 shows the simulated PSRR$^+$ of the 5T OTA under typical process conditions (TT) at 27°C.

Figure 5: Simulated PSRR$^+$ versus frequency at TT, 27°C, $V_{DD} = 5$ V

The low-frequency PSRR$^+$ extracted from simulation is:

$$\text{PSRR}_{\text{sim}}^+ \approx 64.5 \text{ dB} \approx 1679 \text{ V/V} \tag{52}$$

B.5.1 PSRR$^+$ Analytical Estimation and Error

A first-order upper-bound estimate of PSRR$^+$ is given by:

$$\text{PSRR}_{\text{calc}}^+ \approx g_{m,\text{diff}} \cdot r_{o,\text{tail}} \cdot \frac{r_{o,p}}{r_{o,n} \parallel r_{o,p}} \tag{53}$$

Substituting extracted values:

$$\text{PSRR}_{\text{calc}}^+ \approx 1375 \text{ V/V} \approx 62.8 \text{ dB} \tag{54}$$

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The percentage error evaluated in the linear domain is:

$$\% \text{ Error} = \frac{\text{PSRR}^+_{\text{sim}} - \text{PSRR}^+_{\text{calc}}}{\text{PSRR}^+_{\text{calc}}} \times 100\% \approx +22.1\% \tag{55}$$

B.6 First-Order PSRR(+) Derivation

Power-supply rejection ratio with respect to the positive supply (PSRR^+) is defined as the ratio between supply voltage perturbation and the resulting output voltage variation:

$$\text{PSRR}^+ = \left| \frac{v_{dd}}{v_{out}} \right| \tag{56}$$

Equivalently, in small-signal form:

$$\text{PSRR}^+ = \left| \frac{1}{\partial v_{out}/\partial v_{dd}} \right| \tag{57}$$

B.6.1 Dominant Supply Noise Injection Mechanism

In a 5-transistor OTA with PMOS active load, low-frequency supply noise couples predominantly through:

- Channel-length modulation of the PMOS load devices

- Finite output resistance of the PMOS current mirror

A small-signal variation at the supply produces a drain current variation in the PMOS load:

$$\delta i_p \approx \frac{\delta v_{dd}}{r_{o,p}} \tag{58}$$

This current variation appears as a common-mode current injected into the differential pair.

B.6.2 Common-Mode to Differential Conversion

Due to the finite output resistance of the tail current source, the injected common-mode current is partially converted into a differential signal. The conversion factor is proportional to the tail impedance:

$$\delta v_{id} \propto \delta i_p \cdot r_{o,\text{tail}} \tag{59}$$

The resulting differential voltage is amplified by the transconductance of the input differential pair:

$$\delta i_{out} = g_{m,\text{diff}} \cdot \delta v_{id} \tag{60}$$

Combining the above relations:

$$\delta i_{out} \approx g_{m,\text{diff}} \cdot r_{o,\text{tail}} \cdot \frac{\delta v_{dd}}{r_{o,p}} \tag{61}$$

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B.6.3 Output Voltage Formation

The output current is converted to a voltage by the effective output resistance:

$$R_{out} = r_{o,n} \parallel r_{o,p} \tag{62}$$

Thus, the output voltage variation is:

$$\delta v_{out} = \delta i_{out} \cdot R_{out} \tag{63}$$

Substituting:

$$\delta v_{out} \approx g_{m,\text{diff}} \cdot r_{o,\text{tail}} \cdot \frac{R_{out}}{r_{o,p}} \cdot \delta v_{dd} \tag{64}$$

B.7 PSRR(+) Expression

From the definition of PSRR^+:

$$\text{PSRR}^+ = \left| \frac{\delta v_{dd}}{\delta v_{out}} \right| \tag{65}$$

Substituting the previous result:

$$\boxed{\text{PSRR}^+_{\text{calc}} \approx g_{m,\text{diff}} \cdot r_{o,\text{tail}} \cdot \frac{r_{o,p}}{r_{o,n} \parallel r_{o,p}}} \tag{66}$$

This expression represents a first-order, low-frequency upper-bound estimate of PSRR(+) for a single-stage 5T OTA with PMOS active load.

B.7.1 Numerical Evaluation

Using extracted device parameters:

$$g_{m,\text{diff}} = 80 \ \mu\text{S} \tag{67}$$
$$r_{o,\text{tail}} = 4.7 \ \text{M}\Omega \tag{68}$$
$$r_{o,p} = 5.08 \ \text{M}\Omega \tag{69}$$
$$r_{o,n} = 1.91 \ \text{M}\Omega \tag{70}$$

$$r_{o,n} \parallel r_{o,p} = \frac{1.91 \times 5.08}{1.91 + 5.08} \approx 1.39 \ \text{M}\Omega \tag{71}$$

Thus:

$$\text{PSRR}^+_{\text{calc}} \approx 80 \times 10^{-6} \times 4.7 \times 10^6 \times \frac{5.08}{1.39} \approx 1375 \ \text{V/V} \tag{72}$$

Expressed in decibels:

$$\text{PSRR}^+_{\text{calc}} \approx 20 \log_{10}(1375) \approx 62.8 \ \text{dB} \tag{73}$$