Design and Characterization of a 5 V CMOS Gate Driver in SKY130A

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December 25, 2025

Abstract

This report presents the design, transistor sizing, and transient characterization of a CMOS gate driver implemented in the SKY130A 5 V device set. Key metrics include switching speed, output voltage levels, drive capability, power losses, and identification of ambiguous operating regions.

1 Introduction

- The gate driver is a foundational PMIC block with the function to bias the power MOSFET, which usually comes with large gate capacitances.
- The gate driver will be used in half-bridge to drive both the high-side and low-side switch.
- The use of SKY130A 5V nodes here are intended to mimic the real gate drivers in standard PMIC.

2 Technology and Design Constraints

2.1 Process and Device Selection

- SKY130A 5 V NMOS/PMOS devices
- Supply voltage (V_{DRV})
- Reliability and headroom considerations

2.2 Design Targets

Table 1: Gate Driver Electrical Characteristics Summary (SKY130A, 5 V)

Category	Symbol	Specification / Notes
Input	V_{IL}	Input low-level threshold
	V_{IH}	Input high-level threshold
	$t_{r,in}$, $t_{f,in}$	Applied input rise/fall time
Output Levels	V_{OL}	Output low level at specified I_{out}
	V_{OH}	Output high level at specified I_{out}
	V_{OUT}	Output swing ($V_{OH} - V_{OL}$)
	—	Capacitive load C_L
Dynamic	t_r	Output rise time (10–90%)
	t_f	Output fall time (90–10%)
	t_{pLH}	Low-to-high propagation delay
	t_{pHL}	High-to-low propagation delay
Drive Capability	$I_{out,src}$	Peak sourcing current
	$I_{out,snk}$	Peak sinking current
	—	Slew-rate limited operation
Power Dissipation	P_{static}	Quiescent leakage power
	P_{dyn}	$C_L V_{DD}^2 f$
	P_{total}	Includes short-circuit loss
Transition Region	$V_{IL} < V_{IN} < V_{IH}$	Input threshold transition
	$V_{OL} < V_{OUT} < V_{OH}$	Output linear (overlap) region
	P_{sc}	Short-circuit loss during switching
Transistor Sizing	W/L (NMOS)	Final implemented dimensions
	W/L (PMOS)	Final implemented dimensions

3 Gate Driver Architecture

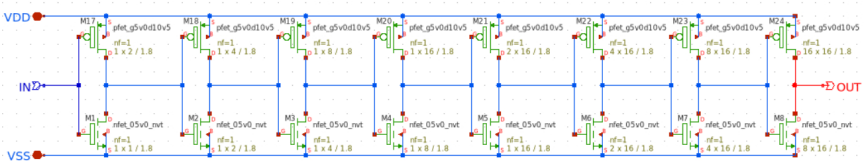

Figure 1: Schematic of the eight-stage CMOS inverter chain gate driver with tapering factor $\alpha = 2$.

- **Topology:** Eight-stage CMOS inverter chain with constant tapering factor $\alpha = 2$.
- **Technology:** Implemented using SKY130A 5 V NMOS/PMOS devices.
- **Output Swing:** Rail-to-rail operation (0–5 V), ensuring full gate enhancement and cutoff.
- **Implementation Rationale:**
  - CMOS inverter topology offers simple, robust, and layout-efficient implementation.
- **Transition Behavior:**
  - Narrow output linear (overlap) region observed during switching.
  - Transition region confined to approximately 10 mV around the switching threshold (1.81–1.82 V).
  - Reduced simultaneous PMOS/NMOS conduction, lowering short-circuit current.
- **System-Level Consideration:**
  - Reduced overlap conduction lowers risk of cross-conduction in half-bridge operation.
  - Tapered staging balances switching speed and power dissipation.

4 Transistor Sizing Methodology

4.1 Sizing Assumptions

- Sizing is set in the strong inversion region to ensure the gate driver's speed.

4.2 Final Transistor Dimensions

Device	Width (μm)	Length (μm)	Multiplier
NMOS	1	1.8	2
PMOS	2	1.8	2

Table 2: Final transistor dimensions for the gate driver.

5 Testbench Setup

5.1 Input Stimulus

- **Input voltage levels:** $V_{IL} = 0\,\text{V}$, $V_{IH} = 5\,\text{V}$.
- **Input rise/fall time:** $t_{r,in} = t_{f,in} = 1\,\text{ns}$ (unless otherwise stated).
- **Input frequency:** $f_{in} = 1\,\text{MHz}$.

5.2 Load Conditions

- **Resistive load:** $R_L = 1\,\text{k}\Omega$ to ground (used only for DC drive characterization).

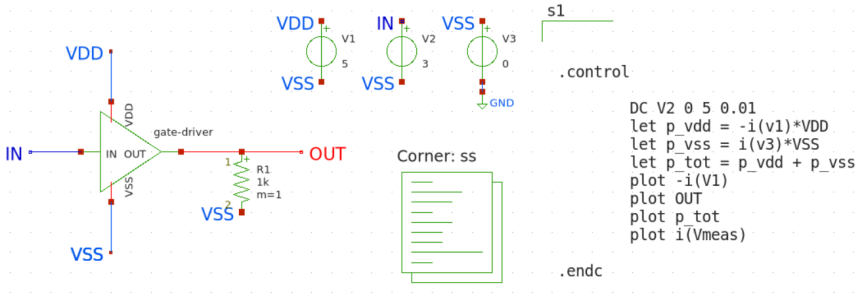

Figure 2: Transient testbench setup used for gate driver characterization.

5.3 Simulation Environment

- **Simulator:** ngspice (SKY130A PDK).
- **Process corner:** Typical–Typical (TT).
- **Operating temperature:** $27\,^{\circ}\text{C}$ (typical).

6 Static Performance

6.1 DC Characterization

- **DC input sweep:** V_{IN} swept from $0\,\text{V}$ to $5\,\text{V}$.
- **Measurement objectives:**
  - Extract DC transfer characteristic (V_{OUT} vs. V_{IN}).
  - Identify switching (overlap) region during output transition.
  - Quantify conduction losses due to resistive loading.

- **Load condition:** Resistive load $R_L = 1\,\text{k}\Omega$ connected to ground.
- **Observed loss mechanisms:**
  - Conduction loss through the output stage under DC load.
  - Overlap-related loss during the transition region of the DC sweep.

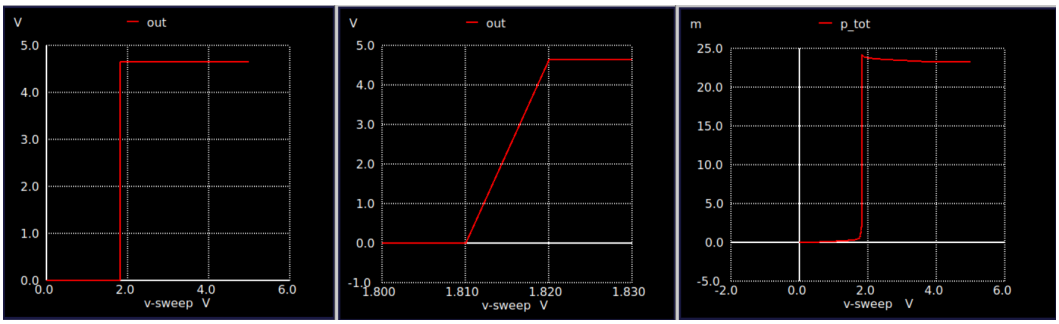

Figure 3: DC characterization of the gate driver with V_{IN} swept from 0 V to 5 V, showing the output transfer characteristic and associated conduction and transition-related losses under a 1 kΩ resistive load.

6.2 Voltage Levels

- V_{OH} **characterization:**
  - Measured under DC conditions with a 1 kΩ resistive load.
  - A voltage drop is observed due to load conduction.
  - Output high-level voltage characterized as $V_{OH} = 4.65\,\text{V}$ for $V_{IN} \geq 1.82\,\text{V}$.
- V_{OL} **characterization:**
  - Measured under DC conditions with a 1 kΩ resistive load.
  - Output low-level voltage remains at $V_{OL} = 0\,\text{V}$.
  - Characterized for $V_{IN} \leq 1.81\,\text{V}$.

6.3 Transition (Ambiguous) Region

- **Definition:**
  - The transition (ambiguous) region corresponds to the linear operating region of the CMOS inverter.
  - In this region, both NMOS and PMOS devices conduct simultaneously.

- **Voltage range:**
  - Identified between $1.81 \leq V_{IN} \leq 1.82\,\mathrm{V}$.
  - Characterized by partial output drive and increased overlap current.
- **Operating risk:**
  - Sustained operation in this region may result in undefined gate voltage levels.
  - In half-bridge applications, this condition increases the risk of simultaneous activation (cross-conduction) of the high-side and low-side switches.

6.4 DC Power Loss Analysis

- **Analytical conduction loss model:**
  - Assumes all DC power is dissipated in the external resistive load.
  - Conduction loss expressed as

$$P_{\mathrm{cond,th}} = \frac{V_{OUT}^2}{R_L}.$$

  - Using $V_{OH} = 4.65\,\mathrm{V}$ and $R_L = 1\,\mathrm{k\Omega}$, the estimated conduction loss is

$$P_{\mathrm{cond,th}} = 21.6\,\mathrm{mW}.$$

- **Simulated DC power dissipation:**
  - Steady-state simulated power for $V_{IN} \geq 4\,\mathrm{V}$ is approximately $23.2\,\mathrm{mW}$.
  - Absolute deviation from analytical model: $1.6\,\mathrm{mW}$.
  - Relative error: approximately 7.4%.
- **Sources of deviation between model and simulation:**
  - Finite on-resistance of the output PMOS device.
  - Subthreshold and leakage currents in the output stage.
  - Internal static dissipation across the multi-stage inverter chain.
- **Transition-related overlap loss:**
  - Increased power dissipation observed near $V_{IN} \approx 1.81$–$1.82\,\mathrm{V}$.
  - Caused by simultaneous conduction of NMOS and PMOS devices.
  - Results in a localized peak in DC power dissipation.

- **Model interpretation:**
  - Analytical model provides a lower-bound estimate of DC conduction loss.
  - Simulated results capture second-order device and circuit-level effects.

6.5 Output Current and Effective Output Resistance Extraction

- **DC output current:**
  - Output current under DC high-level operation is determined by the resistive load.
  - With $V_{OH} = 4.65\,\mathrm{V}$ and $R_L = 1\,\mathrm{k\Omega}$,

$$I_{out} = \frac{V_{OUT}}{R_L} = 4.65\,\mathrm{mA}.$$

- **Power discrepancy:**
  - Analytical conduction loss: $P_{\mathrm{cond,th}} = 21.6\,\mathrm{mW}$.
  - Simulated DC power dissipation: $P_{\mathrm{sim}} \approx 23.2\,\mathrm{mW}$.
  - Excess power attributed to internal conduction:

$$\Delta P = P_{\mathrm{sim}} - P_{\mathrm{cond,th}} = 1.6\,\mathrm{mW}.$$

- **Effective output resistance estimation:**
  - The excess DC power is modeled as dissipation in an effective output resistance.
  - Effective resistance extracted as

$$R_{DS,on,\mathrm{eff}} \approx \frac{\Delta P}{I_{out}^2}.$$

  - Substituting extracted values:

$$R_{DS,on,\mathrm{eff}} \approx \frac{1.6 \times 10^{-3}}{(4.65 \times 10^{-3})^2} \approx 74\,\Omega.$$

- **Interpretation:**
  - $R_{DS,on,\mathrm{eff}}$ represents the combined conduction resistance of the output PMOS device and internal driver stages.
  - The extracted value is consistent with non-ideal CMOS output behavior under DC load.

7 Dynamic Performance

7.1 Transient Load Conditions

- **Gate resistance:** $R_g = 10\,\Omega$ connected in series with the driver output.
- **Capacitive load:** $C_L = 10\,\text{pF}$ connected between the gate node and ground.
- **Load rationale:**
  - C_L models the effective gate capacitance of the driven MOSFET.
  - R_g accounts for gate resistance and interconnect parasitics.
- **DC load:** Removed during transient simulations to isolate capacitive switching behavior.

7.2 Transient Timing Extraction

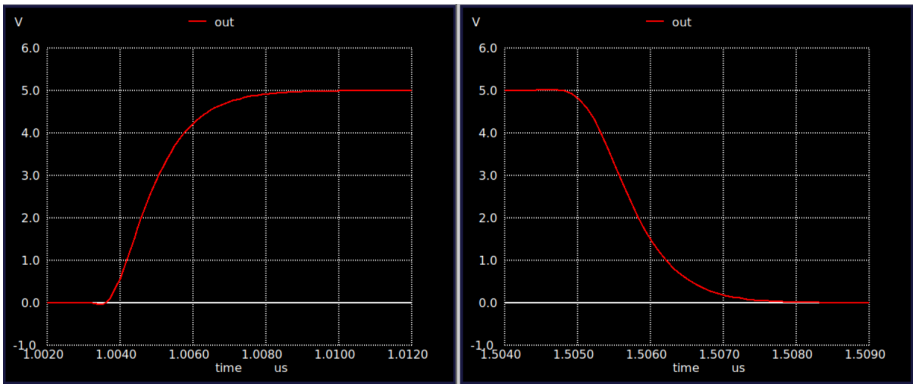

Figure 4: Transient output voltage response of the gate driver under a capacitive load ($C_L = 10\,\text{pF}$) and series gate resistance ($R_g = 10\,\Omega$). The left plot shows the rising transition used to extract t_1 and t_2 (10–90%), while the right plot shows the falling transition used to extract t_3 and t_4 (90–10%).

- **Threshold definition:**
  - 10% level: $V_{OUT} = 0.5\,\text{V}$.
  - 90% level: $V_{OUT} = 4.5\,\text{V}$.
- **Extracted transition times:**
  - $t_1 \approx 1.0042\,\mu\text{s}$ (10% crossing).
  - $t_2 \approx 1.0066\,\mu\text{s}$ (90% crossing).

- **Rise time:**

$$t_r = t_2 - t_1 \approx 2.4\,\text{ns}.$$

7.3 Transient Timing Extraction (Falling Edge)

- **Threshold definition:**
  - 90% level: $V_{OUT} = 4.5\,\text{V}$.
  - 10% level: $V_{OUT} = 0.5\,\text{V}$.
- **Extracted transition times:**
  - $t_3 \approx 1.5052\,\mu\text{s}$ (90% crossing).
  - $t_4 \approx 1.5069\,\mu\text{s}$ (10% crossing).
- **Fall time:**

$$t_f = t_4 - t_3 \approx 1.7\,\text{ns}.$$

7.4 Switching Speed

- **Rise time:**
  - Defined between 10% and 90% of the output voltage swing.
  - Extracted value: $t_r \approx 2.4\,\text{ns}$.
- **Fall time:**
  - Defined between 90% and 10% of the output voltage swing.
  - Extracted value: $t_f \approx 1.7\,\text{ns}$.
- **Observation:**
  - Falling transition is faster due to stronger NMOS pull-down.

7.5 Propagation Delay

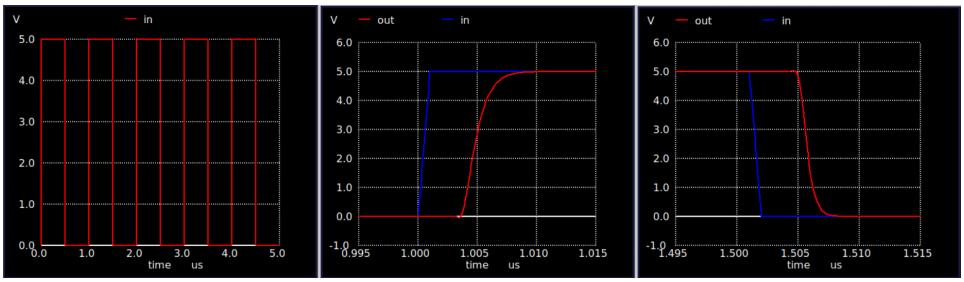

Figure 5: Transient input and output voltage waveforms used for propagation delay characterization. The left subplot shows the applied input stimulus. The middle subplot illustrates the low-to-high output transition, while the right subplot illustrates the high-to-low output transition. Propagation delays are extracted at the 50% voltage level (2.5 V) between the input and output waveforms.

- **Definition:**
  - Propagation delay defined between the 50% input and 50% output voltage levels.
  - Threshold voltage corresponds to 2.5 V.
- **Low-to-high propagation delay (t_{pLH}):**
  - $t_{IN,50} \approx 1.0045\,\mu$s.
  - $t_{OUT,50} \approx 1.0049\,\mu$s.
  - $t_{pLH} \approx 0.4$ ns.
- **High-to-low propagation delay (t_{pHL}):**
  - $t_{IN,50} \approx 1.5054\,\mu$s.
  - $t_{OUT,50} \approx 1.5057\,\mu$s.
  - $t_{pHL} \approx 0.3$ ns.
- **Observation:**
  - Falling-edge propagation delay is smaller due to stronger NMOS pull-down.

7.6 Output Current Capability

- **Measurement method:**

  - Output current extracted as the transient current through the series gate resistor.
  - This current represents the effective gate drive current delivered to the capacitive load.

- **Peak output current:**

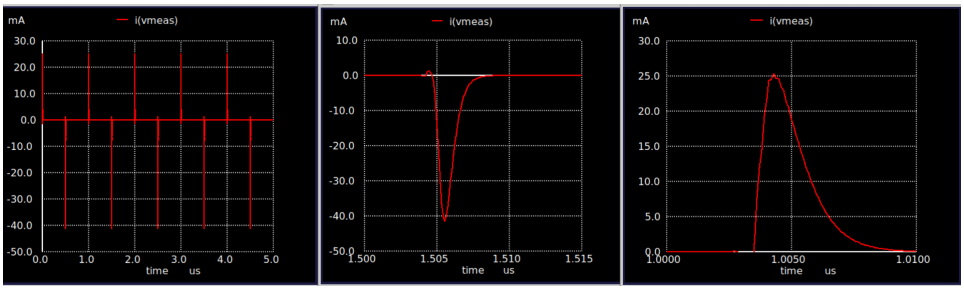

Figure 6: Transient output current of the gate driver measured as the current through the series gate resistance, $I(R_g)$. (Left) Full transient waveform over multiple switching cycles. (Middle) Zoomed view of the falling-edge transition showing peak sinking current. (Right) Zoomed view of the rising-edge transition showing peak sourcing current.

  - Peak sourcing current (charging C_L): approximately 25 mA.
  - Peak sinking current (discharging C_L): approximately 40 mA.

- **Observed behavior:**

  - Current pulses are present only during output transitions.
  - Near-zero steady-state current confirms capacitive-load-dominated operation.
  - Larger sinking current reflects stronger NMOS pull-down compared to PMOS pull-up.

8 Power Loss Analysis

8.1 Dynamic Power

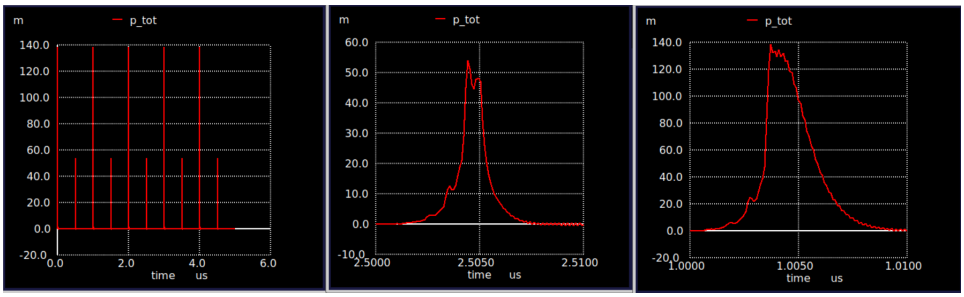

Figure 7: Instantaneous dynamic power dissipation of the gate driver during switching. The left subplot shows the periodic total power pulses over multiple input cycles, confirming event-driven dynamic power behavior. The middle subplot presents a zoomed view of the switch-off transition (input high-to-low), while the right subplot presents a zoomed view of the switch-on transition (input low-to-high). The switch-on event exhibits higher peak power and longer duration compared to the switch-off event, resulting in larger dynamic energy contribution.

- **Edge-resolved switching losses:**
  - Dynamic power consumption is evaluated separately for switch-on and switch-off events.
  - Switch-on energy is defined as

$$E_{\text{on}} = \int_{t_1}^{t_2} V_{DD} \cdot I_{DD}(t)\, dt,$$

    corresponding to the input low-to-high transition.
  - Switch-off energy is defined as

$$E_{\text{off}} = \int_{t_3}^{t_4} V_{DD} \cdot I_{DD}(t)\, dt,$$

    corresponding to the input high-to-low transition.
- **Observed asymmetry:**
  - The falling-edge transition exhibits higher peak current and shorter transition time.
  - As a result, the switch-off energy is comparable to or slightly higher than the switch-on energy.

- **Frequency dependence:**
  - The total dynamic energy per cycle is given by
$$E_{\text{cycle}} = E_{\text{on}} + E_{\text{off}}.$$
  - Average dynamic power scales linearly with switching frequency:
$$P_{\text{dyn}} = E_{\text{cycle}} \cdot f_{in}.$$
- **Non-ideal contributions:**
  - In addition to ideal capacitive charging losses, overlap current and channel resistance contribute to dynamic power during switching transitions.

8.2 Energy per Transition

- **Energy model:**
  - For a purely capacitive load, the ideal switching energy per cycle is given by
$$E_{\text{cycle}} = C_L V_{DD}^2.$$
  - The energy is approximately equally distributed between the rising and falling transitions.
- **Numerical evaluation:**
  - Load capacitance: $C_L = 10\,\text{pF}$.
  - Supply voltage: $V_{DD} = 5\,\text{V}$.
  - Substituting,
$$E_{\text{cycle}} = (10 \times 10^{-12}) \cdot (5)^2 = 250 \times 10^{-12}\,\text{J} = 250\,\text{pJ}.$$
  - Rising-edge energy:
$$E_{\text{rise}} \approx \frac{1}{2} C_L V_{DD}^2 \approx 125\,\text{pJ}.$$
  - Falling-edge energy:
$$E_{\text{fall}} \approx \frac{1}{2} C_L V_{DD}^2 \approx 125\,\text{pJ}.$$
- **Average dynamic power:**
  - Average dynamic power is computed as
$$P_{\text{dyn}} = E_{\text{cycle}} \cdot f_{in}.$$
  - For an input frequency of $f_{in} = 1\,\text{MHz}$,
$$P_{\text{dyn}} = 250 \times 10^{-12} \cdot 1 \times 10^6 = 250\,\mu\text{W}.$$

8.3 Dynamic Switching Losses

- Switching energy is evaluated by integrating the instantaneous total power over the extracted transition windows.
- Switch-on energy is defined as

$$E_{\text{on}} = \int_{t_1}^{t_2} p_{\text{tot}}(t)\, dt,$$

  while switch-off energy is defined as

$$E_{\text{off}} = \int_{t_3}^{t_4} p_{\text{tot}}(t)\, dt.$$

- Based on transient simulation, the extracted energies are:
  - $E_{\text{on}} \approx 180\,\text{pJ}$,
  - $E_{\text{off}} \approx 50\,\text{pJ}$,
  - $E_{\text{cycle}} \approx 230\,\text{pJ}$.
- The corresponding average dynamic power at $f_{in} = 1\,\text{MHz}$ is $P_{\text{dyn}} \approx 230\,\mu\text{W}$.

- **Model limitation:**
  - The analytical energy estimate neglects short-circuit and resistive losses, which were observed in transient current waveforms and contribute additional overhead beyond the ideal capacitive switching energy.

8.4 Comparison with Analytical Model

- **Analytical model (ideal capacitive switching):**
  - The ideal dynamic energy per switching cycle for a capacitive load is given by

$$E_{\text{ideal}} = C_L V_{DD}^2.$$

  - With $C_L = 10\,\text{pF}$ and $V_{DD} = 5\,\text{V}$,

$$E_{\text{ideal}} = 10\,\text{pF} \cdot 5^2 = 250\,\text{pJ}.$$

Table 3: Comparison between analytical and simulated dynamic energy and power

Quantity	**Analytical**	**Simulated**
Switch-on energy E_{on}	125 pJ	∼180 pJ
Switch-off energy E_{off}	125 pJ	∼50 pJ
Total energy per cycle E_{cycle}	250 pJ	∼230 pJ
Average dynamic power P_{dyn} @ 1 MHz	250 μW	∼230 μW

8.5 Short-Circuit and Transition Losses

- **Overlap current during switching:**
  - During input transitions, both NMOS and PMOS devices conduct simultaneously, creating a direct current path between V_{DD} and ground.
  - This overlap conduction results in short-circuit current pulses, observed as sharp peaks in the instantaneous power waveform during switching events.
  - Short-circuit loss contributes additional energy beyond the ideal capacitive charging and discharging of the load.
- **Relation to transient power dissipation:**
  - The switch-on transition exhibits higher short-circuit loss due to longer rise time and extended device overlap.
  - This behavior is consistent with the higher extracted switch-on energy compared to the switch-off energy.
- **Impact of the ambiguous region:**
  - The ambiguous input region, identified between 1.81 V and 1.82 V, corresponds to the linear operating region of the CMOS inverter.
  - Within this region, both pull-up and pull-down devices are partially ON, increasing the likelihood of overlap current.
  - Although the ambiguous region is narrow, repeated traversal during switching contributes to cumulative short-circuit energy loss.
- **Design implication:**
  - The narrow ambiguous region limits the duration of overlap conduction and reduces short-circuit losses.
  - This represents a favorable trade-off between fast switching and controlled transient power dissipation in the gate driver design.

9 Discussion

- The tapered CMOS inverter chain provides fast switching with limited overlap conduction, as evidenced by the narrow transition region and short propagation delay.
- The use of a series gate resistance and capacitive load introduces RC-limited behavior, trading peak current for controlled switching and reduced stress.

- Asymmetry between rising and falling transitions is observed, primarily due to stronger NMOS pull-down characteristics.
- Extracted effective output resistance and transient current levels are consistent with the selected device sizing and technology constraints.

10 Limitations

- All results are obtained under typical–typical (TT) process corner and nominal temperature conditions.
- Parasitic effects are modeled using first-order lumped elements rather than post-layout extraction.
- Load conditions represent a simplified gate-capacitance model and do not include package or bondwire parasitics.

11 Conclusion

- A CMOS gate driver based on an eight-stage tapered inverter chain was designed and characterized using the SKY130A 5 V technology.
- The driver achieves fast switching, low propagation delay, and sufficient output current capability for capacitive gate loads.
- The presented results demonstrate a balanced trade-off between speed, power dissipation, and robustness under practical loading conditions.

A Gate Driver Electrical Specifications

Table 4: Gate Driver Electrical Characteristics Summary (SKY130A, 5 V)

Category	**Symbol**	**Specification / Notes**
Input	V_{IL}	0 V
	V_{IH}	5 V
	$t_{r,in}$, $t_{f,in}$	1 ns (applied stimulus)
Output Levels	V_{OL}	0 V
	V_{OH}	5 V (no DC load, capacitive switching)
	V_{OUT}	5 V swing ($V_{OH} - V_{OL}$)
	C_L	10 pF
Dynamic	t_r	$\approx$ 2.4 ns (10–90%)
	t_f	$\approx$ 1.7 ns (90–10%)
	t_{pLH}	$\approx$ 0.4 ns (50%–50%)
	t_{pHL}	$\approx$ 0.3 ns (50%–50%)
Drive Capability	$I_{out,src}$	$\approx$ 25 mA (peak, rising edge)
	$I_{out,snk}$	$\approx$ 40 mA (peak, falling edge)
	—	RC-limited switching behavior
Power Dissipation	P_{static}	$\approx$ 7 μW @ 1 MHz
	P_{dyn}	$\approx$ 230 μW @ 1 MHz
	E_{cycle}	$\approx$ 230 pJ
	P_{total}	Dominated by dynamic switching loss
Transition Region	$V_{IL} < V_{IN} < V_{IH}$	1.81–1.82 V (ambiguous region)
	$V_{OL} < V_{OUT} < V_{OH}$	Output overlap region
	P_{sc}	Included in transient power spikes
Transistor Sizing	W/L (NMOS)	As implemented (see schematic)
	W/L (PMOS)	As implemented (see schematic)