Course Number: EC-ENGR 5590VL-0001 Special Topics in ECE

Tutorial: 2

(Lab report + Homework)

**TITLE**

Layout in Cadence Virtuoso for NAND and NOR Gates

Date of Performing Experiment: 10th September 2019

Due Date: 17th September 2019

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# Objective:

To draw layout in Cadence Virtuoso for basic gates (NAND and NOR gate) and simulate it using the schematic and symbol from previous tutorial.

# Theory:

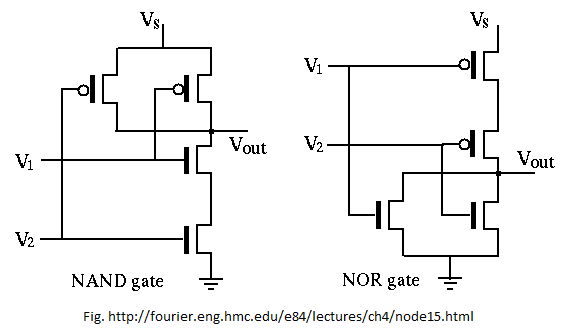
The NAND and NOR gates are implemented with 2 NMOS and 2 PMOS in CMOS logic. The CMOS (Complementary MOSFET) logic is effective as PMOS act as strong pull-up device and NMOS acts as strong pull-down device. The fabrication of NMOS and PMOS in a CMOS technology is done by 3 methods:

1. N-well process
2. P-well process
3. Twin tub process

The N-well process is most commonly used in fabrication process due to its simplicity. We will be using N-well process in the Virtuoso Cadence tool. In N-well process, P-substrate is used. After oxidation and masking, n-well is formed using diffusion process and the SiO2 layer is removed. Then, polysilicon is deposited for gates formation, remaining polysilicon part is stripped off and oxidation layer is formed. By masking and N-diffusion, n-type (n+) dopants are diffused to form the source and drain terminals. Further steps are done for formation of insulation layer and metallization of the gates. Hence, both PMOS and NMOS are form on same wafer.

In Cadence tool: “Poly” is used for connecting the polysilicon (gate), “Metal1” is used as wires for connecting the terminals and also for the VDD and GND. “Via” is used to make contact with different layers (like polysilicon and metal). N-well is tied to VDD. Make connections as per circuit diagram.

Circuit Diagram using CMOS:



# Procedure for Creating Symbol of NOR from Schematic:

1. Open Virtuoso as per earlier tutorial. Open MobaXterm, new TUX cluster window. Type password.

ls

CadenceSetup(Enter)

CDKSetup(Enter)

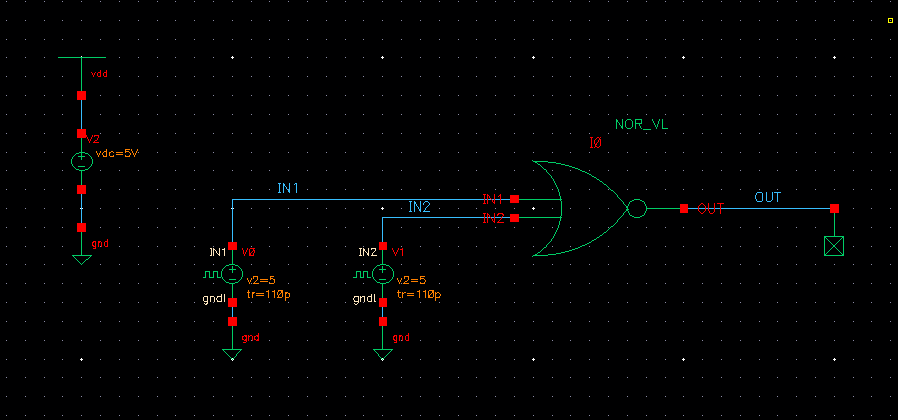
Cd cadence6

Virtuoso &

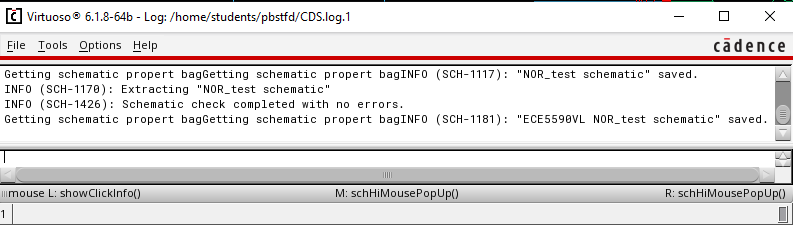
1. Select the created library in 1st tutorial.
2. Go in File🡪 Open🡪 NOR\_VL (open the NOR schematic of earlier tutorial)
3. Save it by “NOR\_Schematic\_Test” name.
4. Keep the schematic file named “NOR\_VL” for creating a symbol from previous tutorial.
5. Delete the VDD, GND, the two Vpulse signals and 5V voltage source. Keep one VDD and GND connection as per below image.
6. Click on Create 🡪 Pin. In “Create Pin” window type names of Pins: IN1 IN2. Select direction as “input”. Click “hide”. Place the pins at the respective positions in the schematic. Repeat the process for output pin: OUT, by selecting direction as “output”. The schematic is as follows after adding pins.
7. Click on Create 🡪 Cellview🡪 from Cellview. In Cell name, type “NOR\_VL”. Click OK. In “Symbol Generation Option”, “Left Pins” has input names and in “Right Pins” have output names. Click OK.
8. Delete the green and red lines in the symbol to create a customized symbol. A standard NOR gate symbol can be created.
9. Using create 🡪 Shape🡪 Line, arc and Circle, create a standard symbol. Connect the wires with the pins.
10. Click Create🡪Selection Box 🡪 Automatic 🡪Hide. Selection box gets added automatically. Adjust by dragging if alignment is wrong.
11. To simulate, go in File🡪 New File window, type under “Cell” NOR\_test. Click OK.
12. Create 🡪 Instance🡪 Browse. Click on “Hide”. On “Component Browser” window, select the created library (EC5590VL) and Select the “NOR\_VL” symbol. Place the symbol on the schematic as instance.
13. Go in Create 🡪 Instance. Add all the power sources that were deleted earlier. VDD, GND, Vsource and two Vpulse signals from the “basic” library.
14. Add “noConn” at the output. Create🡪 Wire Name, as done in previous schematic. Check and Save the schematic.
15. Launch🡪 ADE L and repeat the simulation steps as in assignment 1 by adding model files.

# Tables/Graphs for NOR Symbol:

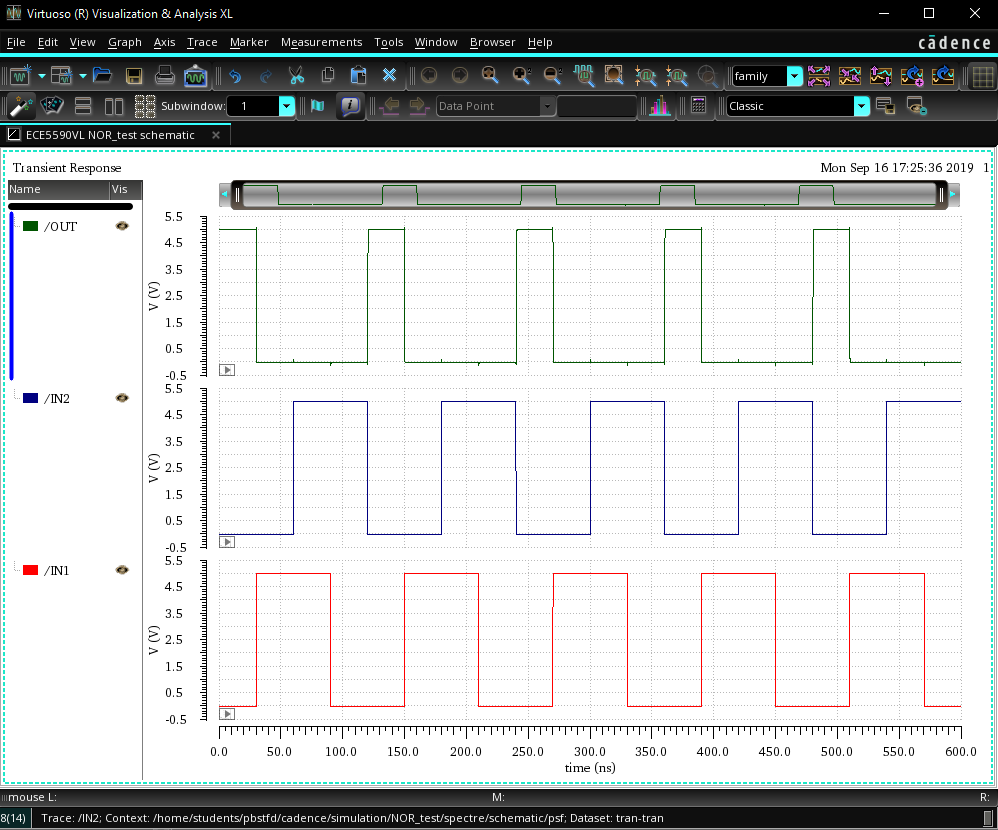
1. Schematic of NOR using symbol



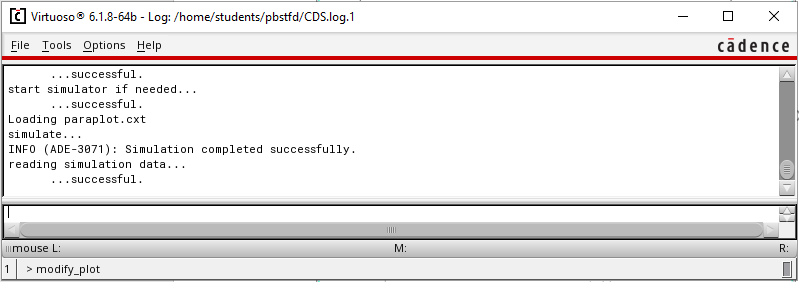
1. Log of Virtuoso check and save



1. Simulation using NOR symbol

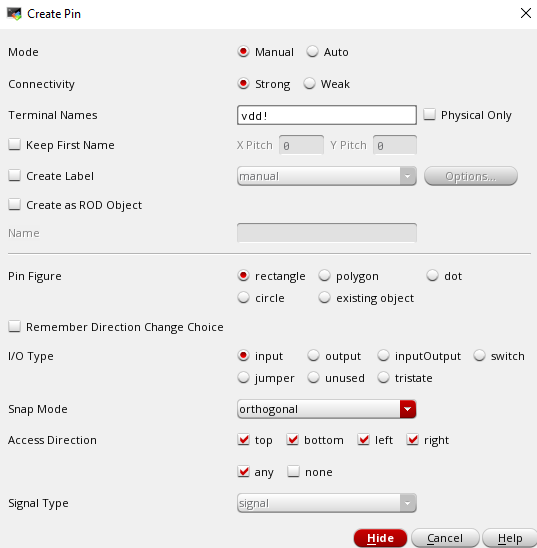


1. Simulation log

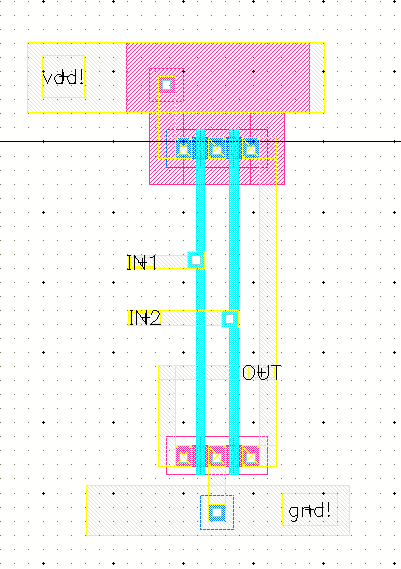


# Procedure for Creating NOR Layout:

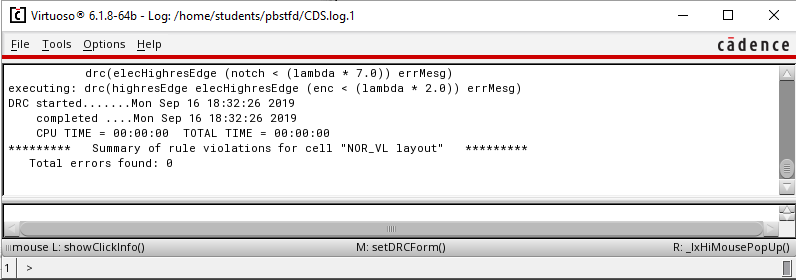
1. In CIW window, in File🡪 New🡪 cellview🡪 give cell name same as that was given for the schematic and symbol, “NOR\_VL” and select the layout option in application.
2. Go in Create🡪 Instance and in NSCU\_TechLib\_ami06, add the PMOS and NMOS transistors with the properties same as the instances in schematic.
3. Press Shift + f for viewing the layout of the instances.
4. Use “metal1” to connect the wires and “poly” to connect the polysilicon gates. These options are available in “Layer” tab at the left side of screen.
5. Use “r” key draw rectangle, “m” key to move an object and “s” key to stretch a layer.
6. Add metal rectangles for VDD and GND. Extend the n-well to connect it to VDD.
7. To connect different layers, go in Create🡪 Via. Use “M1\_Poly” to connect Poly with Metal, “M1\_N” to connect N-well to VDD and “M1\_P” to connect GND.
8. Now, select metal1 and go in Create🡪 Pin and as per below image, create pin for vdd! gnd! and IN1, IN2, OUT. Select I/O type as “output” for the OUT pin. Place the pins on the layout at appropriate locations.



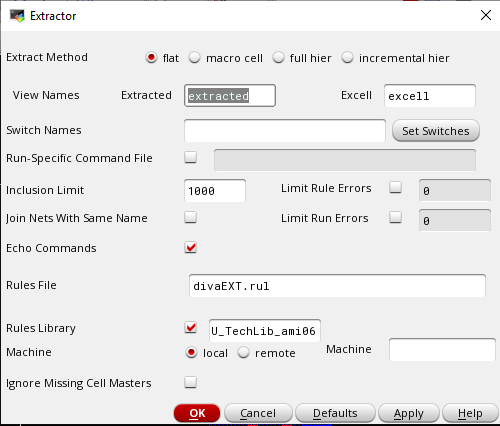
1. The layout should look as below (colors inverted).



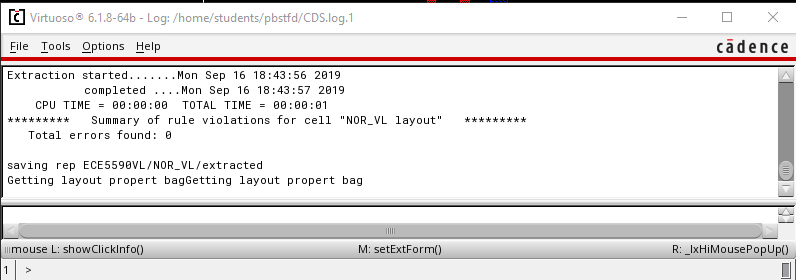
1. Go in Verify🡪 DRC to check if any errors. Errors will be shown by white lines. Correct them and again verify using DRC check. Following window must show 0 errors.



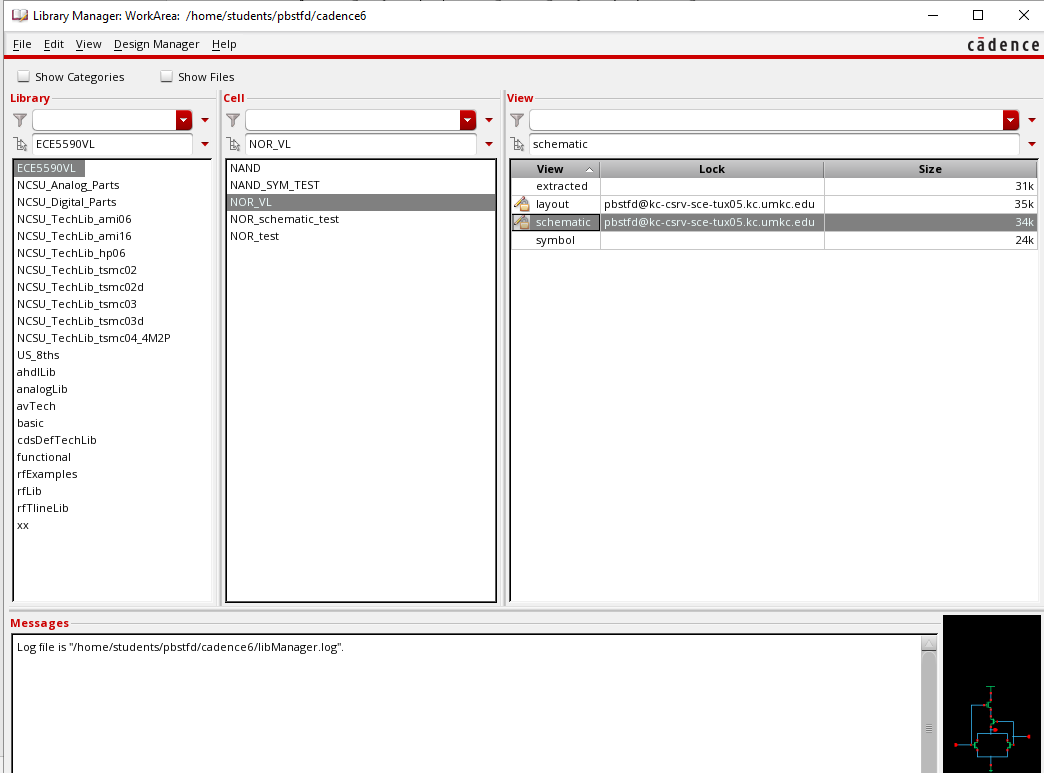
1. Then click on the Verify🡪 Extract and check if field are as per below image. Click Set Switches and select the “Extract\_parasitic\_caps” option. Click on “OK”

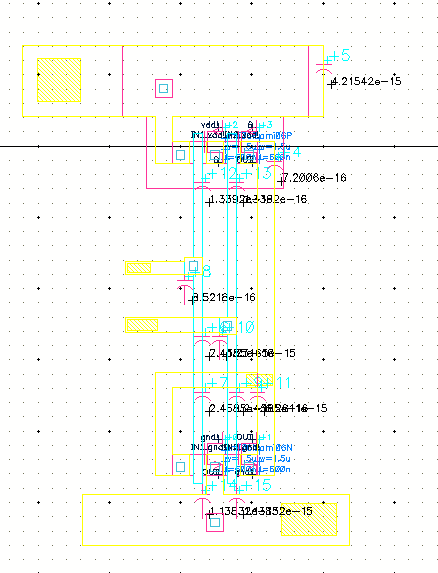


1. After extraction, errors shown must be 0. NOR\_VL extracted view must be saved.

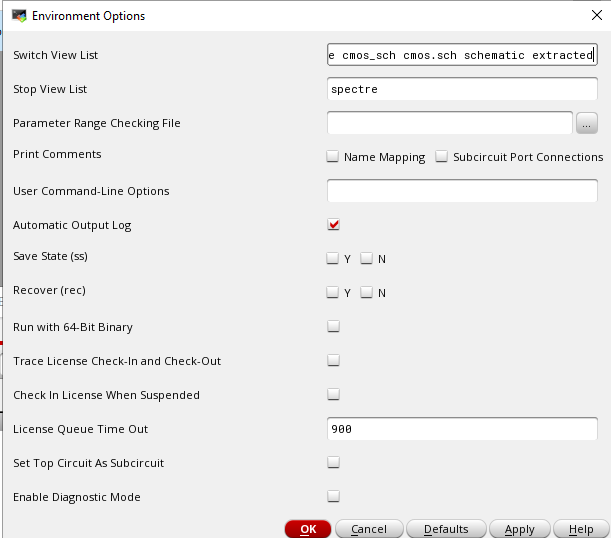


1. Save design and close all other window except CIW and library manager. In library manager window, click on “NOR\_VL” and you must see all 3 files: schematic, layout and symbol.
2. Open the extracted file to view the capacitances.

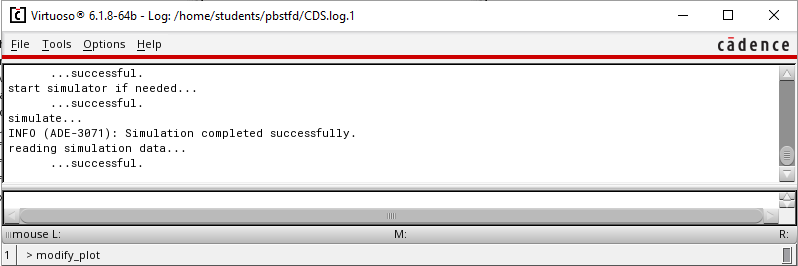




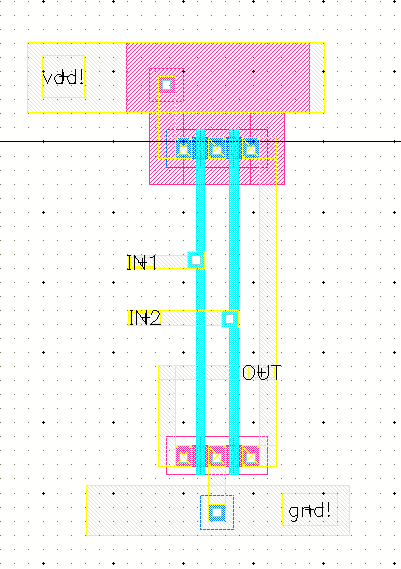
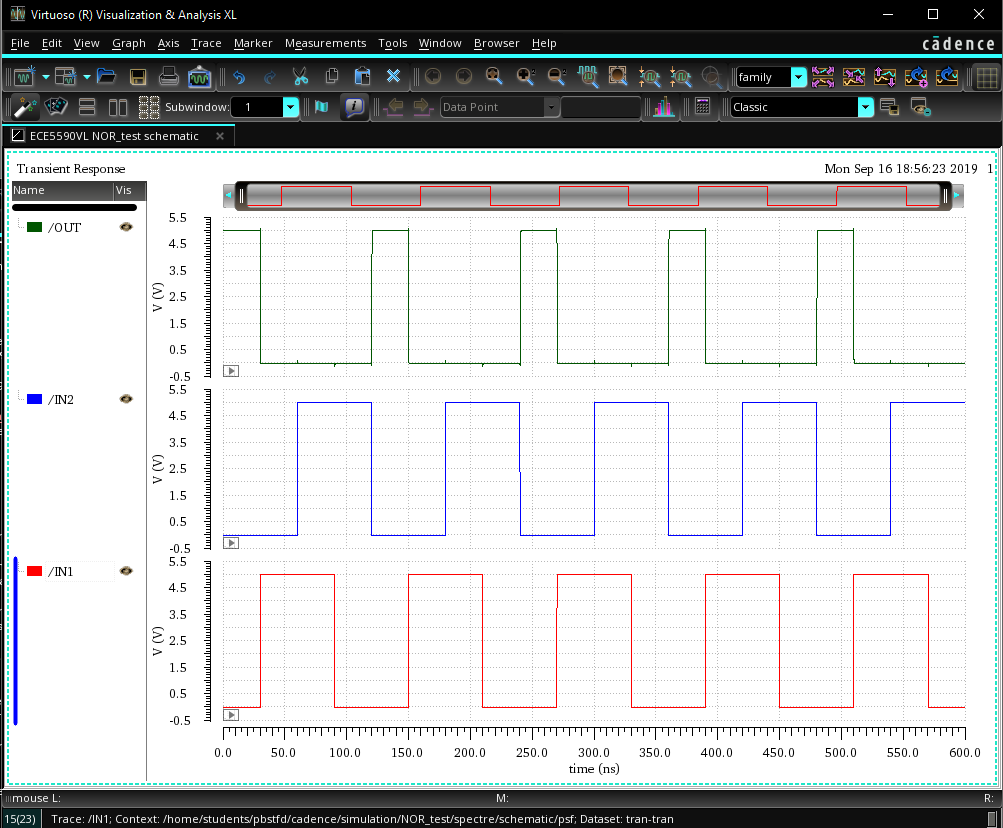
1. Open the NOR\_test file to simulate the symbol along with layout.
2. Go in Launch🡪 ADE l and follow the procedure done for schematic simulation with one additional step.
3. Go in Setup🡪Environment and change “veriloga” to “extracted” as per below image.



1. Run Simulation and capture waveform. CIW window must show successful simulation.



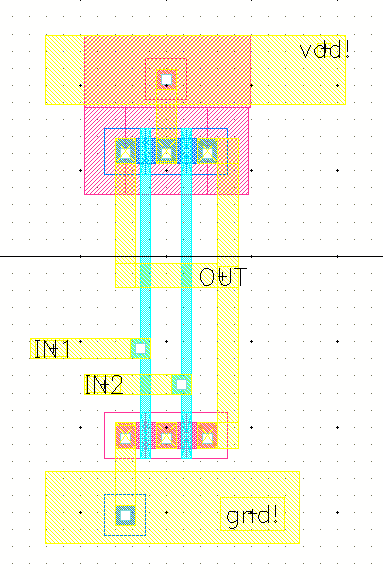
# Tables/Graphs for NOR Layout:

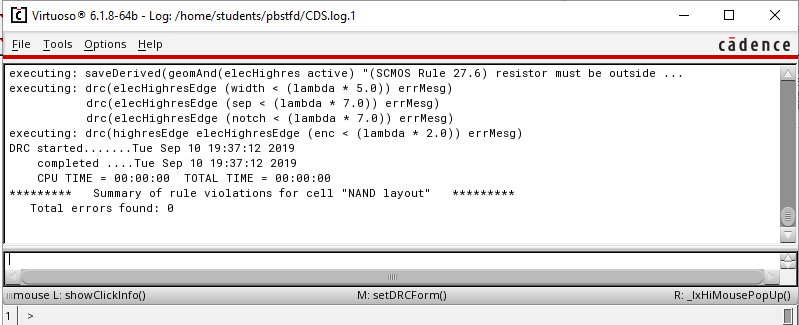
# Tables/Graphs for NAND Layout:

This section was done during lab session and has procedure similar to NOR gate.

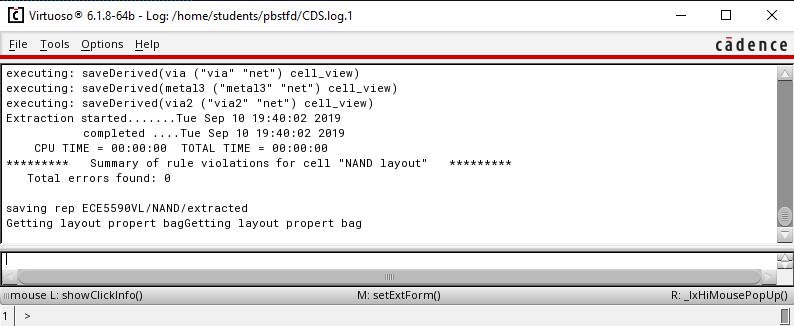
1. Layout of NAND gate



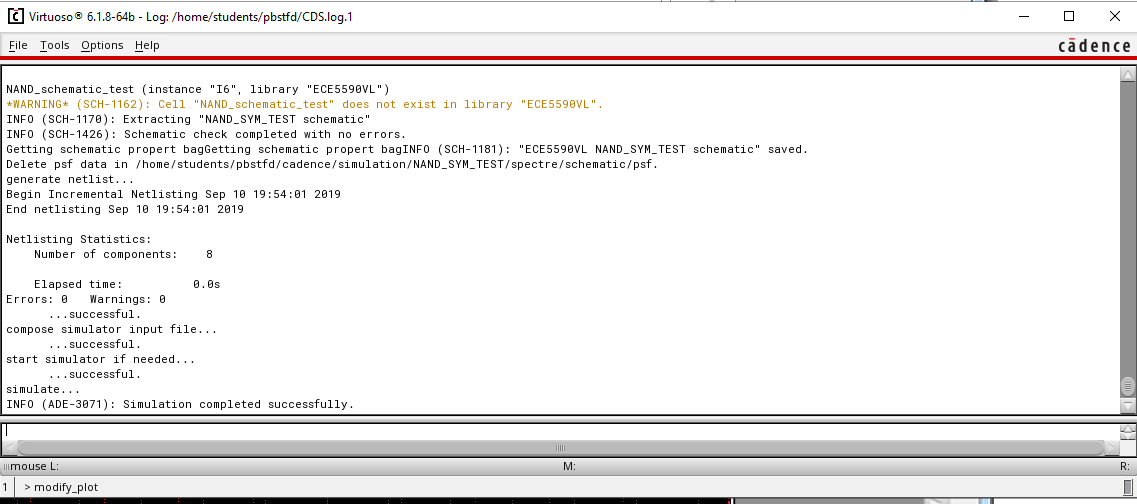
1. DRC check of NAND Layout

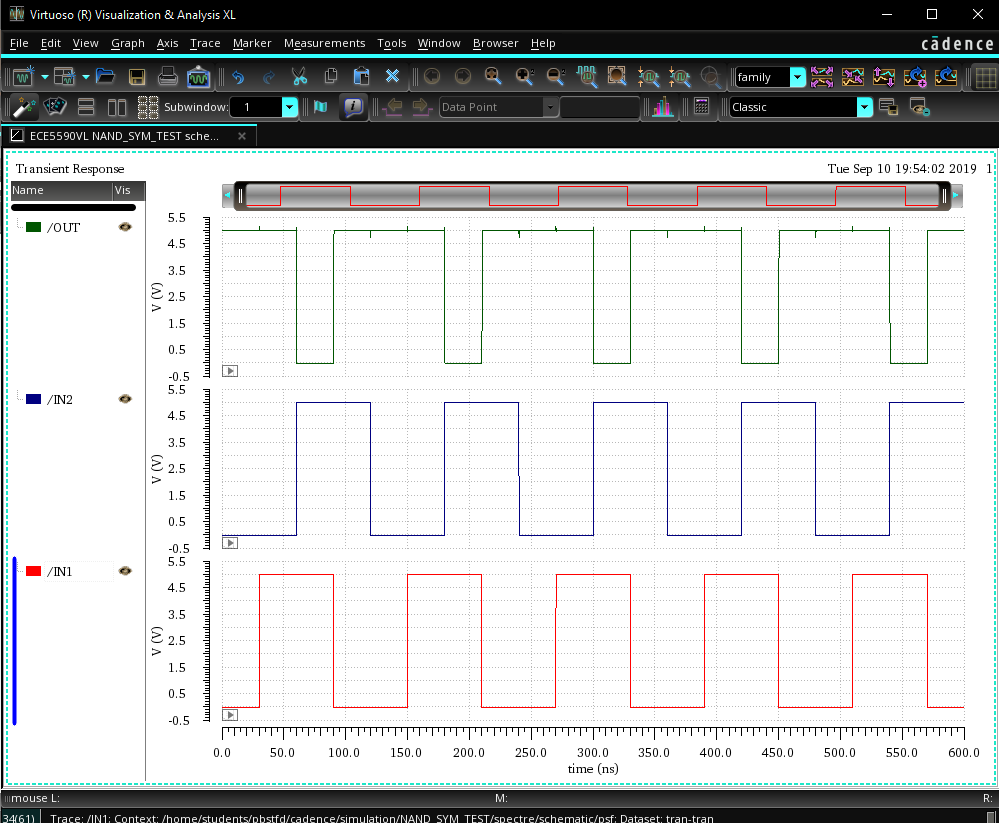


1. CIW window after Verify🡪 extracted



1. Simulation of Symbol using Layout





# Discussion of Result:

The waveforms of simulations of NAND gate and NOR Gate match with the truth table for all the combinations. Also, the layout works perfectly after changing simulation environment to “extracted”. Key point is to keep the schematic, symbol and layout names same in order to simulate the schematic of symbol. DRC check is useful to verify the layout.

# Conclusion:

In this lab session, we learnt to create the layout of NAND gate and implemented the layout of NOR gate using Cadence Virtuoso. We understood the fabrication of n-well process for implementation of CMOS logic. We also understood the steps for extracting the capacitors, simulating