Course Number: EC-ENGR 5590VL-0001 Special Topics in ECE

LEC 47031

Tutorial: 4

Homework

**TITLE**

Schematic, Symbol, layout design and LVS check for **XNOR** gate using Cadence Virtuoso

Date of Performing Experiment: 24th September 2019

Due Date: 1st October 2019

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# Objective:

To draw schematic, symbol and layout for the XNOR gate using Cadence Virtuoso. Performing LVS check on the schematic and extracted layout to verify if they match.

# Theory:

The XNOR gate give high output only when all inputs are same i.e. (0, 0) or (1, 1). If there are odd number of high inputs then the output is low. It is called exclusive NOR gate.

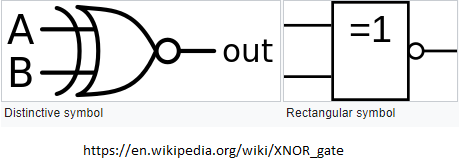
This practical introduces to the implementation of XOR gate using CMOS logic: NMOS and PMOS transistors. The implementation is done in Cadence virtuoso software.

XOR Gate:

Truth Table:

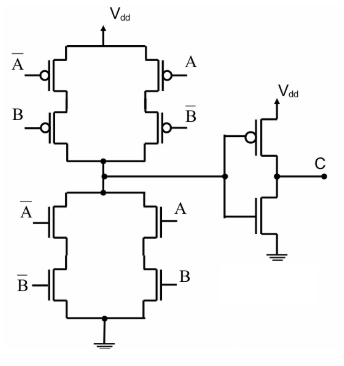
|  |  |  |
| --- | --- | --- |
| Input 1 | Input 2 | Output |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Symbol: XOR gate

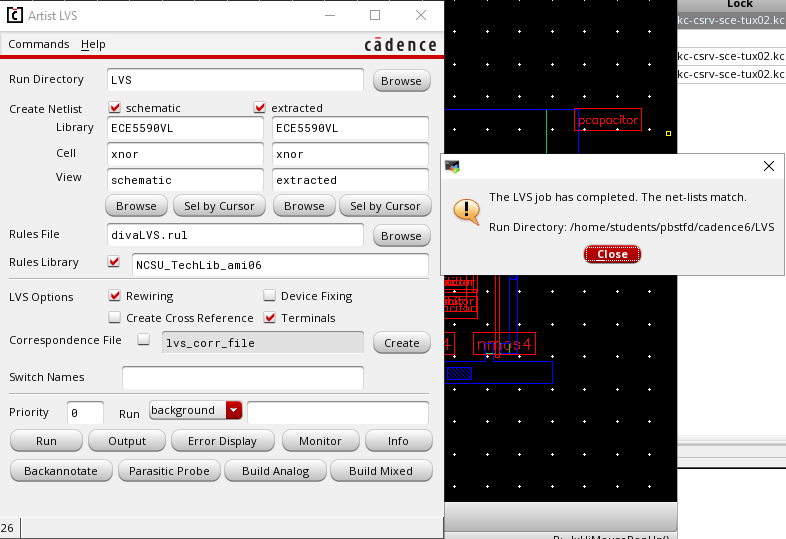


Equation:

Circuit Diagram using CMOS:



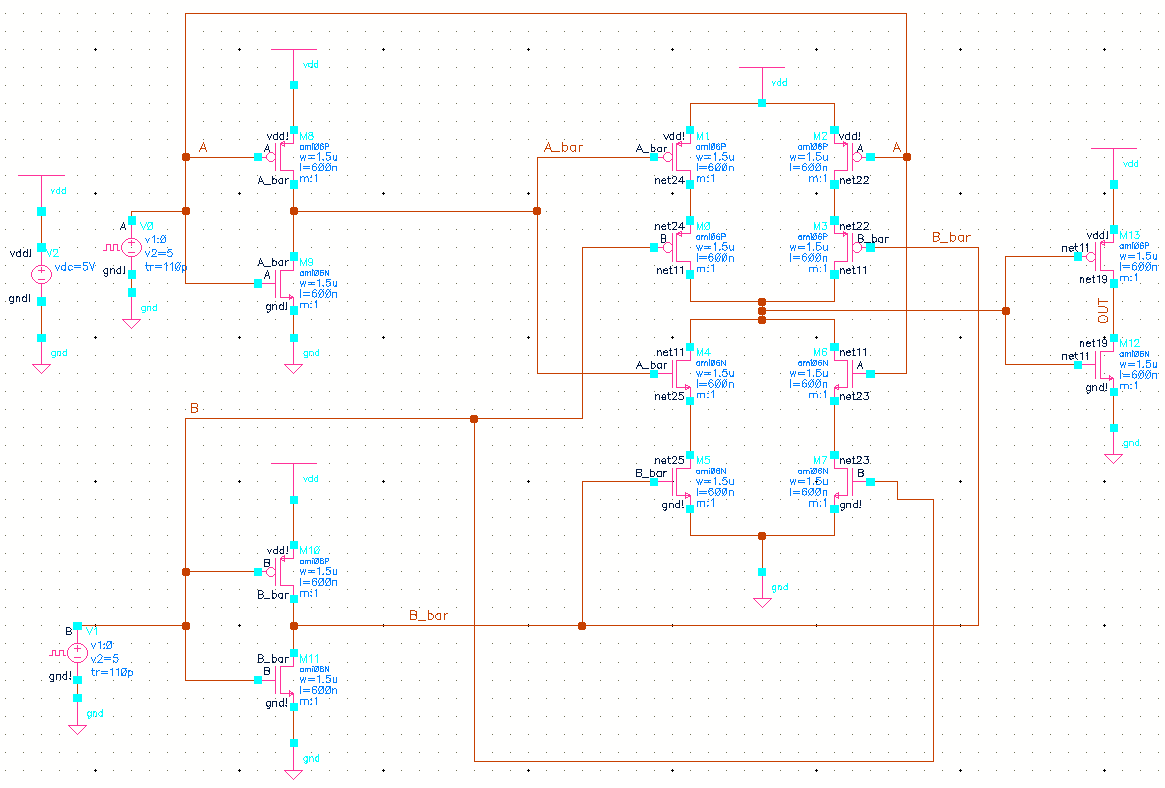
# Procedure:

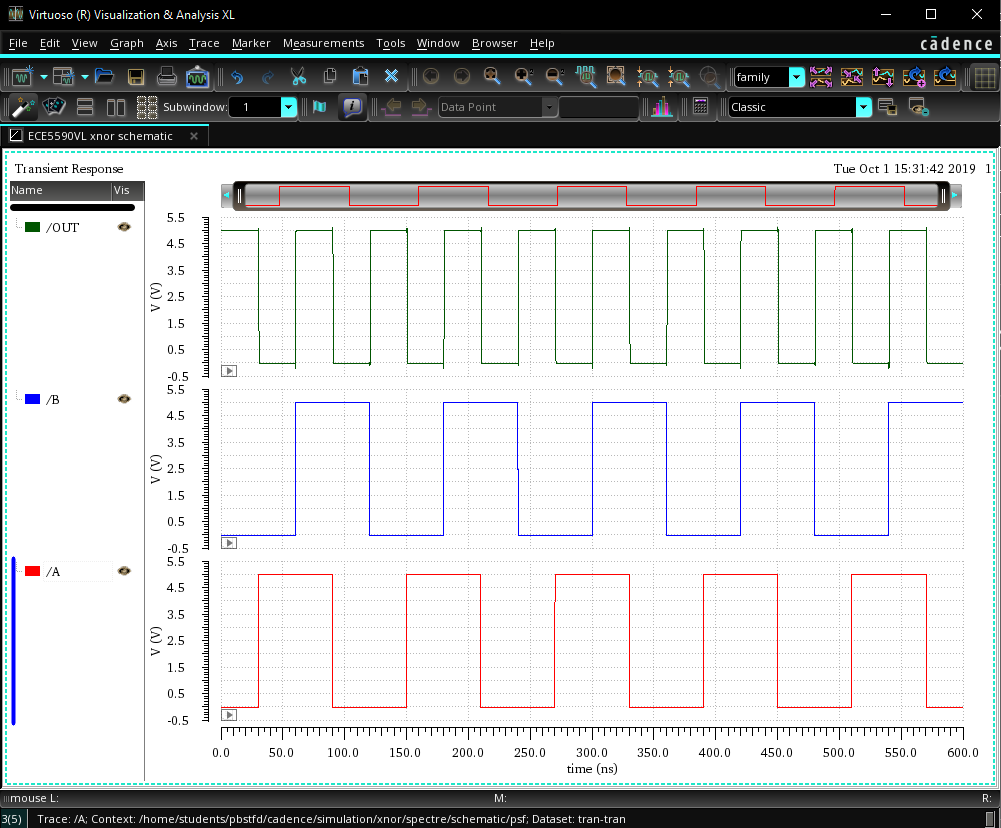
1. Follow the same procedure as in tutorial 1 and 2 to create the schematic, symbol and layout.
2. Name all the filenames by same name. Only the test schematic file will have different name.
3. First create the schematic and test if logic is correct by simulation. Add the inverter in front of XOR schematic to get XNOR logic.
4. Then, create a symbol and save the test schematic.
5. Create the layout by following the steps as for XOR gate.
6. In CIW window, in File🡪 New🡪 cellview🡪 give cell name same as that was given for the schematic and symbol, “xnor” and select the layout option in application.
7. Go in Create🡪 Instance and in NSCU\_TechLib\_ami06, add the 7 PMOS and 7 NMOS transistors with the properties same as the instances in schematic.
8. Press Shift + f for viewing the layout of the instances.
9. Use “metal1” to connect the wires and “poly” to connect the polysilicon gates. These options are available in “Layer” tab at the left side of screen.
10. Use meatl2 to connect all the horizontal connections.
11. Use “r” key draw rectangle, “m” key to move an object and “s” key to stretch a layer.
12. Add metal rectangles for VDD and GND. Extend the n-well to connect it to VDD.
13. To connect different layers, go in Create🡪 Via. Use “M1\_Poly” to connect Poly with Metal, “M1\_N” to connect N-well to VDD, “M1\_P” to connect GND and for poly with metal2 use first use M1\_P Via and on the same Via paste M2\_M2 Via.
14. Now, select metal1 and go in Create🡪 Pin and as per below image, create pin for vdd! gnd! and IN1, IN2, OUT. Select I/O type as “output” for the OUT pin. Place the pins on the layout at appropriate locations.
15. Perform LVS Check after creating layout.
16. Go in library and open the extracted layout of XNOR gate. Verify🡪 LVS. In schematic, browse the schematic file and in extracted, browse the extracted file of XNOR as per below image. 
17. Click on run and you must get job completed message. Afterwards, click on Output to get the report.

# 

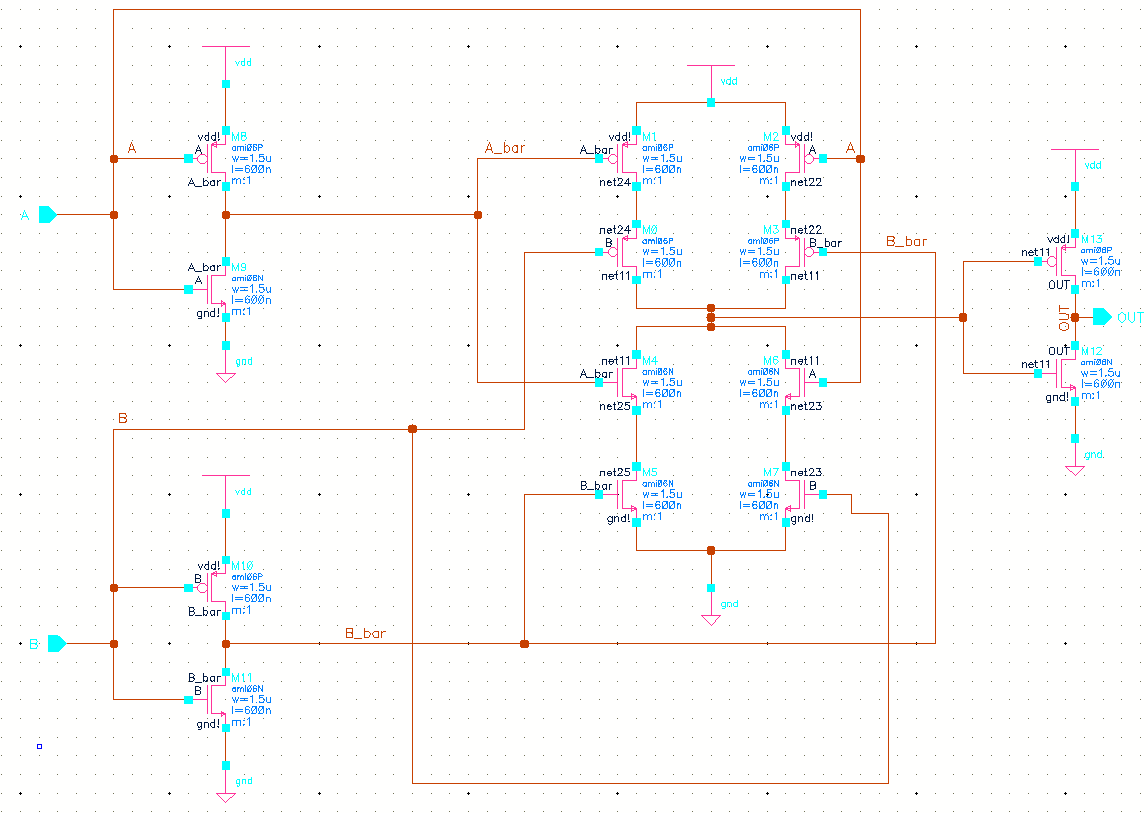
# Table/Graphs:

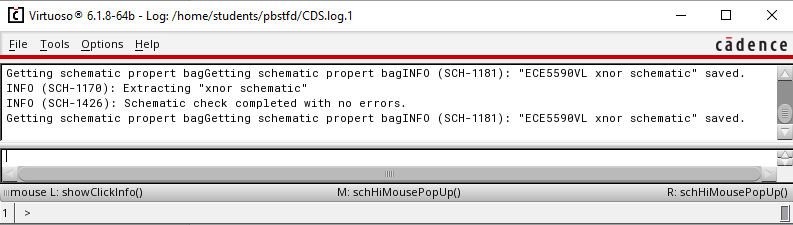
1. Schematic to verify the logic



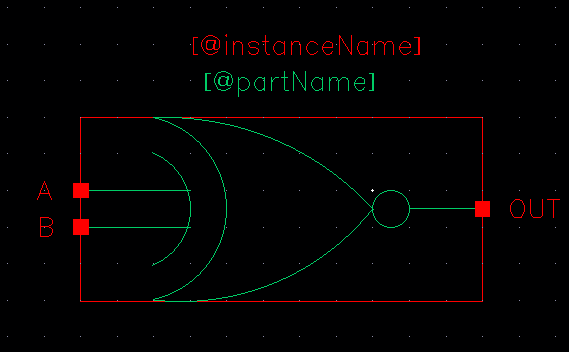


1. Schematic with pins

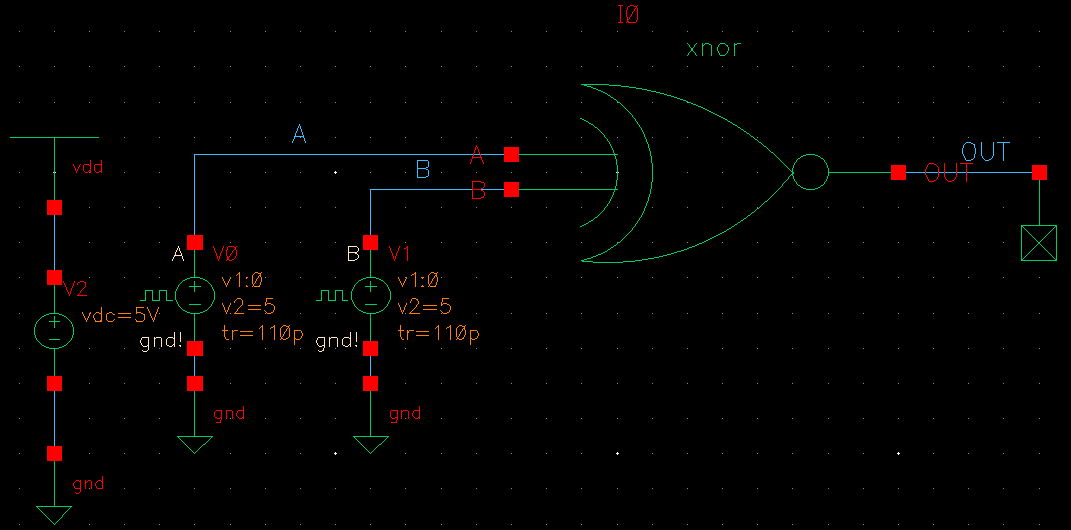


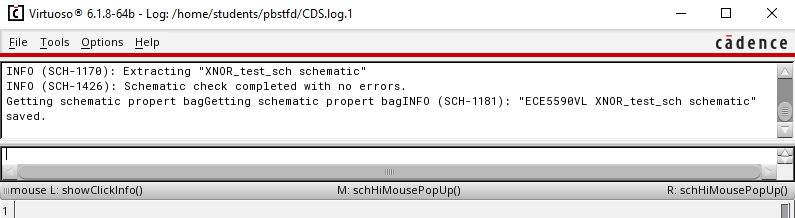


1. Symbol

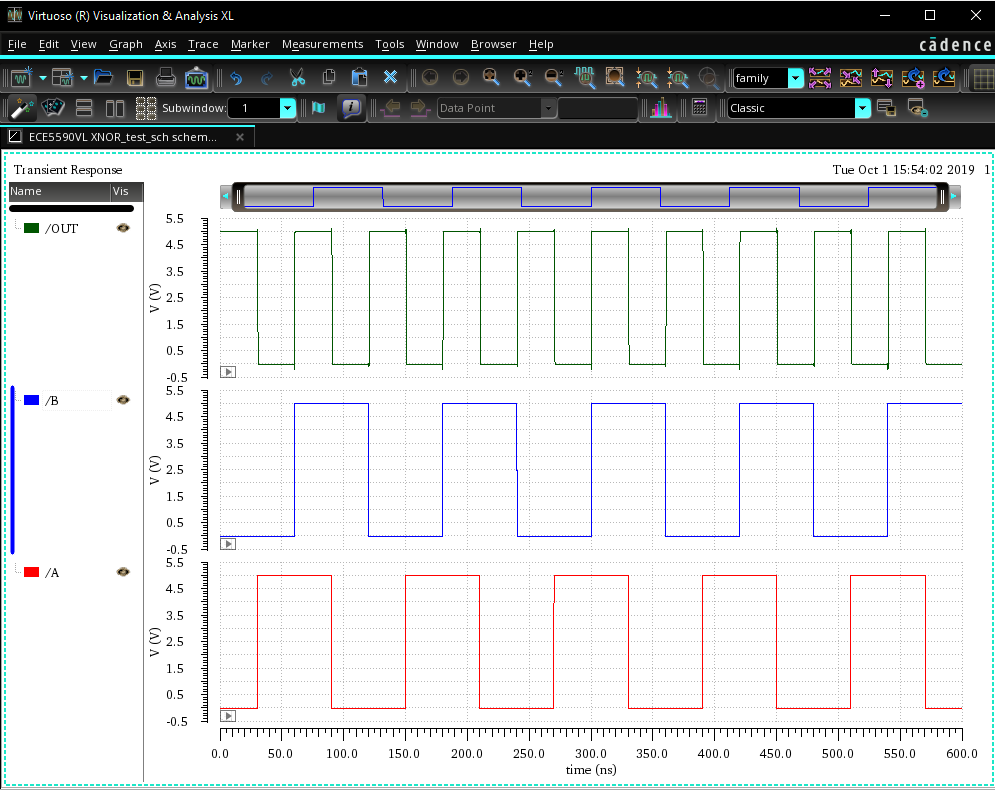


1. Schematic using Symbol

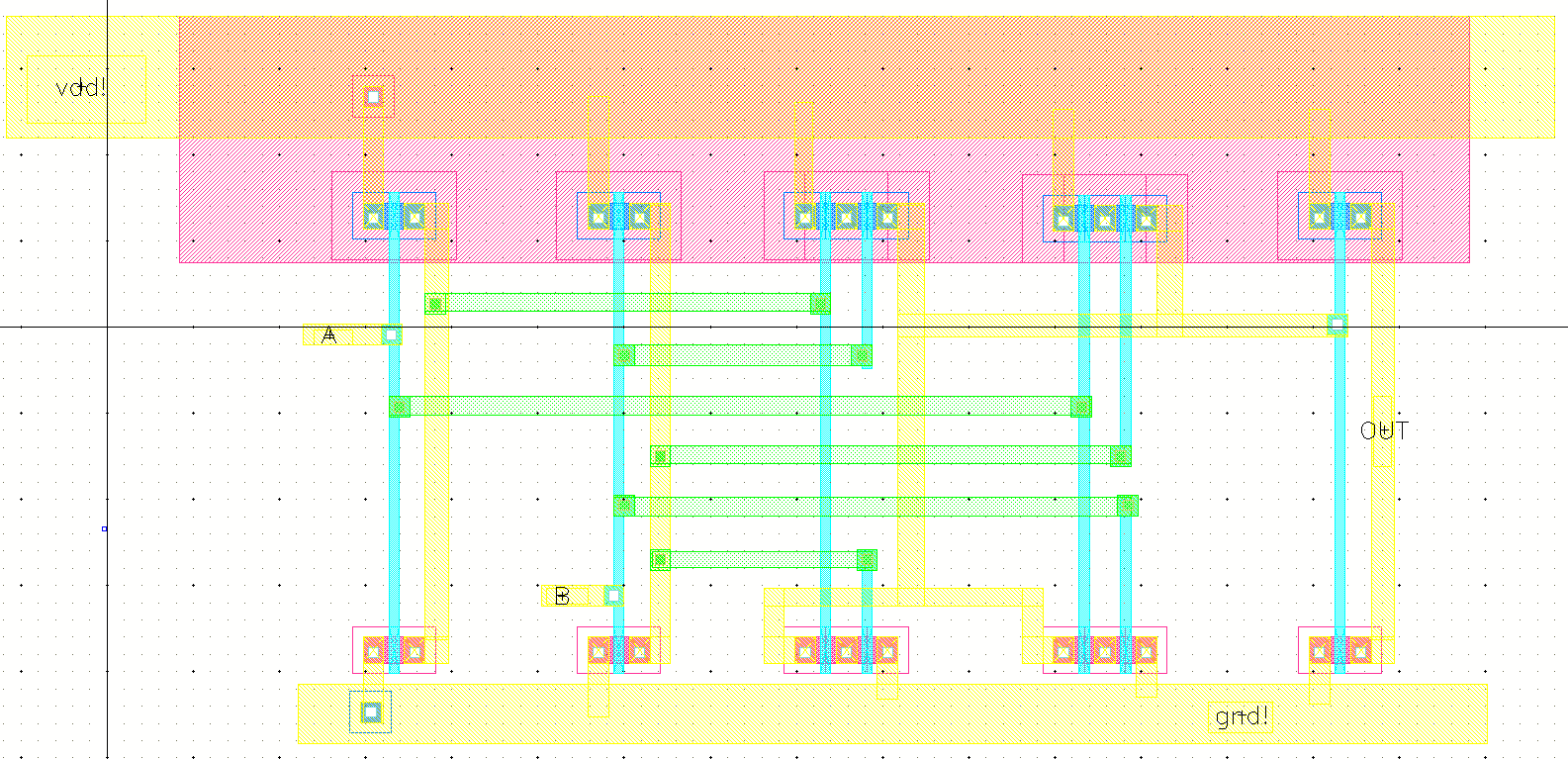




1. Simulation output with symbol schematic

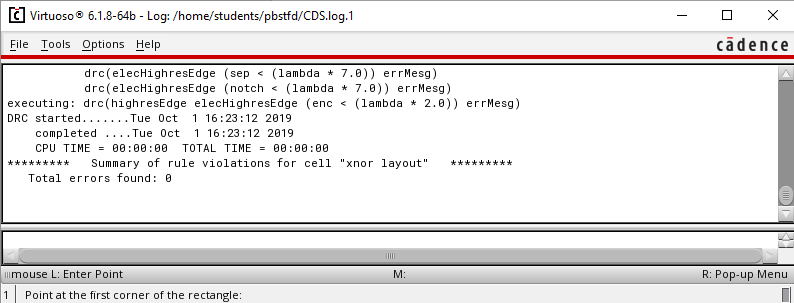


1. Layout for XOR

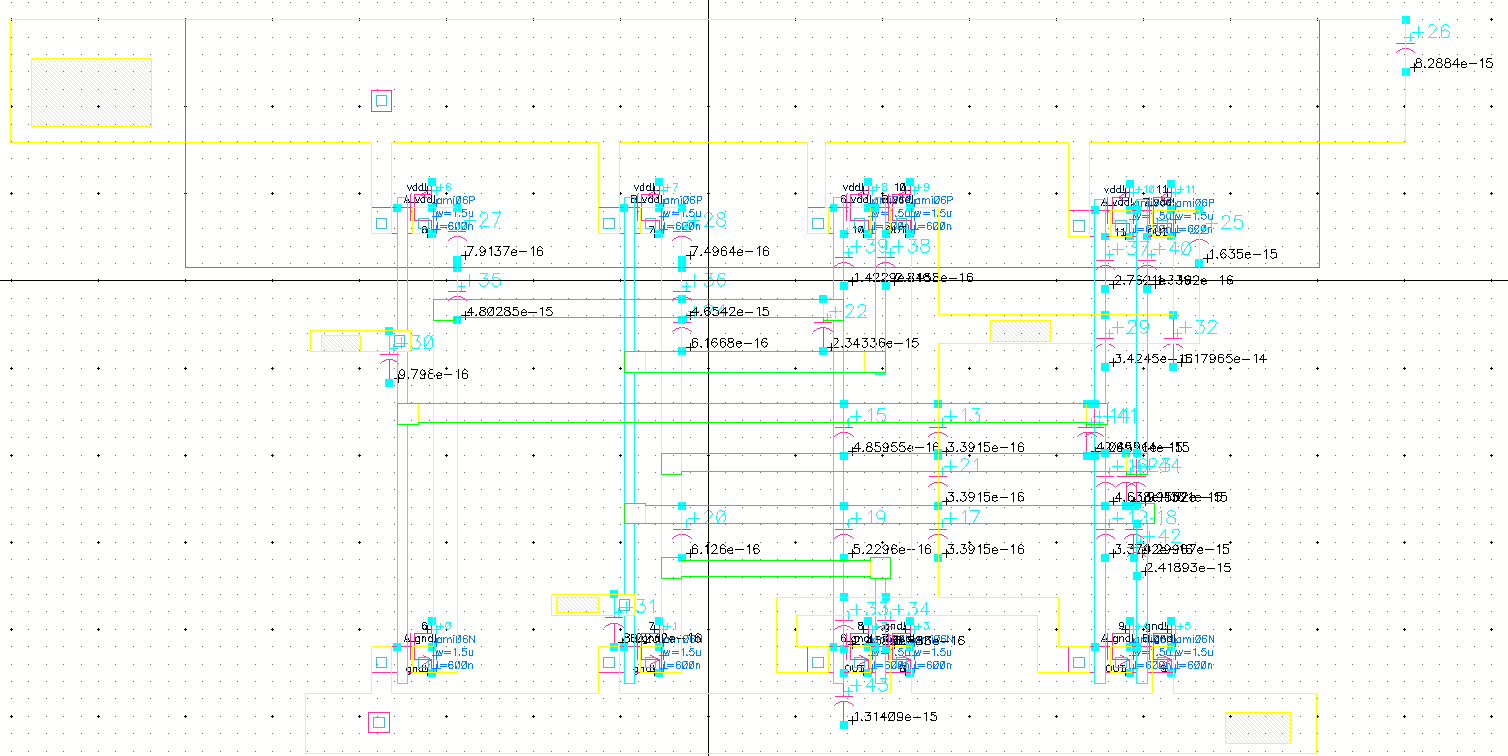


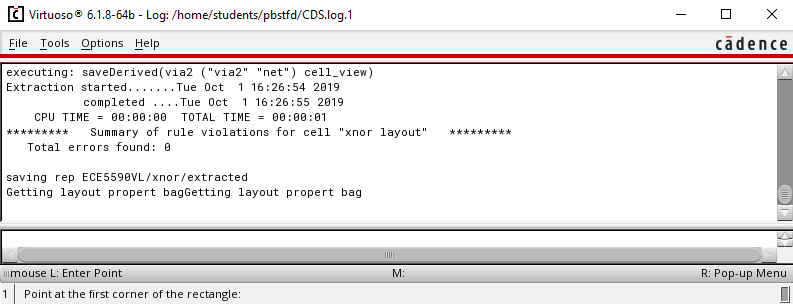
The green horizontal layer is metal2.

1. DRC Check

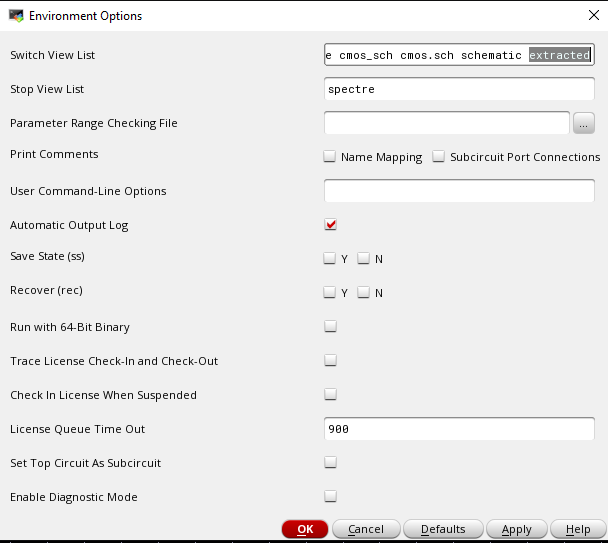


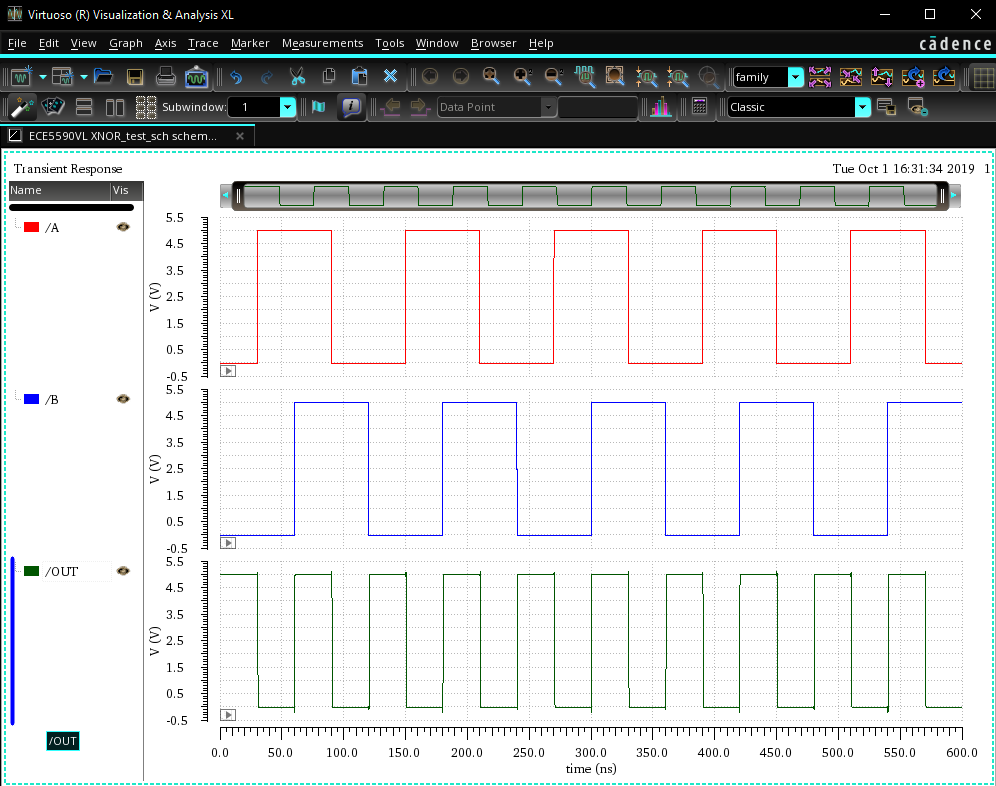
1. Extracted layout with parasitic capacitances



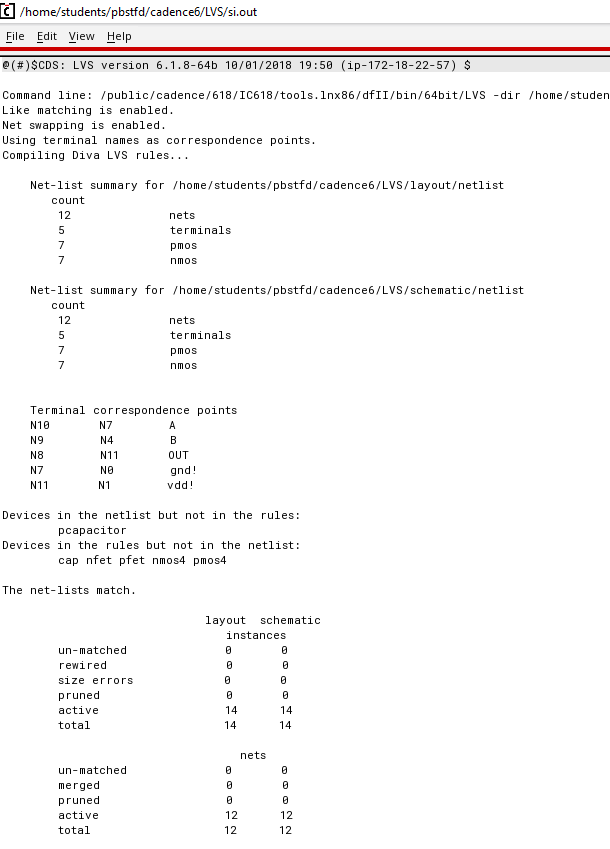


1. Simulation of Layout using extracted environment





1. LVS Check Output Report. Unmatched instances must be 0.



# Discussion of Result:

The LVS report proves that the schematic and layout match if un-matched instances are 0. The simulation result of schematic and extracted environment matches the truth table of XNOR gate.

# Conclusion:

In this lab session, we learnt to create complex layout using metal2 layer. When there are more number of PMOS and NMOS transistors, checking the individual blocks helped. The LVS check feature helps to verify if the schematic and layout match.