Course Number: EC-ENGR 5590VL-0001 Special Topics in ECE

LEC 47031

Tutorial: 4

Classwork

**TITLE**

Schematic, Symbol, layout design and LVS check for XOR gate using Cadence Virtuoso

Date of Performing Experiment: 24th September 2019

Due Date: 1st October 2019

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# Objective:

To draw schematic, symbol and layout for the XOR gate using Cadence Virtuoso. Performing LVS check on the schematic and extracted layout to verify if they match.

# Theory:

The XOR gate give high output only when there are odd number of high inputs. If both inputs are same i.e. (0, 0) or (1, 1) then the output is low. It is called exclusive OR gate.

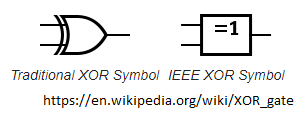
This practical introduces to the implementation of XOR gate using CMOS logic: NMOS and PMOS transistors. The implementation is done in Cadence virtuoso software.

XOR Gate:

Truth Table:

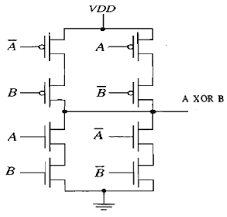
|  |  |  |
| --- | --- | --- |
| Input 1 | Input 2 | Output |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Symbol: XOR gate



Equation:

Circuit Diagram using CMOS:

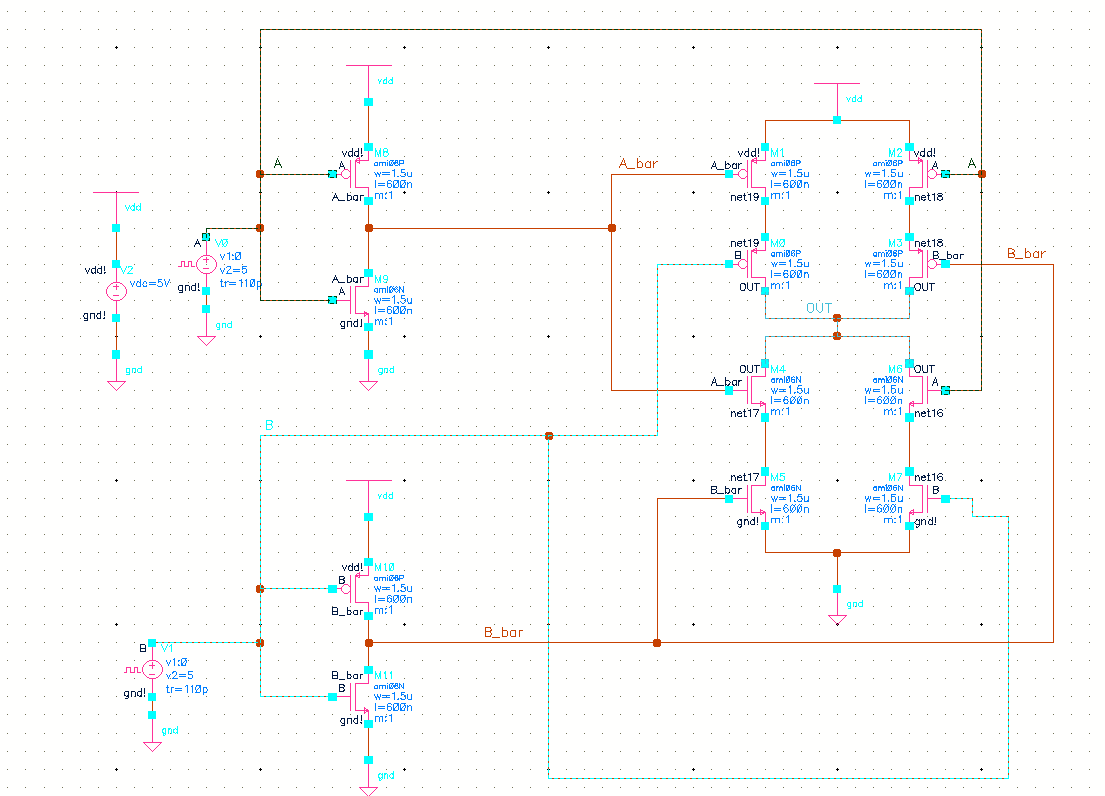


# Procedure:

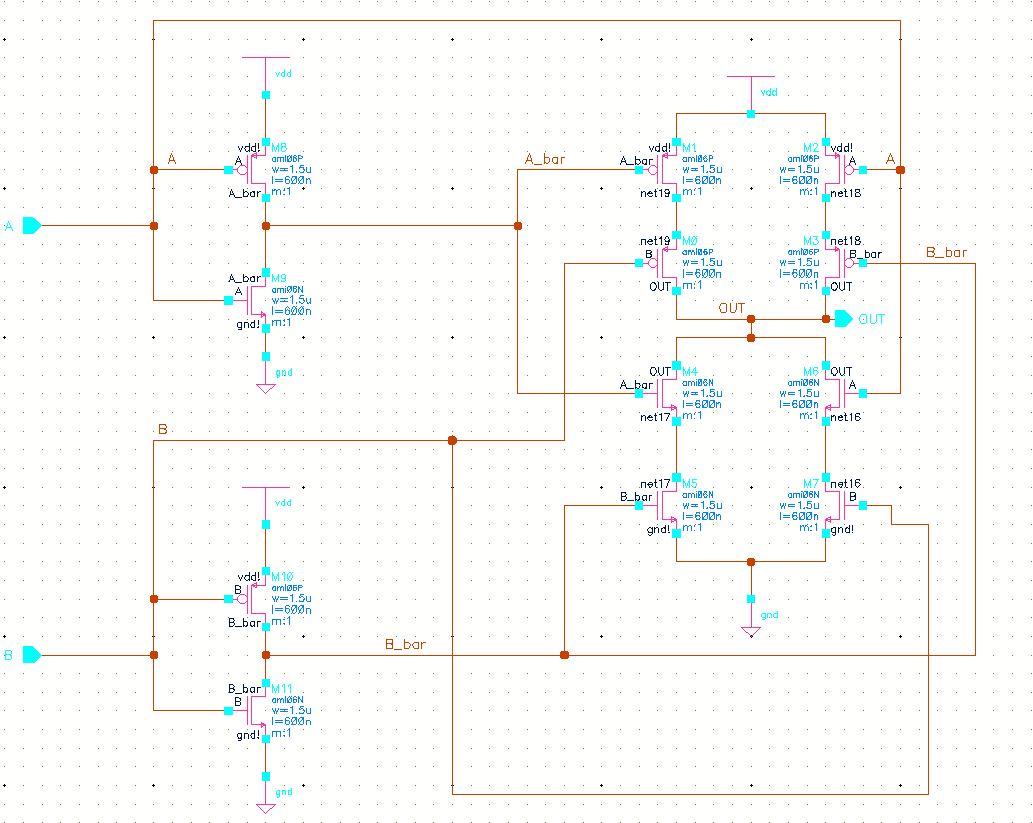
1. Follow the same procedure as in tutorial 1 and 2 to create the schematic, symbol and layout.
2. Name all the filenames by same name. Only the test schematic file will have different name.
3. First create the schematic and test if logic is correct by simulation.
4. Then, create a symbol and save the test schematic.
5. Create the layout by following the steps as for NAND gate but now for horizontal connection use the Metal2 layer. Use Shift+F to view layout of NMOS and NMOS components.
6. For connecting Vias from poly with Metal1 use M1\_P, metal1 to vdd (n-well) use M1\_N, metal1 to gnd (p-well) use M1\_P and for poly with metal2 use first use M1\_P Via and on the same Via paste M2\_M2 Via.

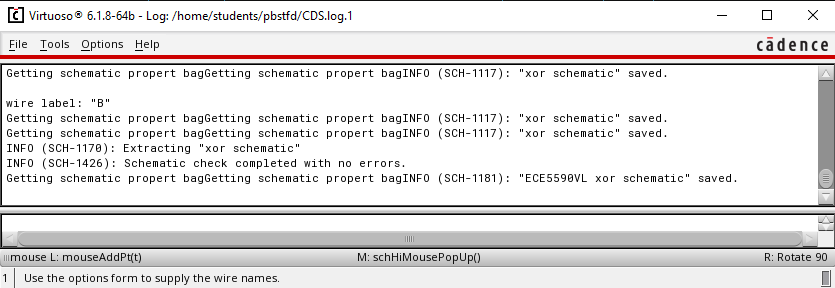
# Table/Graphs:

1. Schematic to verify the logic

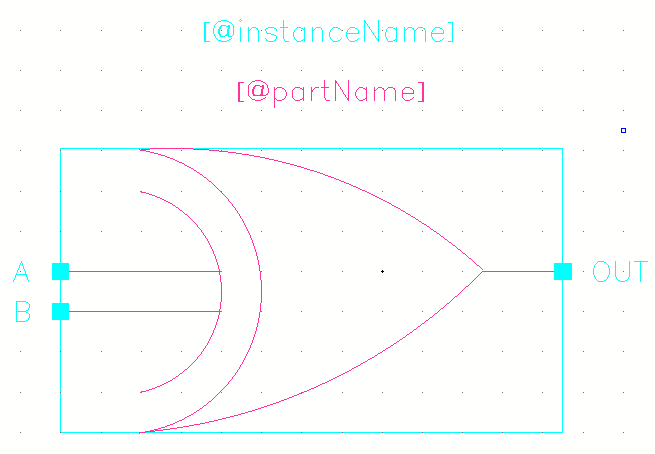


1. Schematic with pins

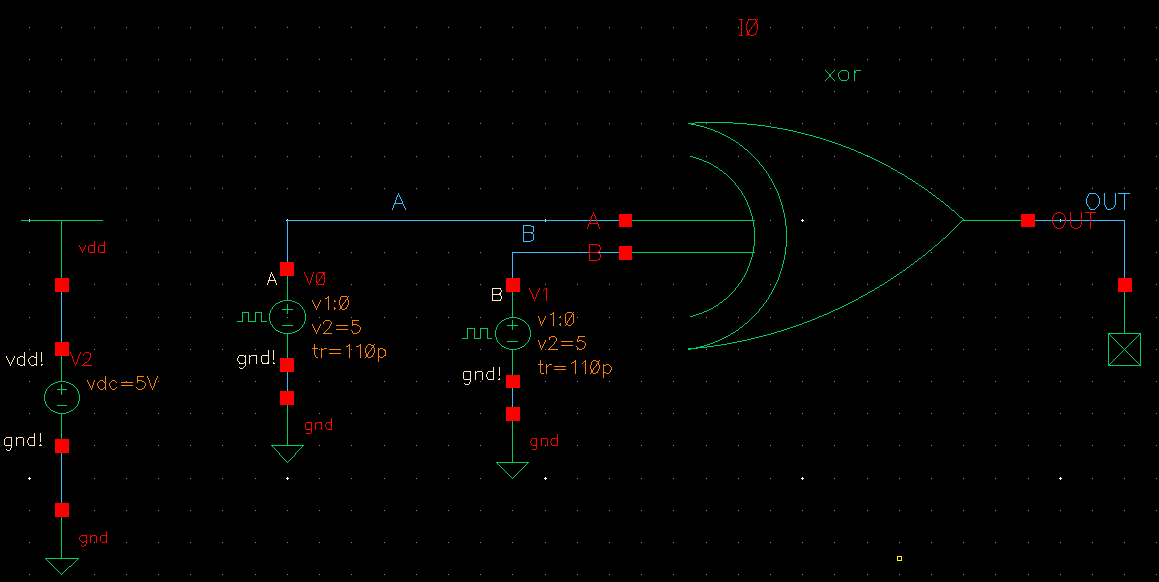


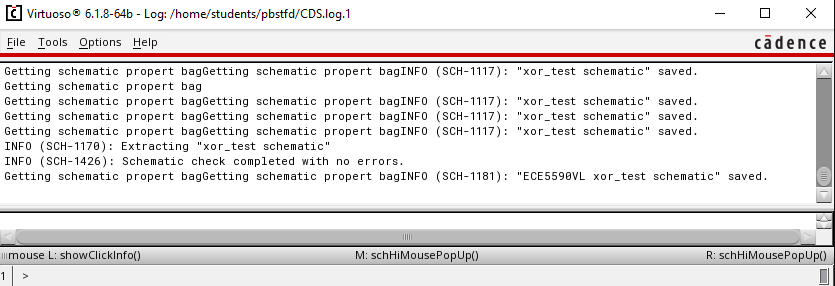


1. Symbol

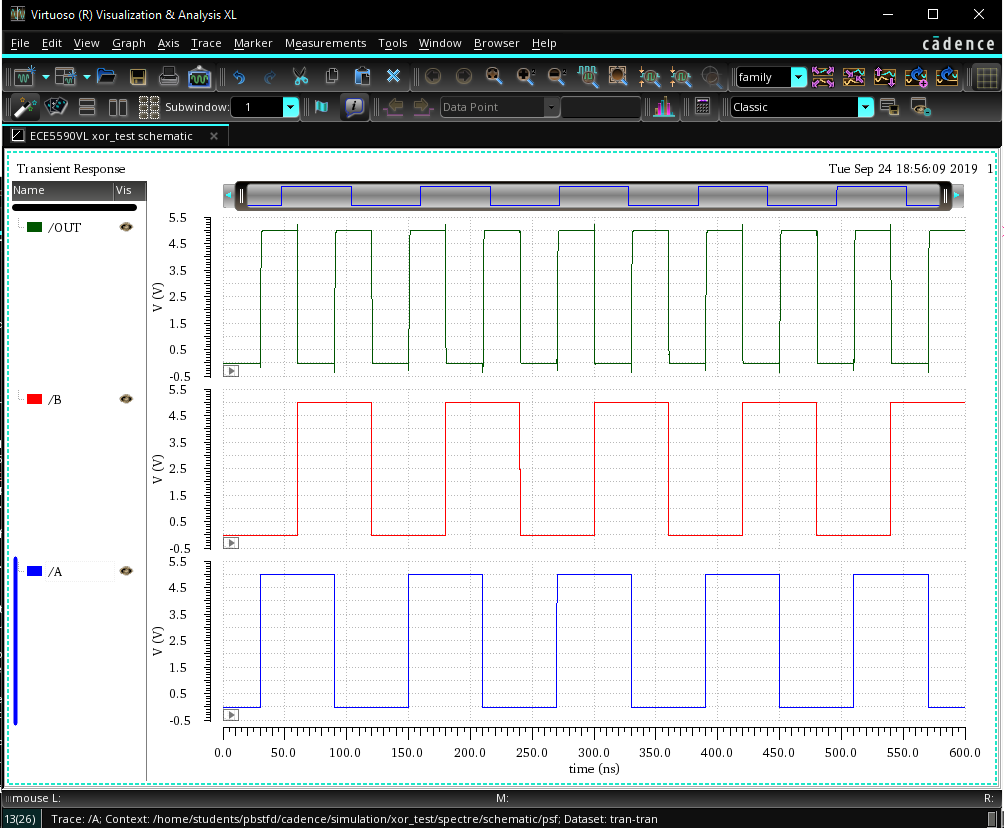


1. Schematic using Symbol

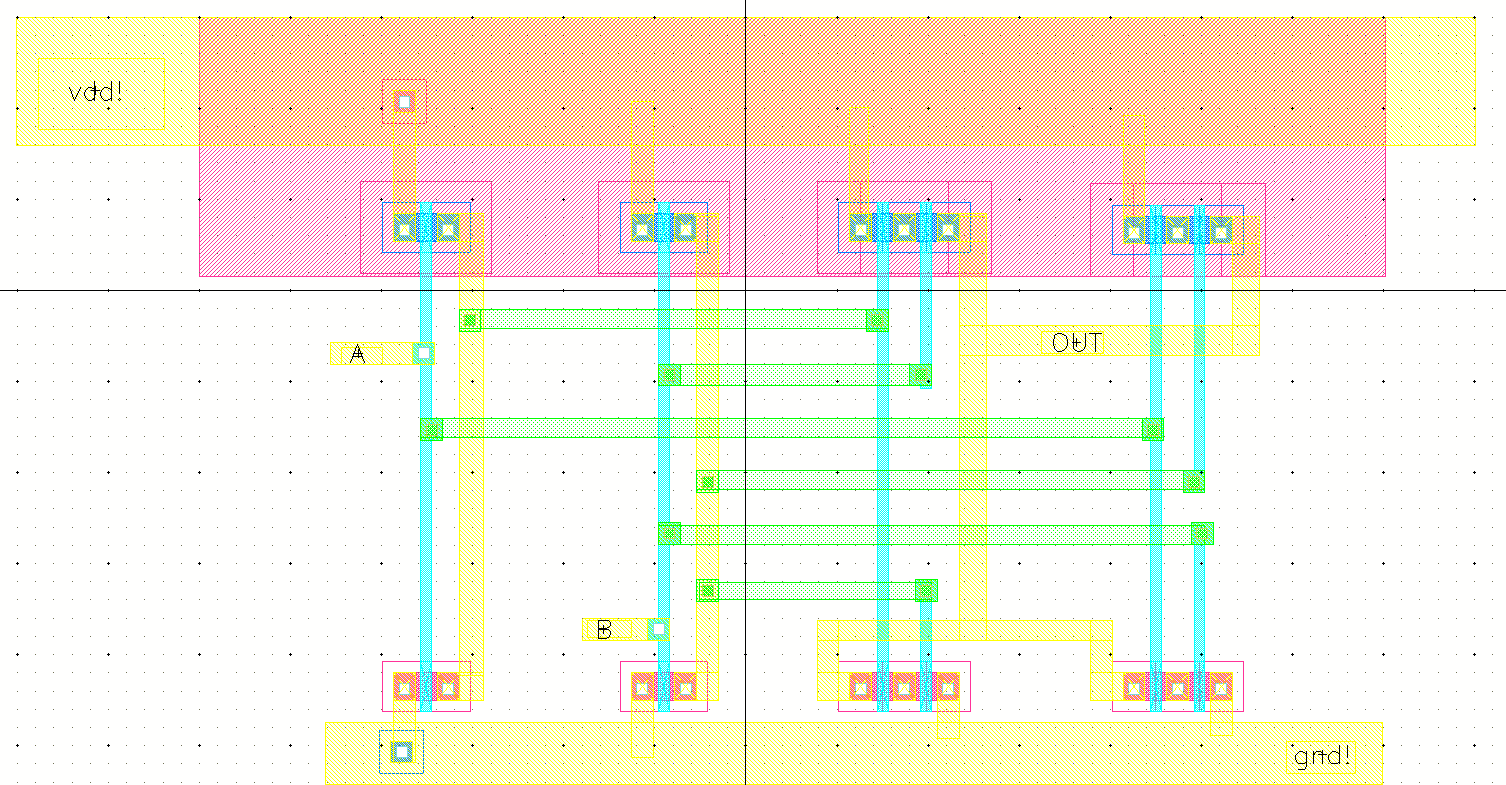




1. Simulation output with symbol schematic

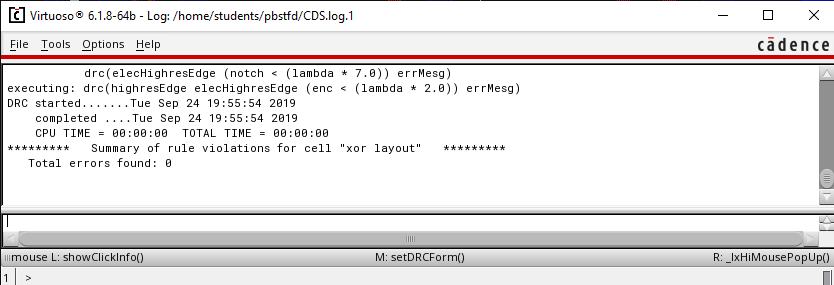


1. Layout for XOR

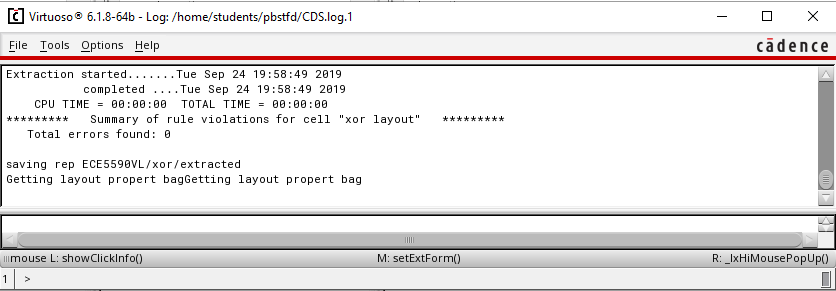


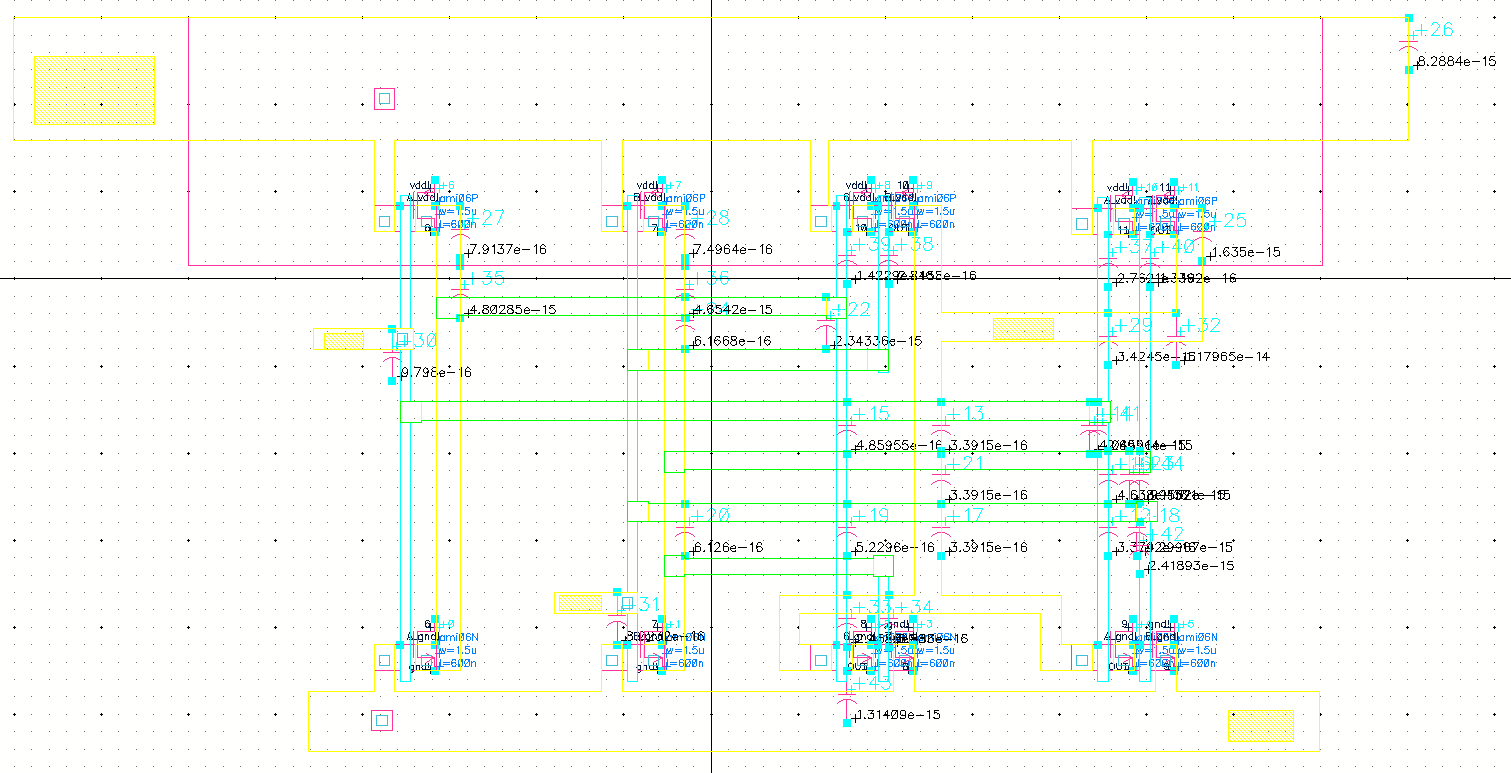
The green horizontal layer is metal2.

1. DRC Check

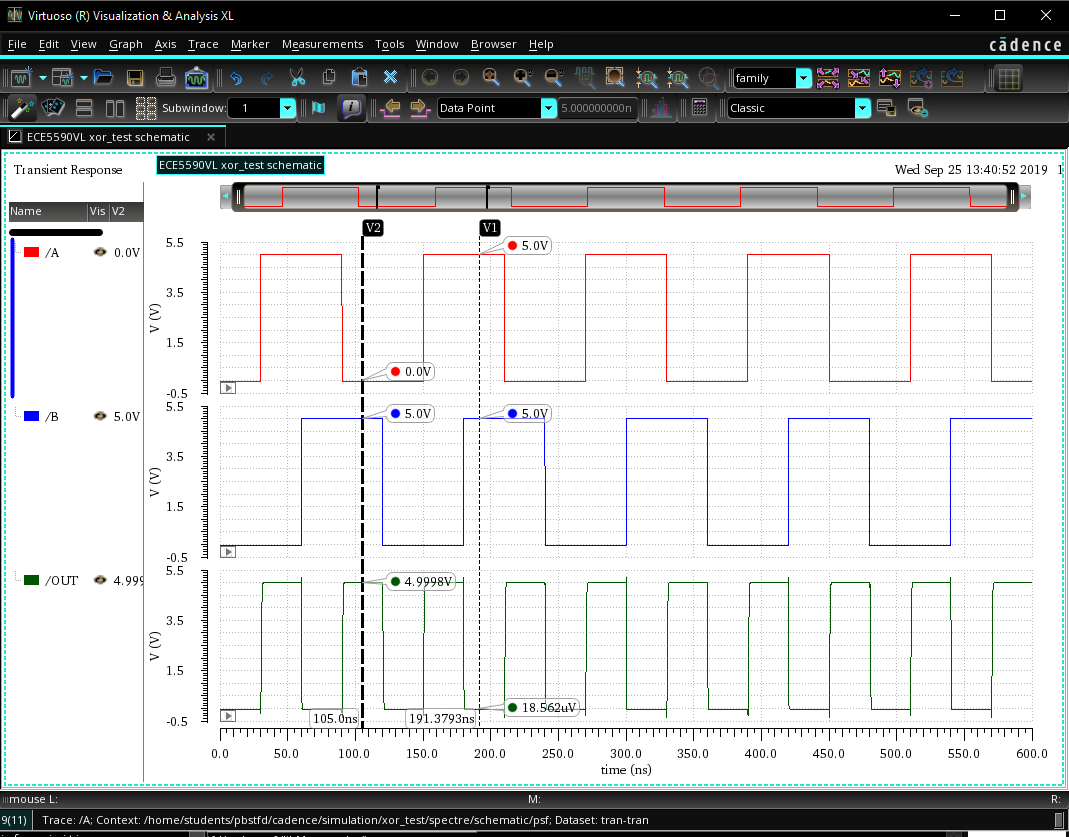


1. Extracted layout with parasitic capacitances

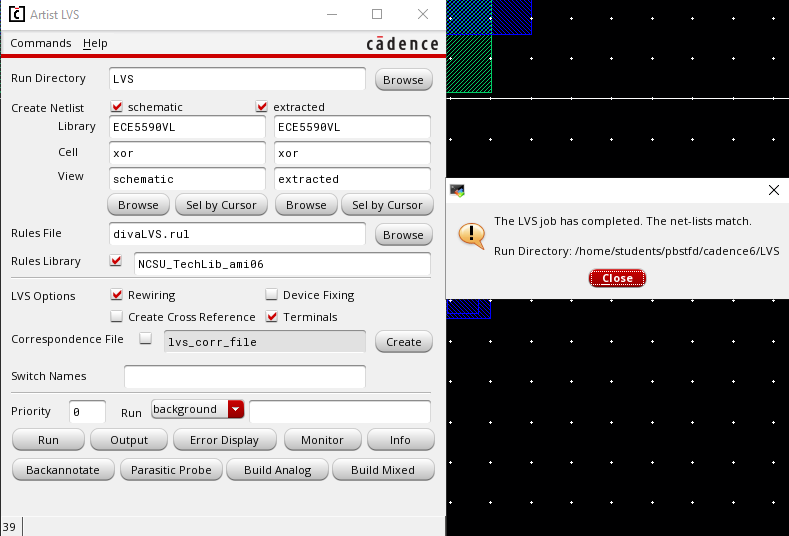




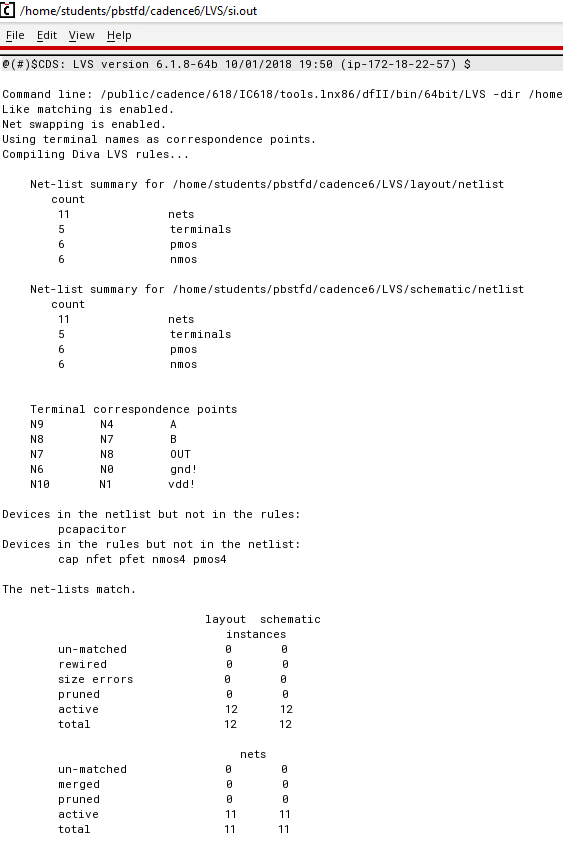
1. Simulation of Layout using extracted environment



1. LVS Check. Go in library and open the extracted layout of XOR gate. Verify🡪 LVS. In schematic, browse the schematic file and in extracted, browse the extracted file of XOR as per below image. Click on run and you must get job completed message. Afterwards, click on Output to get the report.



1. LVS Output: Unmatched instances must be 0.



# Discussion of Result:

The LVS report proves that the schematic and layout match if un-matched instances are 0. The simulation result of schematic and extracted environment matches the truth table of XOR gate.

# Conclusion:

In this lab session, we learnt to create complex layout using metal2 layer. When there are more number of PMOS and NMOS transistors, checking the individual blocks helped. The LVS check feature helps to verify if the schematic and layout match.