Course Number: EC-ENGR 5590VL-0001 Special Topics in ECE

LEC 47031

Tutorial : 1

**TITLE**

Introduction to Cadence and Schematic design of NAND and NOR Gate using Cadence

Date of Performing Experiment: 3rd September 2019

Due Date: 10th September 2019

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**Name: Prerana Samant**

# Objective:

To Setup and configure Cadence Virtuoso using MobaXterm and create schematic for basic gates (NAND and NOR gate) using Cadence.

# Theory:

The NAND and NOR gates are universal gates in digital circuits since all the gate logic can be implemented using these gates. The implementation of these gates requires two NMOS transistors and two PMOS transistors. This practical introduces to the basic implementation of NAND gate using CMOS logic: NMOS and PMOS transistors. The implementation is done in Cadence virtuoso software.

NAND Gate:

This gate produces 1 when any of the input is 0 and produces 0 only when all the inputs are 1.

Truth Table:

|  |  |  |
| --- | --- | --- |
| Input 1 | Input 2 | Output |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

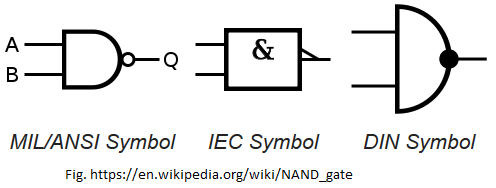
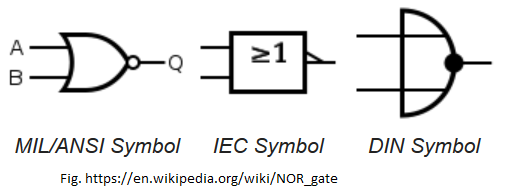
NOR Gate:

This gate produces 1 only when all inputs are 0. If any of the input is 1, it produces 0 output.

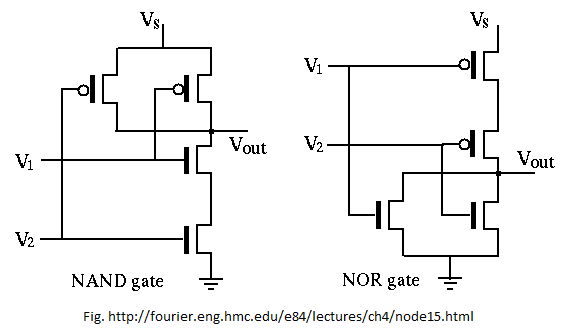
Truth Table:

|  |  |  |
| --- | --- | --- |
| Input 1 | Input 2 | Output |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

Symbol: 1. NAND gate 2. NOR Gate

Circuit Diagram using CMOS:



# Procedure:

1. Open MobaXterm, new TUX cluster window. Type password.
2. For first time installing Cadence, make directory Cadence6, run setup and enter the directory using following commands.

mkdir Cadence6 (Enter)

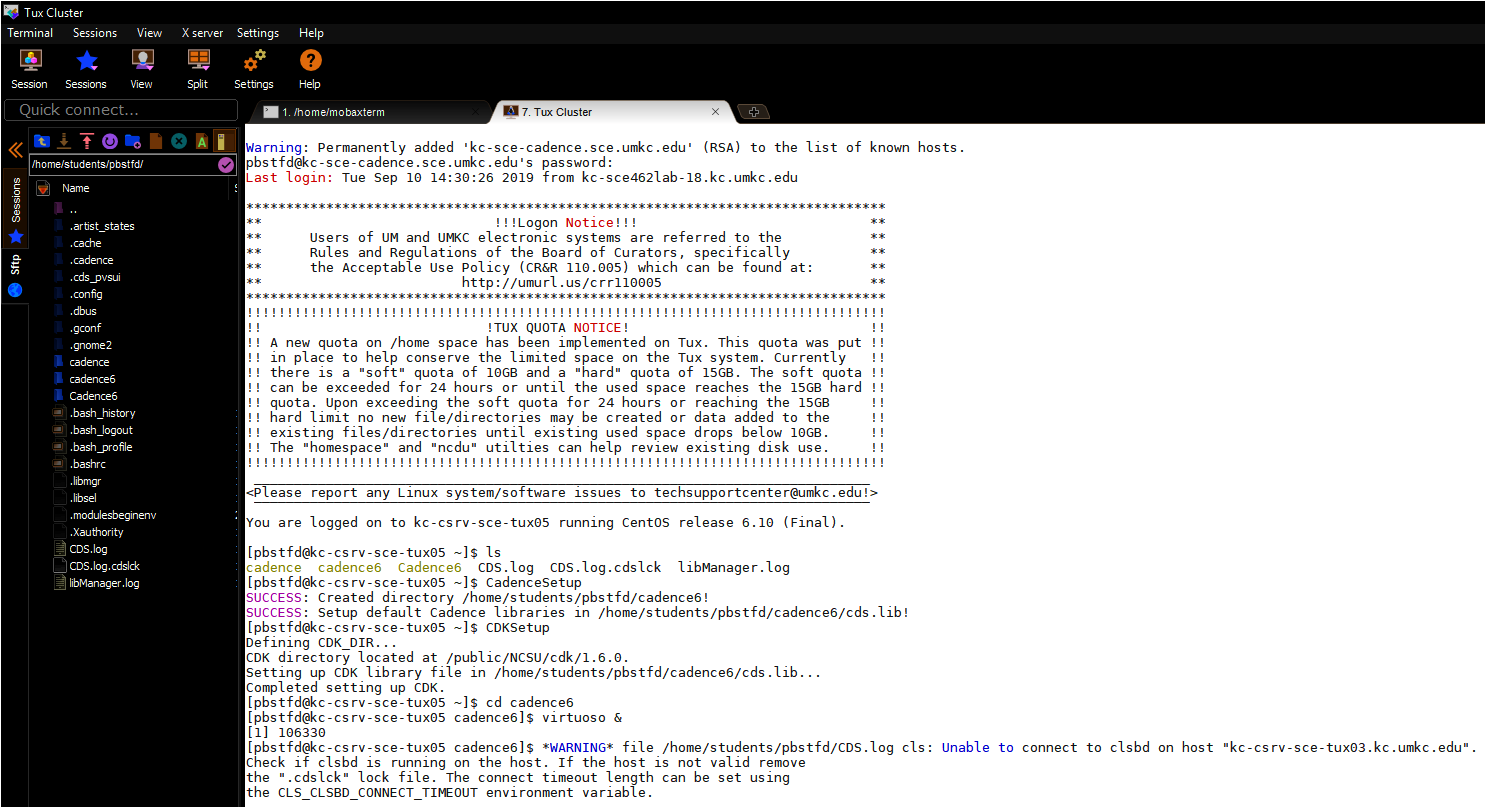
ls

CadenceSetup(Enter)

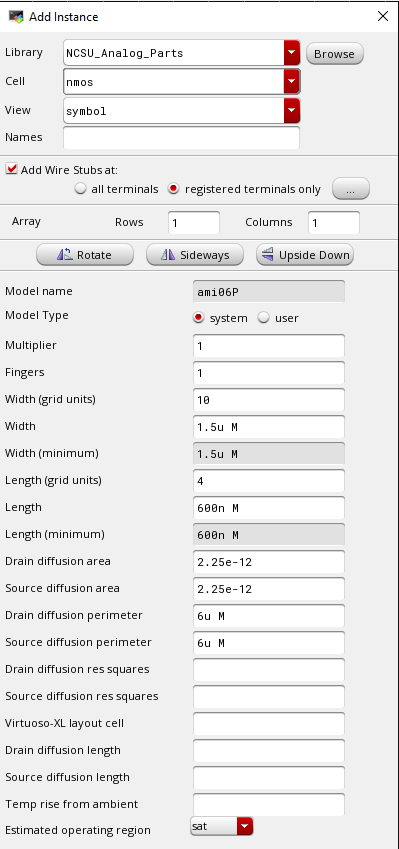
CDKSetup(Enter)

Cd cadence6

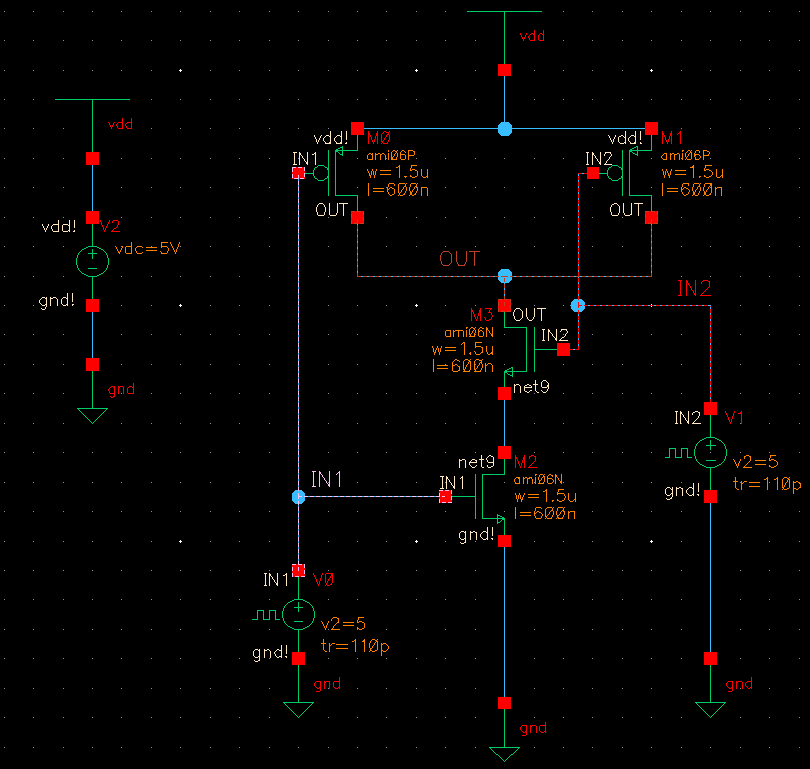
Virtuoso &



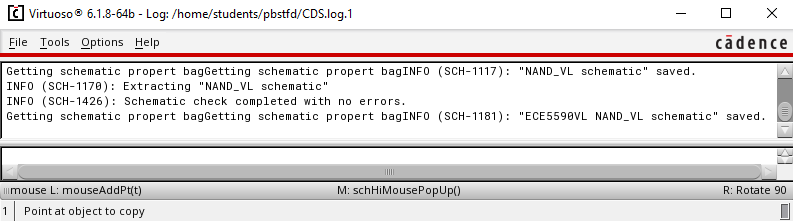
1. Create the new Library by clicking on New 🡪 Library in “New Library” tab. Give any name and attach it to the existing library “NSCU\_TechLib\_ami06”. Click ok.
2. Go in File🡪 New🡪 Cellview. In New File, select the created library, give cell name as “NAND\_VL”. In Application tab, select “Open With” as “Schematic L”. This will open the schematic editor.
3. Next task is to add NMOS and PMOS transistors. Create🡪 Instance. In “Add Instance” tab, click on browse. This will open the “Component Browse window”.
4. Select the NSCU\_Analog\_Parts. Select P\_Transistors🡪 PMOS. Then select the PMOS transistor. After clicking on close, the cursor will appear as PMOS symbol. Place the symbol at the required location. Since, we require 2 PMOS transistors, place one more symbol and then click “ESC” key.
5. To change the properties, right click the component and select properties. Edit the properties as shown in figure and then click “OK” at the bottom of the window.



1. Similarly, place the NMOS transistors by selecting N\_transistors🡪 NMOS in “Component Browse” window. Edit the properties of NMOS like PMOS.
2. Create the circuit for NAND gate as per the theoretical circuit.
3. Add the VDD, GND and Vpulse to simulate the circuit. Select them by, create 🡪 Instance🡪 selecting VDD/GND/Vpulse. Configure the timings of Vpulse with rise time/ fall time (110psec), period (120ns), pulse width (60ns) and different delays for two sources (60ns and 120ns), voltage1=5V, voltage2=0V. Also, set the voltage of VDC to 5V.
4. Add the connecting “wires” by clicking the red box on the components. Drag the mouse to connect it to the other terminal.
5. Now Create🡪 Wire Name. In “Create wire name” type names of wires for inputs and outputs. For e.g. IN1 IN2 OUT. Click on “hide” and then click on the schematic on the respective wires to name them.
6. The schematic looks like below image.



1. Click check and save button. The virtuoso window must show “no errors”.



1. Now, simulate the circuit by Launch🡪 ADE L. In the virtuoso Analog design environment, click Setup🡪 Model Libraries 🡪 click to add files🡪 click on the 3 dots to upload files.
2. In “Choose model file window” select the matlab files “ami06N.m” and “ami06P.m” (copy these files to the Cadence6 folder using FileZilla). Click on “Open”🡪 OK.
3. In “Analyses” tab 🡪 choose “tran” for transient analysis. Set stop time as 600ns. Click OK.
4. Click Outputs🡪 To be plotted🡪 Select on Schematic. Now select the signals from the schematic.
5. Go in Simulation🡪 Run or Green arrow on the Window. Simulation window will open. Click on “split all strips”. The inputs and outputs will be shown as individual waveforms one above the other. Verify the output as per truth table.

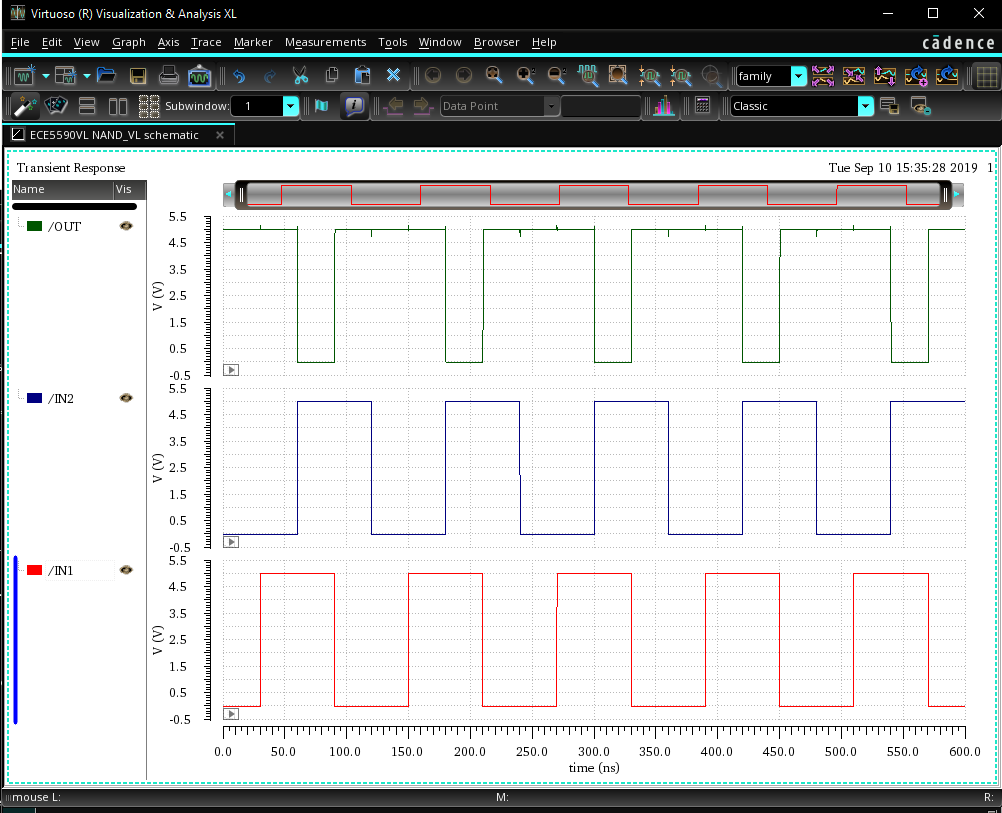
A screenshot of a cell phone

Description automatically generated

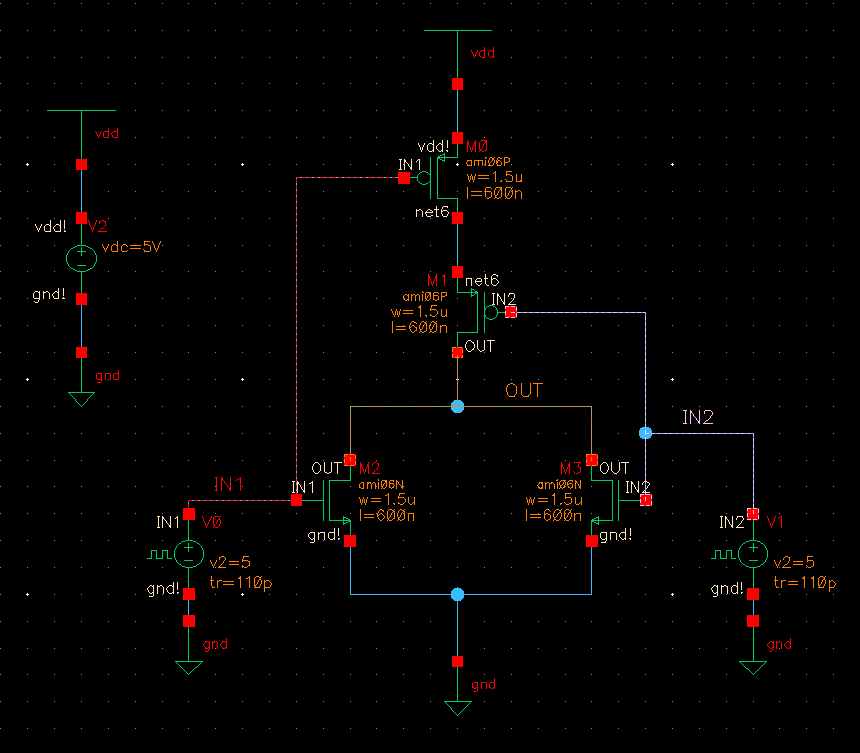
1. Repeat similar steps for NOR gate. Create schematic as per the circuit diagram. The results of NOR gate are in below section.

# Table/Graphs:

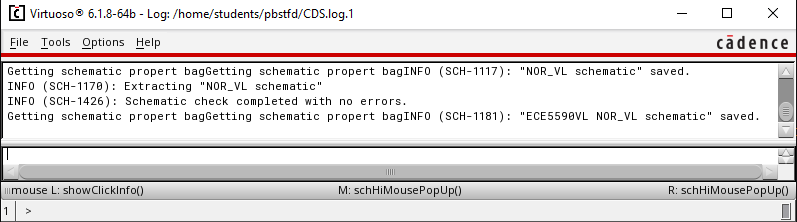
1. Simulation NAND gate



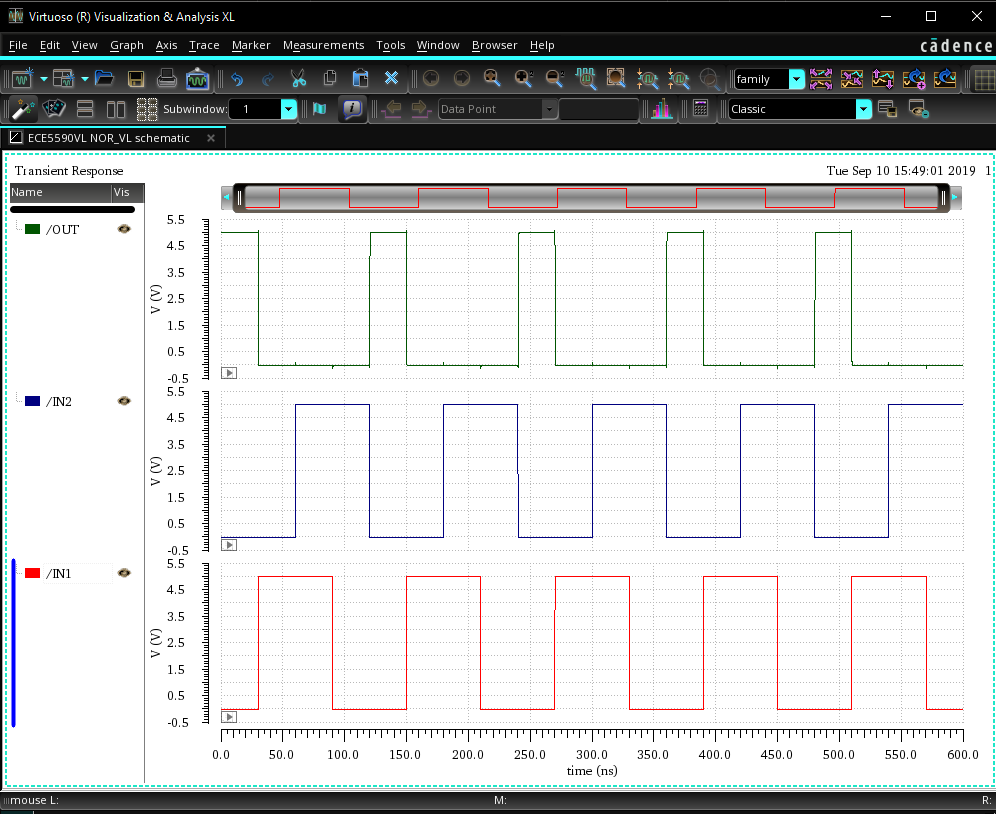
1. Schematic NOR Gate

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1. Virtuoso log NOR Gate



1. Simulation output NOR Gate



1. Virtuoso Log Simulation NOR gate

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# Discussion of Result:

The waveforms of simulations of NAND gate and NOR Gate match with the truth table for all the combinations.

# Conclusion:

In this lab session, we learnt to create the schematic of NAND and NOR gate using CMOS circuit using Cadence Virtuoso. We also understood the steps for simulating the schematic by adding the model libraries to the PMOS and NMOS transistors.

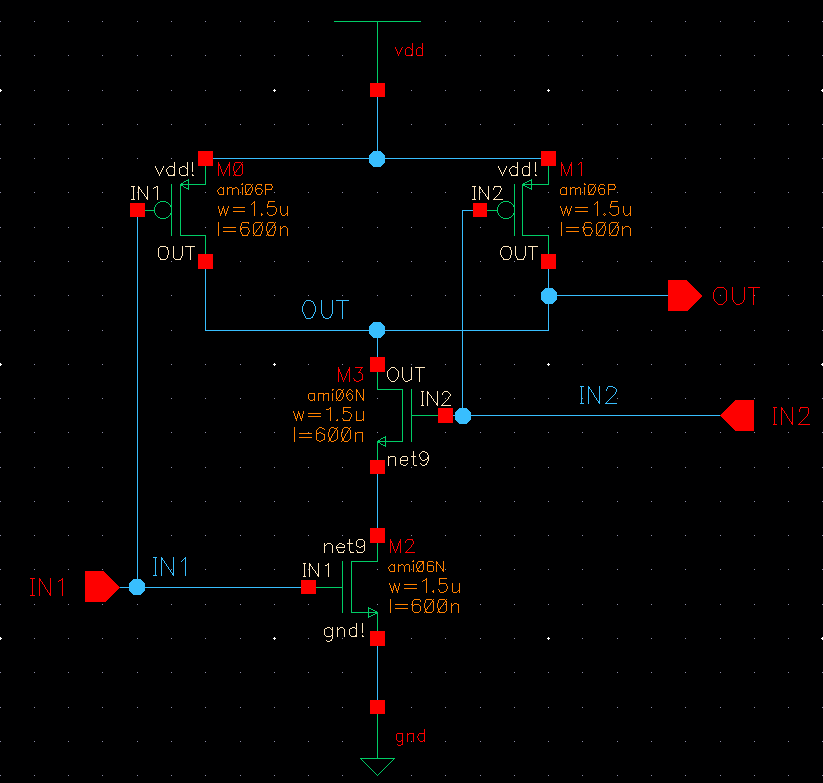
Homework: Tutorial 1 (STudent ID 14344331)

Title:

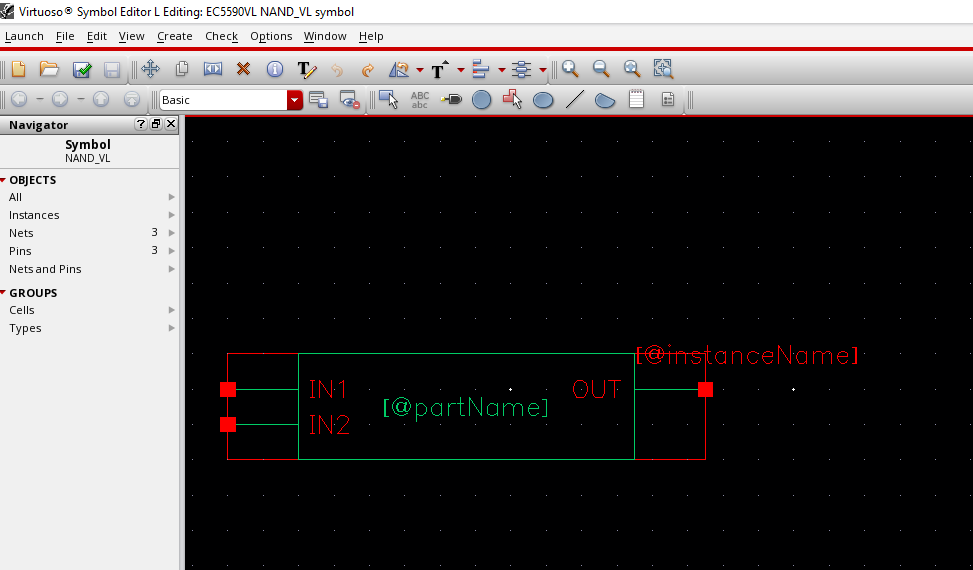
Creating NAND Symbol from the NAND Schematic

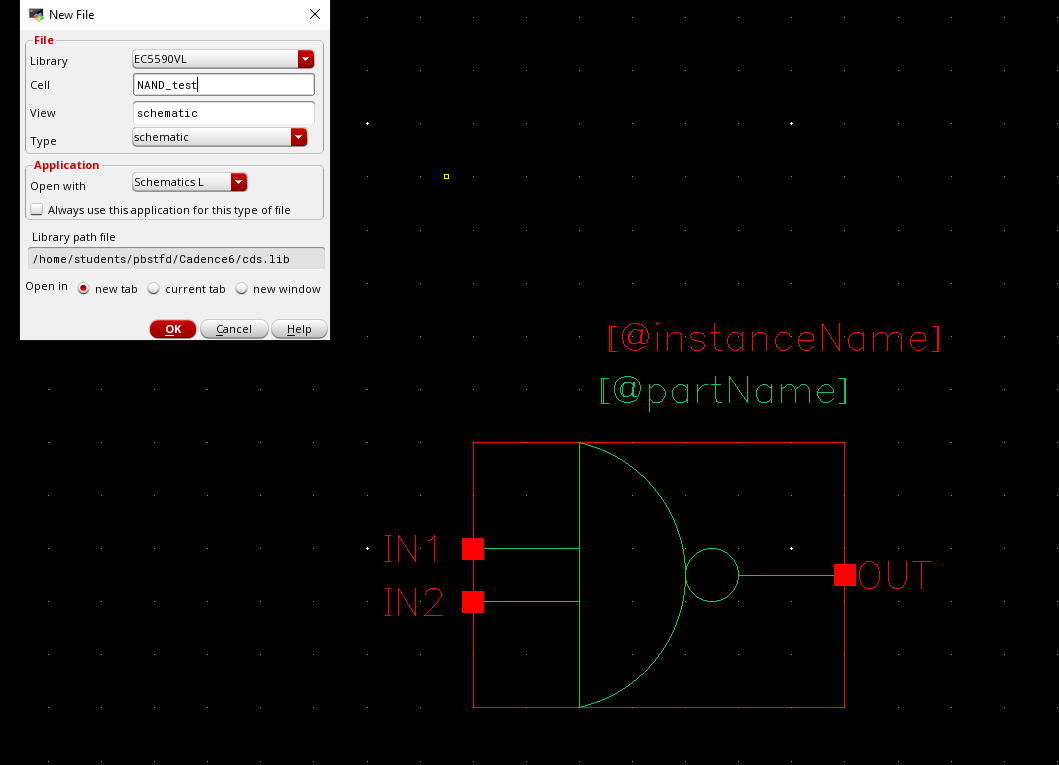
# Procedure:

1. Open the NAND Schematic created in 1st Lab session.
2. Delete the VDD, GND, the two Vpulse signals and 5V voltage source. Keep one VDD and GND connection as per below image.
3. Click on Create 🡪 Pin. In “Create Pin” window type names of Pins: IN1 IN2. Select direction as “input”. Click “hide”. Place the pins at the respective positions in the schematic. Repeat the process for output pin: OUT, by selecting direction as “output”. The schematic is as follows after adding pins.



1. Click on Create 🡪 Cellview🡪 From Cellview. In Cell name, type NAND\_VL. Click OK. In “Symbol Generation Option”, “Left Pins” has input names and in “Right Pins” have output names. Click OK.
2. Delete the green and red lines in the symbol to create a customized symbol. A standard NAND gate symbol can be created.
3. Using create 🡪 Shape🡪 Line, arc and Circle, create a standard symbol. Connect the wires with the pins.
4. Click Create🡪Selection Box 🡪 Automatic 🡪Hide. Selection box gets added automatically. Adjust by dragging if alignment is wrong.
5. To simulate, Go in File🡪 New File window, type under “Cell” NAND\_test. Click OK.

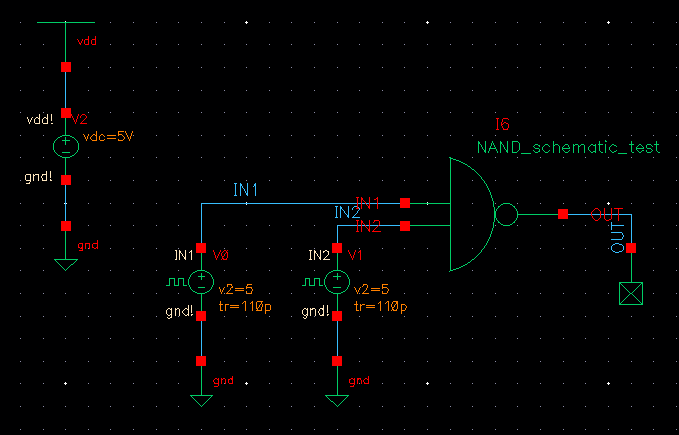




1. Create 🡪 Instance🡪 Browse. Click on “Hide”. On “Component Browser” window, select the created library (EC5590VL) and Select the NAND\_Schematic\_Test symbol. Place the symbol on the schematic as instance.
2. Go in Create 🡪 Instance. Add all the power sources that were deleted earlier. VDD, GND, Vsource and two Vpulse signals from the “basic” library.
3. Add “noConn” at the output. Create🡪 Wire Name, as done in previous schematic. Check and Save the schematic.
4. Launch🡪 ADE L and repeat the simulation steps as in assignment 1.

# Tables/Graphs:

1. Schematic of NAND using symbol

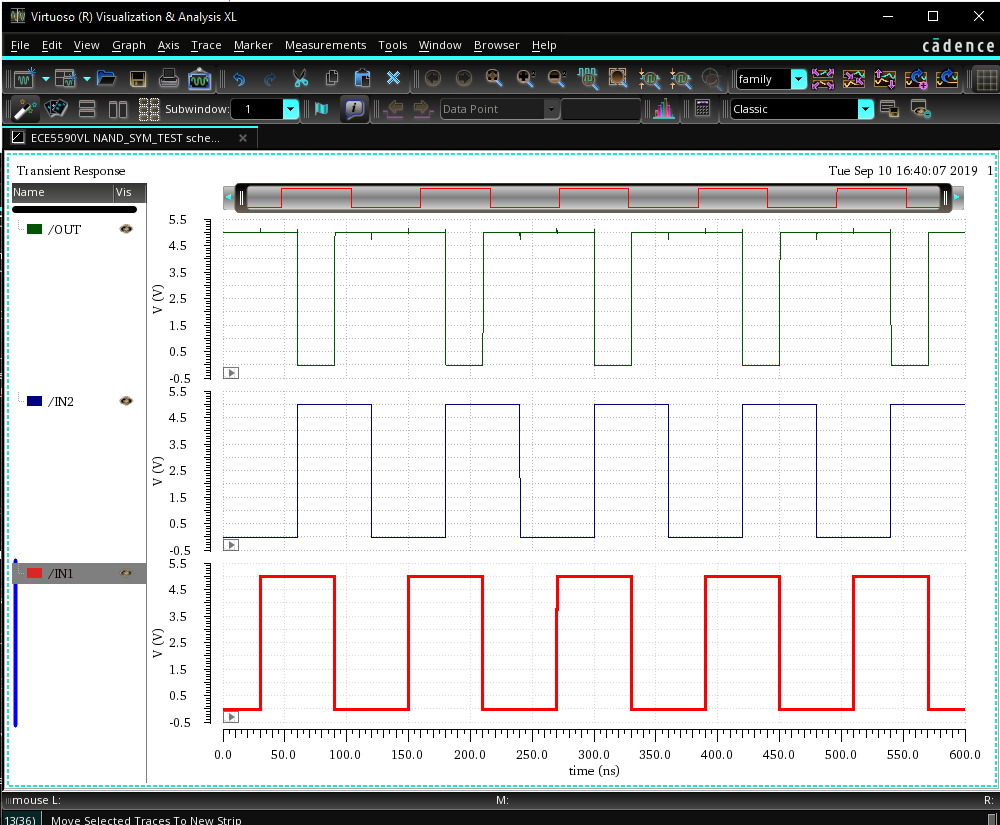


1. Log of Virtuoso check and save

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1. Simulation using NAND symbol



1. Simulation log

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Description automatically generated