Course Number: EC-ENGR 5590VL-0001 Special Topics in ECE

Tutorial

(Lab report + Homework)

**TITLE**

Schematic, Symbol and Layout in Cadence Virtuoso for Full Adder

Date of Performing Experiment: 29th October 2019

Due Date: 5th November 2019

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# Objective:

To create schematic, symbol and layout in Cadence Virtuoso for Full Adder using Half Adders and the OR gate. So first objective is to create schematic, symbol and layout for OR gate and utilize the previously created Half Adder module to design the Full Adder.

# Theory:

Full Adder takes into consideration the previous carry. So there are 3 inputs and 2 outputs.

For creating a Full Adder in CMOS logic, 2 XOR gate generates the SUM output and the 2 AND gates plus 1 OR gate is used to generate the CARRY output. Hence, we can first create sub-circuit of XOR gate, AND gate and the OR gate and use it to design Full Adder.

Alternatively, we can create sub-circuit of half adder and use two half adders to implement the full adder. I have used the first method to implement the Full adder.

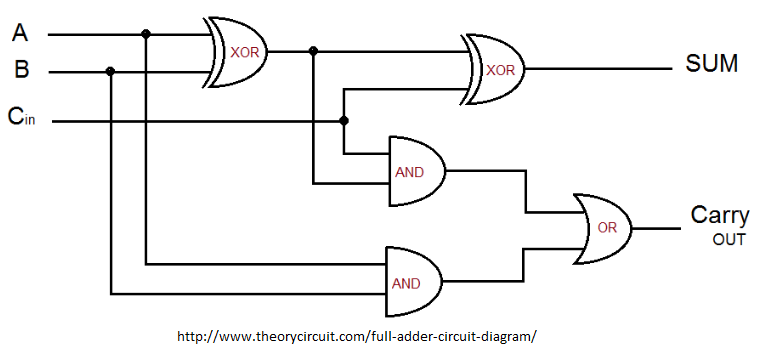
The Full adder has only 3 inputs. One of the input is carry from previous state. It adds the current inputs with the previous carry.

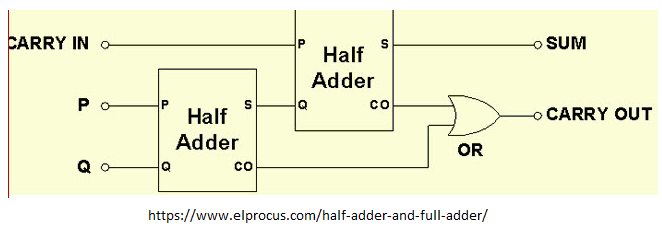
Truth Table:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | Cin | Sum | Carry |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

Equations:

Circuit implementation:





# Procedure for Creating Schematic and Symbol:

1. Open Virtuoso as per earlier tutorial. Open MobaXterm, new TUX cluster window. Type password.

ls

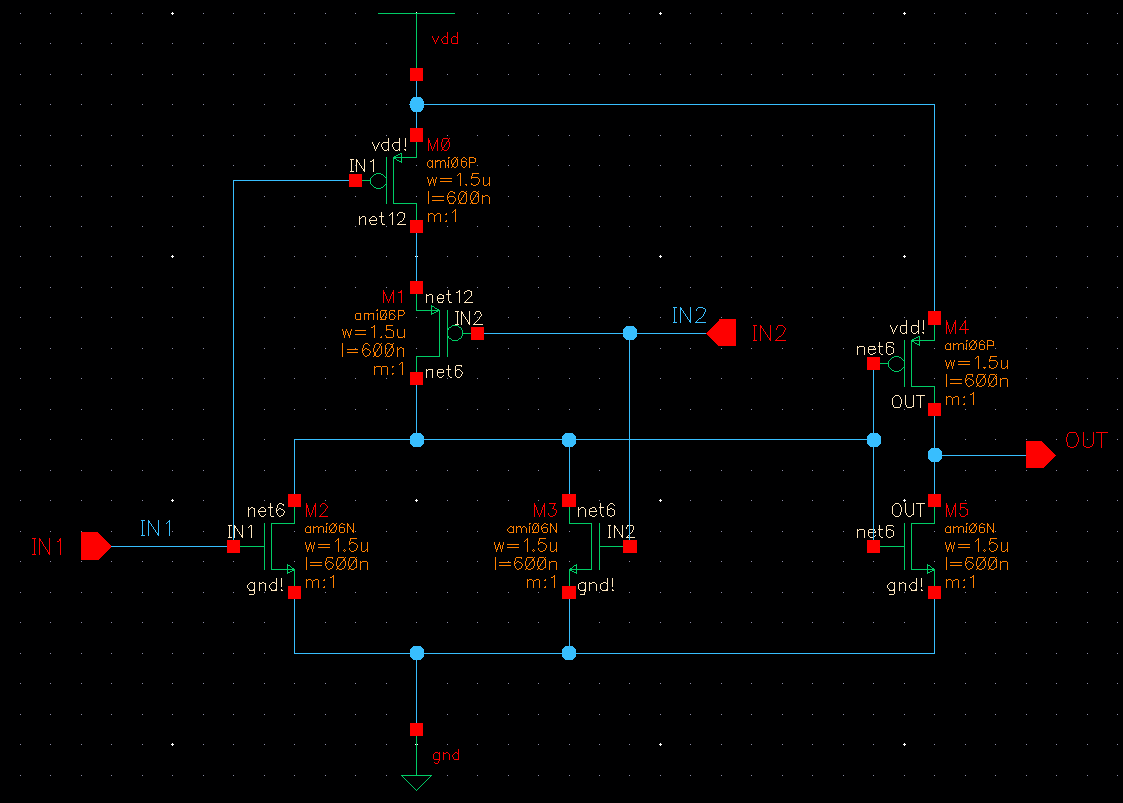
CadenceSetup(Enter)

CDKSetup(Enter)

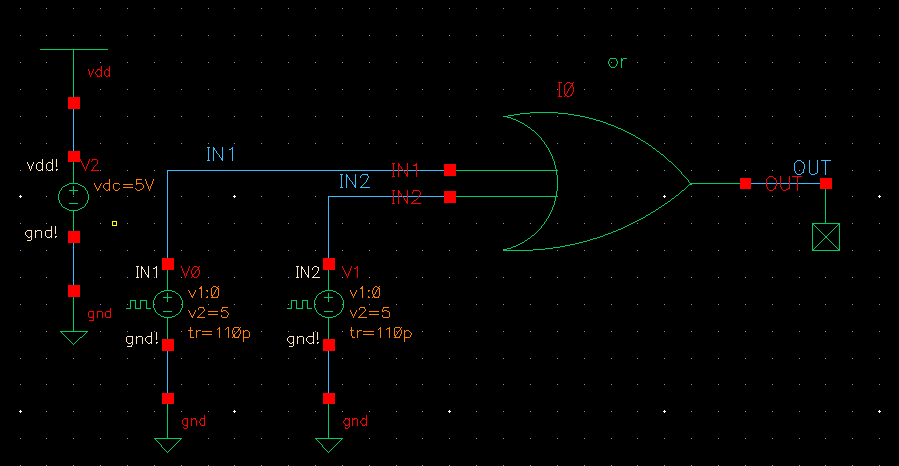
Cd cadence6

Virtuoso &

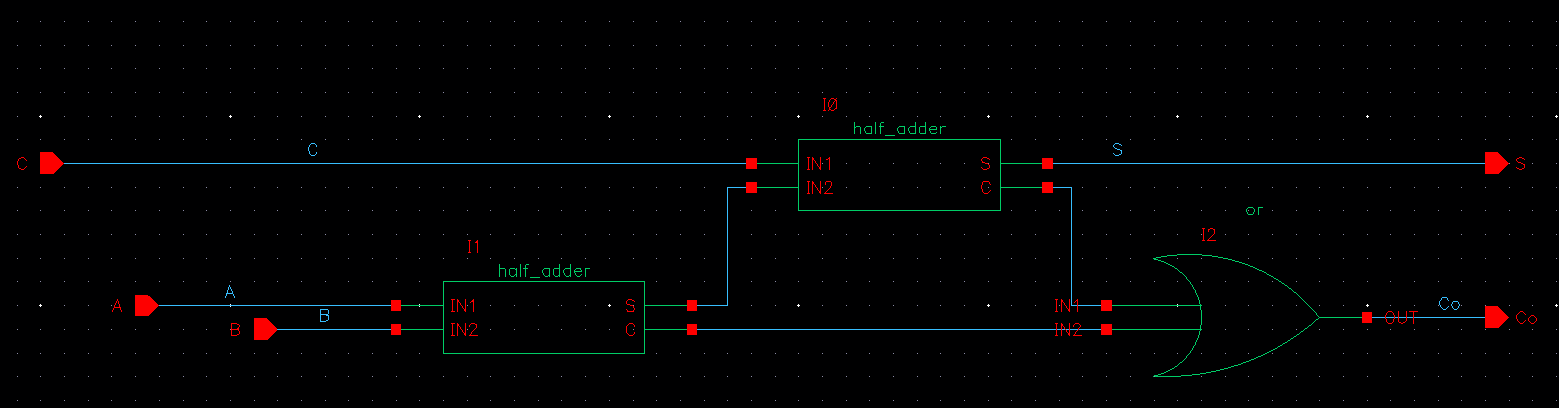
1. Select the created library in 1st tutorial. First create the OR gate.
2. Go in File🡪 New🡪 Cellview🡪 Name the schematic as “or”
3. Create the schematic for OR gate by re-using the NOR gate created earlier. Open the NOR gate schematic and copy paste the schematic into OR schematic. Add a NMOS and PMOS to create an inverter.
4. Simulate the circuit to check if it’s working.
5. Now, Delete the VDD, GND, the two Vpulse signals and 5V voltage source.
6. Click on Create 🡪 Pin. And pins to the input and output.



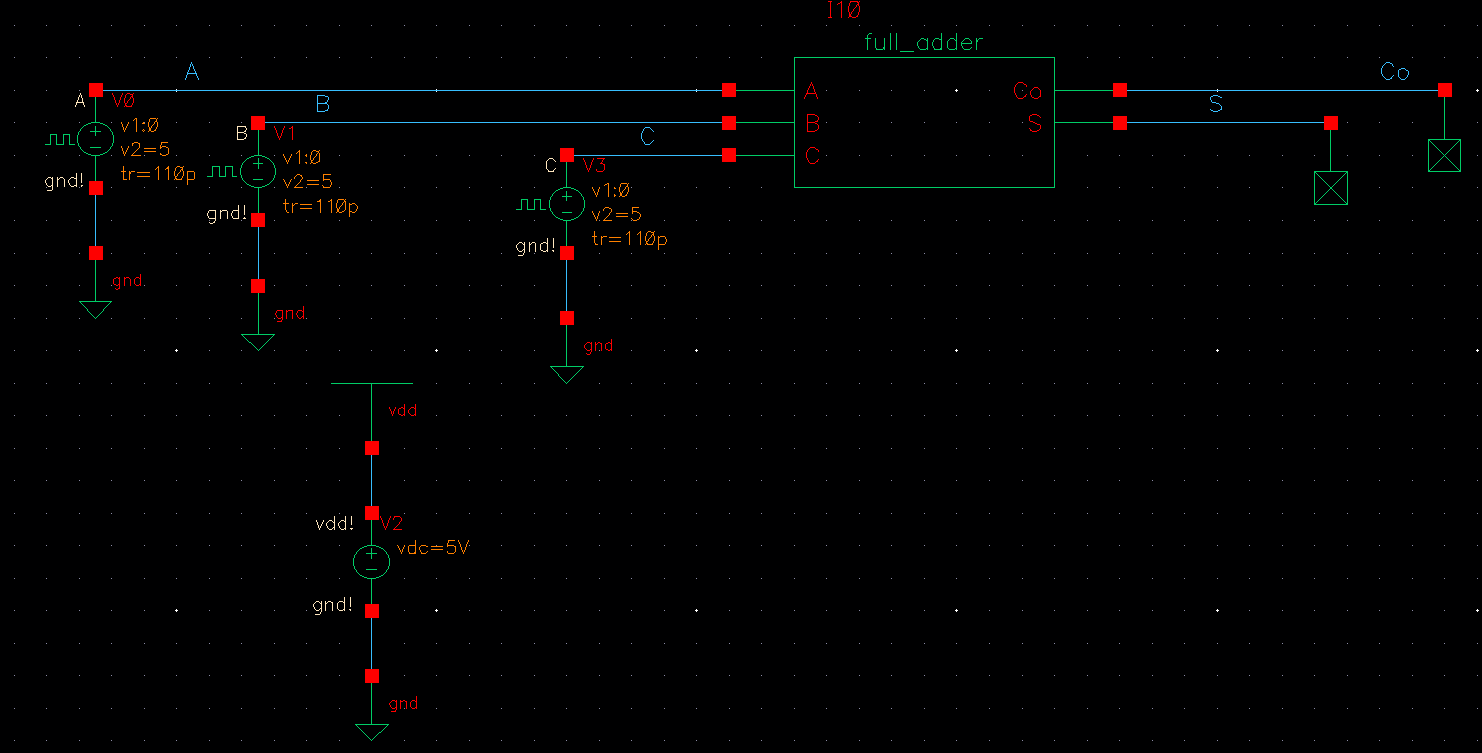
1. Click on Create 🡪 Cellview🡪 from Cellview. Create a symbol and simulate the schematic of symbol to verify its truth table by Launch🡪 ADE L.



1. Now create a new schematic by File🡪 New🡪 Cellview. Name it “full\_adder”. Go in Create🡪 Instance🡪 select your created library. It will show the symbols that have been created in previous tutorials.
2. Place two Half Adders symbols and the OR gate symbol. Connect the input outputs to get a Full Adder with Sum and Carry outputs.
3. Simulate it to check the output. Then remove the sources and place the input/output Pins in schematic.

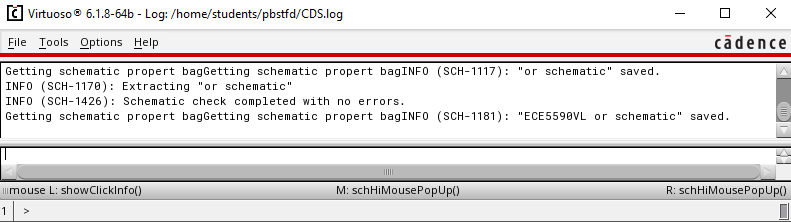


1. Now create the symbol for Full Adder by Create 🡪 Cellview🡪 from Cellview. Save it.
2. Open a new schematic window and create a schematic using the Full Adder symbol. Simulate it to verify the output.

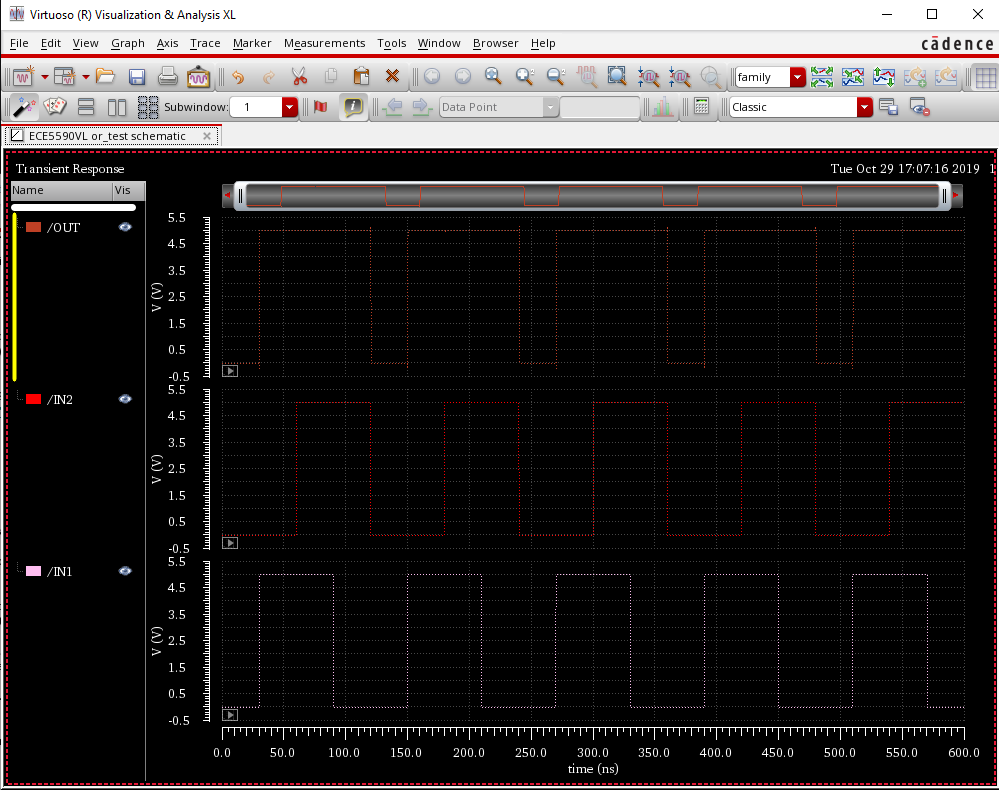


# Tables/Graphs for Full Adder Schematic and Symbol:

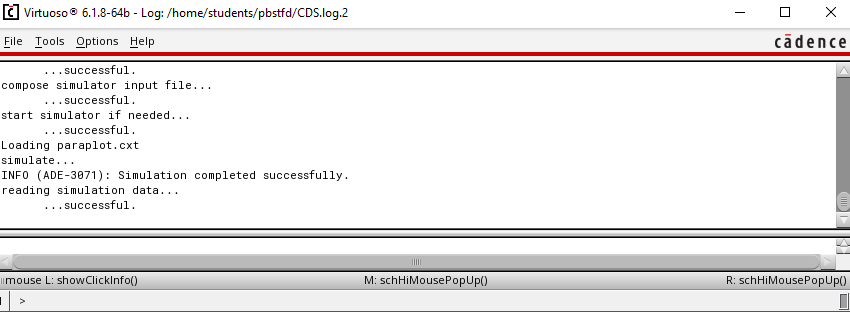
1. Log of Schematic for **OR** gate



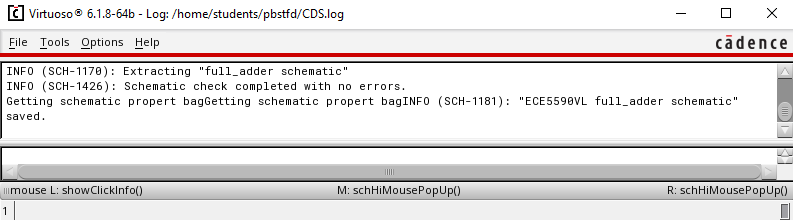
1. Simulation using **OR** symbol



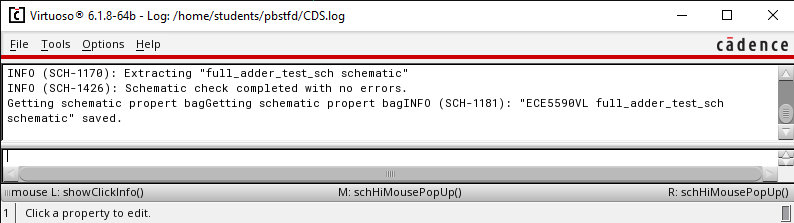
1. Simulation log **OR**



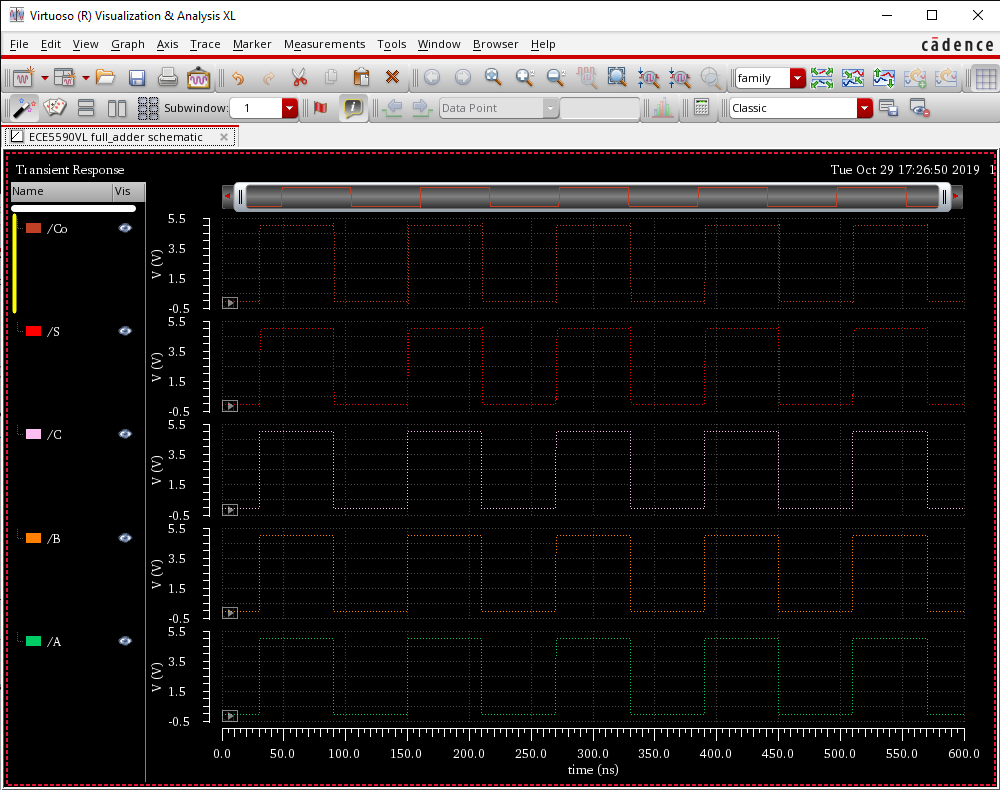
1. Log of Schematic for **Full Adder**

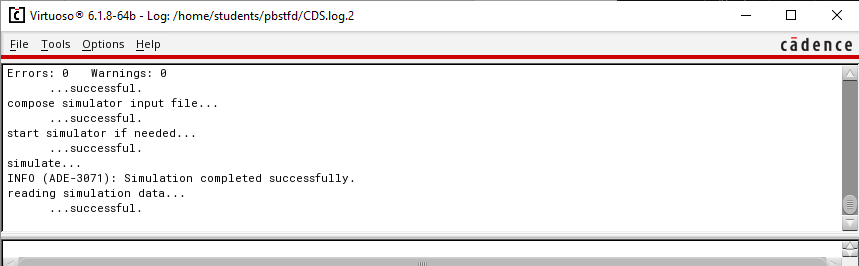


1. Log of Schematic test circuit for **Full Adder**



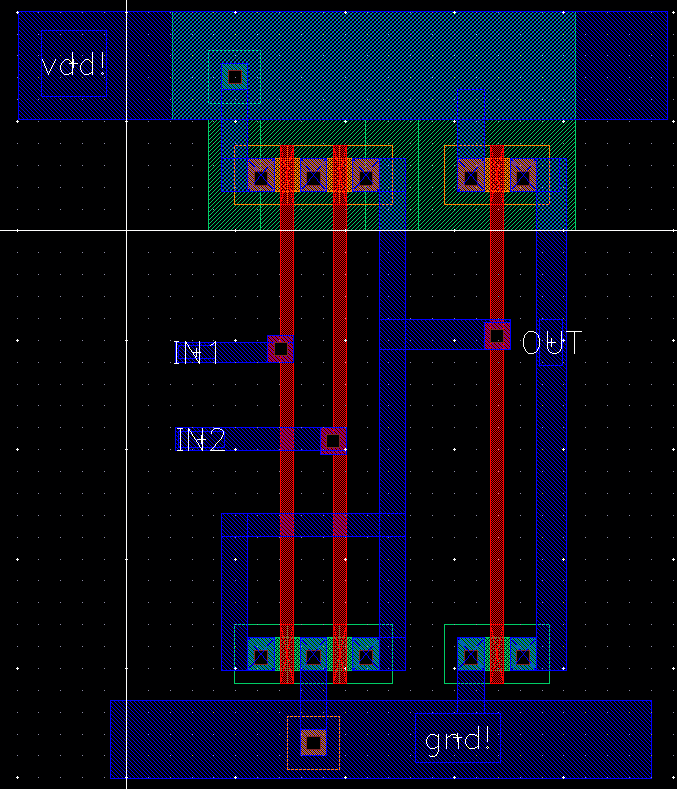
1. Simulation of **Full Adder**



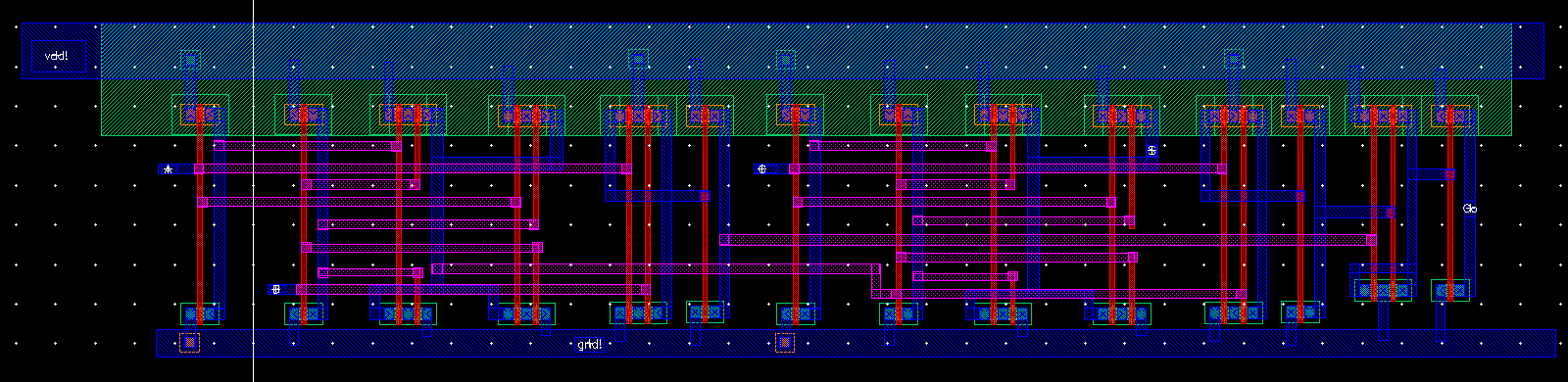


# Procedure for Creating Full Adder Layout:

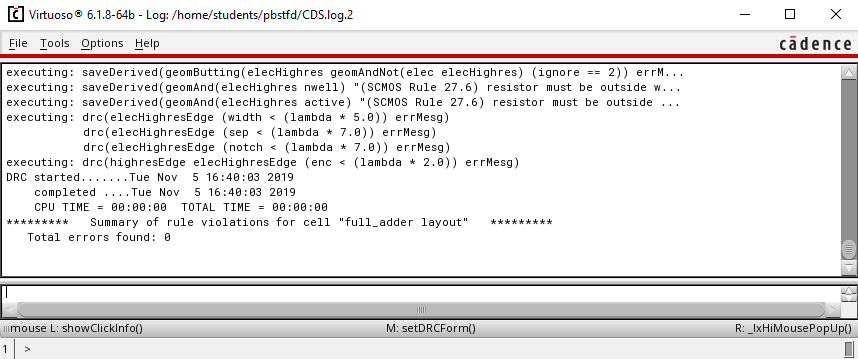
1. First create layout for **OR** gate.
2. In CIW window, in File🡪 New🡪 cellview🡪 give cell name same as that was given for the schematic and symbol, “or” and select the layout option in application.
3. Open the “nor” layout and copy paste the entire layout in “or” layout file.
4. We have to add an inverter ahead of NOR gate.
5. Go in Create🡪 Instance and in NSCU\_TechLib\_ami06, add the PMOS and NMOS transistors with the properties same as the instances in schematic.
6. Press Shift + f for viewing the layout of the instances.
7. Use “metal1” to connect the wires and “poly” to connect the polysilicon gates. These options are available in “Layer” tab at the left side of screen.
8. Extend the VDD and GND metals. Extend the n-well to connect it to VDD.
9. To connect different layers, go in Create🡪 Via. Use “M1\_Poly” to connect Poly with Metal, “M1\_N” to connect N-well to VDD and “M1\_P” to connect GND.
10. Change the output pin at the output of inverter.
11. Layout must look as below:



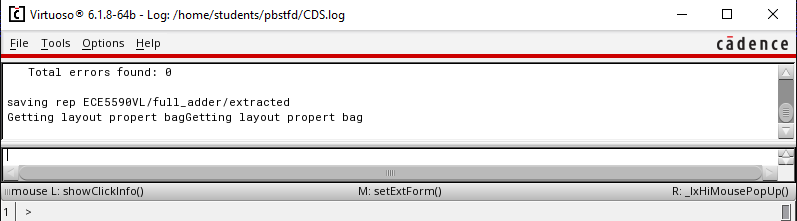
1. Simulate it with extracted environment. Verify the LVS check to match the schematic with the layout. Results are in Graphs section.
2. After verifying layout of OR gate, proceed for the Full Adder layout.
3. Copy the layout of Half Adder and the OR gate in the layout window “full\_adder”.
4. Use Metal2 layer to connect horizontally like in XOR gate layout. Use Via “M1\_M2” overlapped with “M1\_Poly” to connect to connect Metal2 with Poly.
5. Now, select metal1 and go in Create🡪 Pin and as per below image, create pin for vdd! gnd! and A, B, C, S and Co. Select I/O type as “output” for the OUT pin. Place the pins on the layout at appropriate locations.
6. Adjust the layout so as to have common n-well, VDD and GND.
7. The layout should look as below.



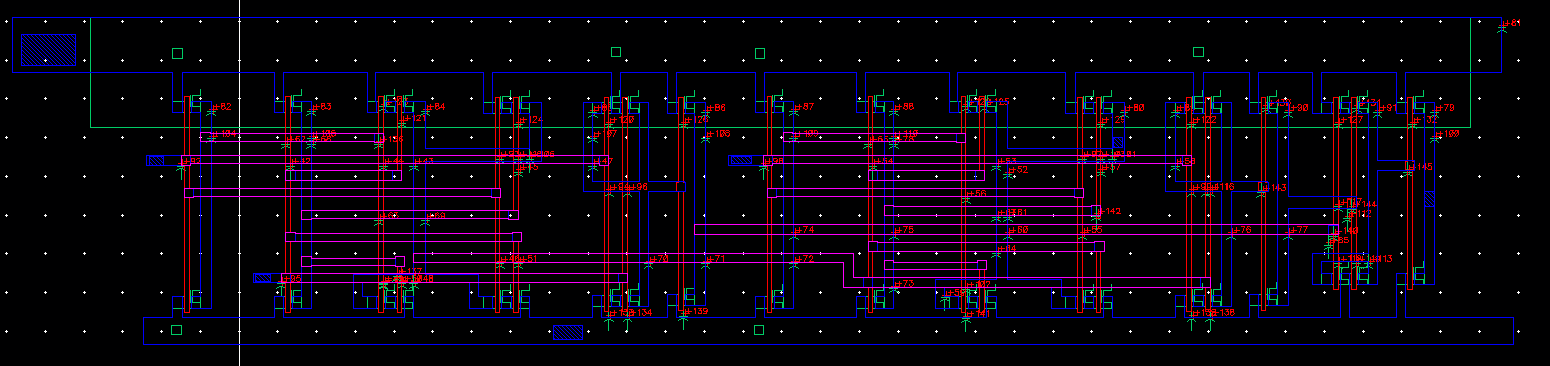
1. Go in Verify🡪 DRC to check if any errors. Errors will be shown by white lines. Correct them and again verify using DRC check. Following window must show 0 errors.



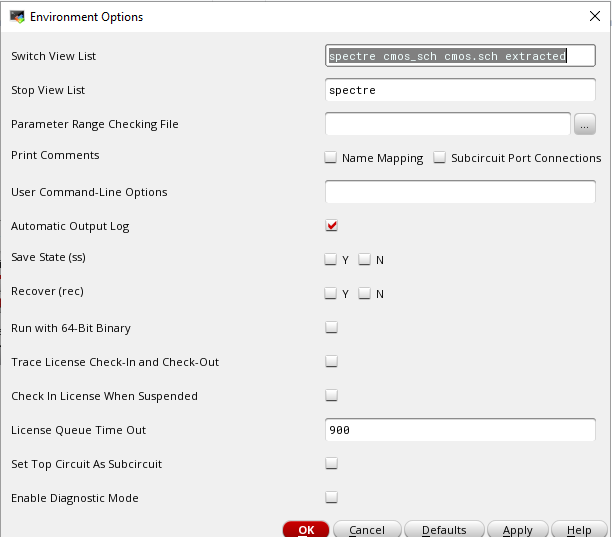
1. Then click on the Verify🡪 Extract and check if field are as per below image. Click Set Switches and select the “Extract\_parasitic\_caps” option. Click on “OK”
2. After extraction, errors shown must be 0. “full\_adder” extracted view must be saved.



1. Save design and close all other window except CIW and library manager. In library manager window, click on “full\_adder” and you must see all 3 files: schematic, layout and symbol.
2. Open the extracted file to view the capacitances.



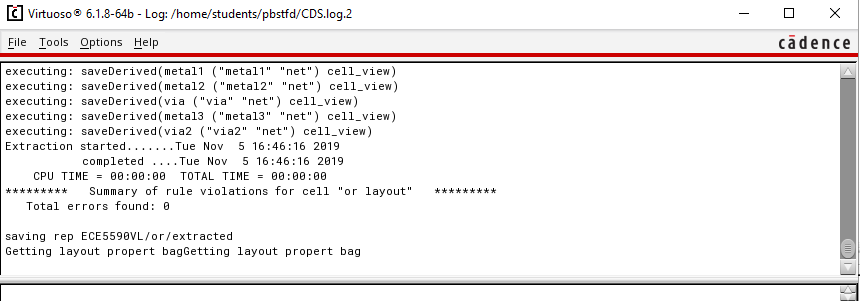
1. Open the file to simulate the symbol along with layout.
2. Go in Launch🡪 ADE l and follow the procedure done for schematic simulation with one additional step.
3. Go in Setup🡪Environment and change “schematic veriloga” to “extracted”.



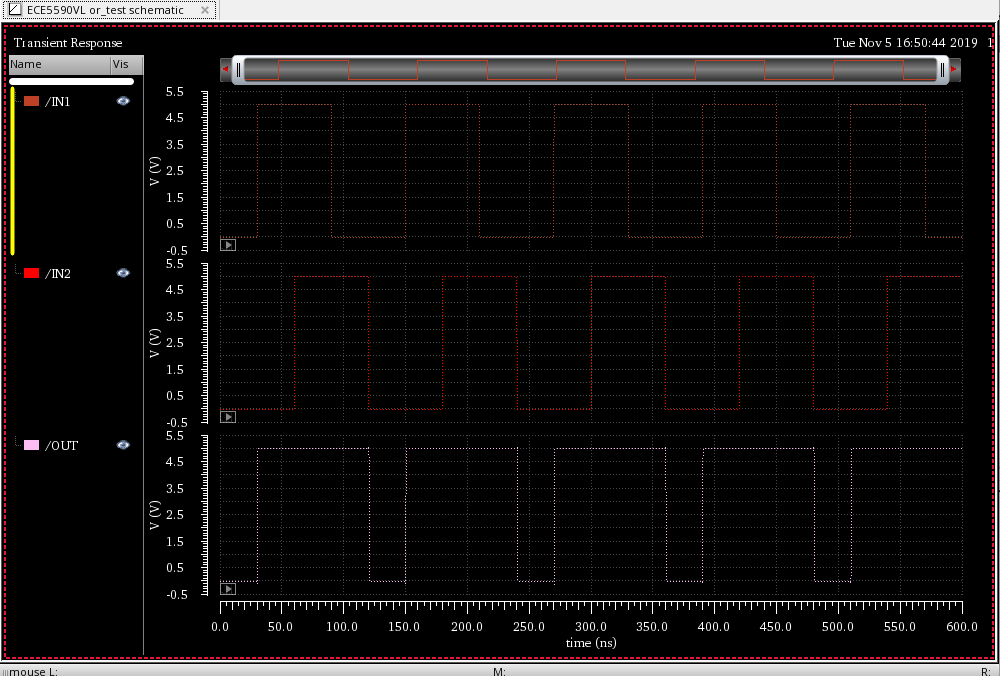
1. Run Simulation and capture waveform. CIW window must show successful simulation.
2. Verify the LVS check to match the schematic and layout.

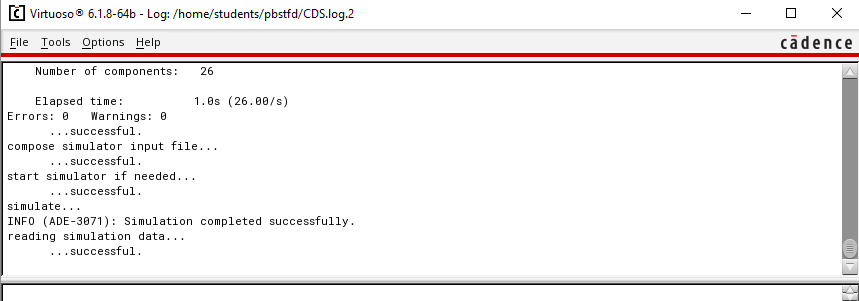
# Tables/Graphs for Full\_Adder Layout:

1. DRC Check for Layout and extracted layout saved for **OR** gate.

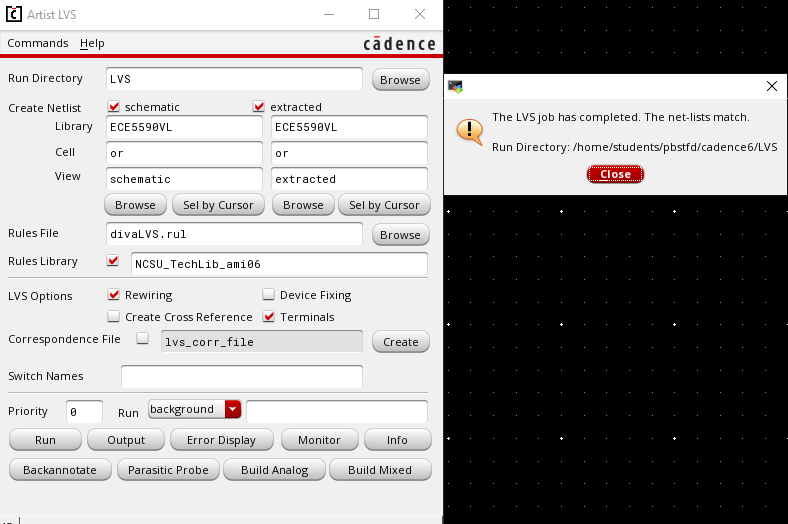


1. Simulation of Layout **OR**:

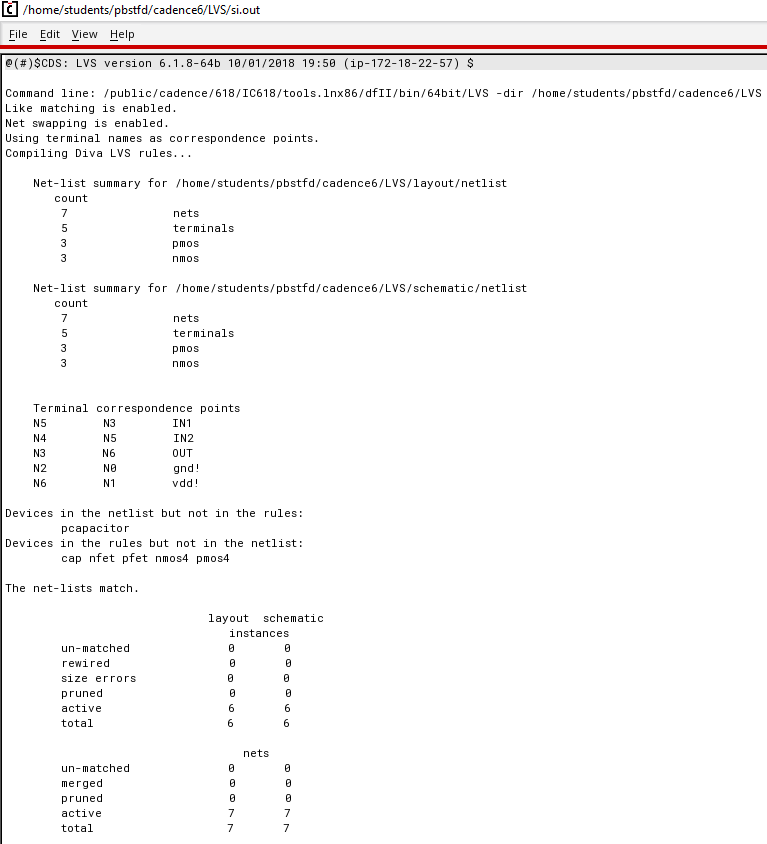




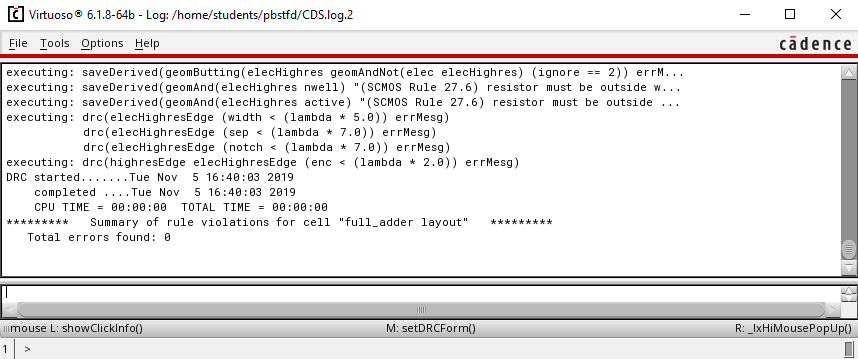
1. LVS Job done **OR**:



1. LVS Output **OR**:

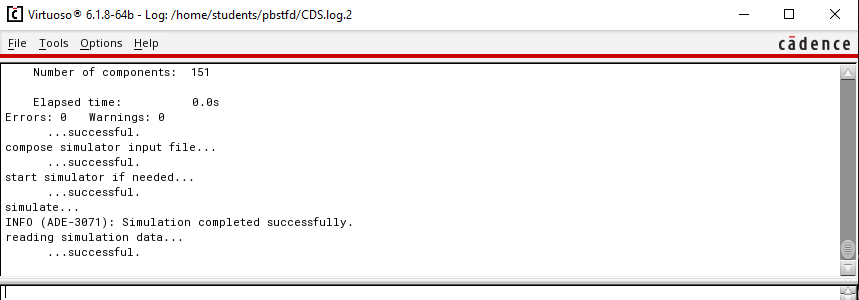


1. DRC Check for **Full Adder**

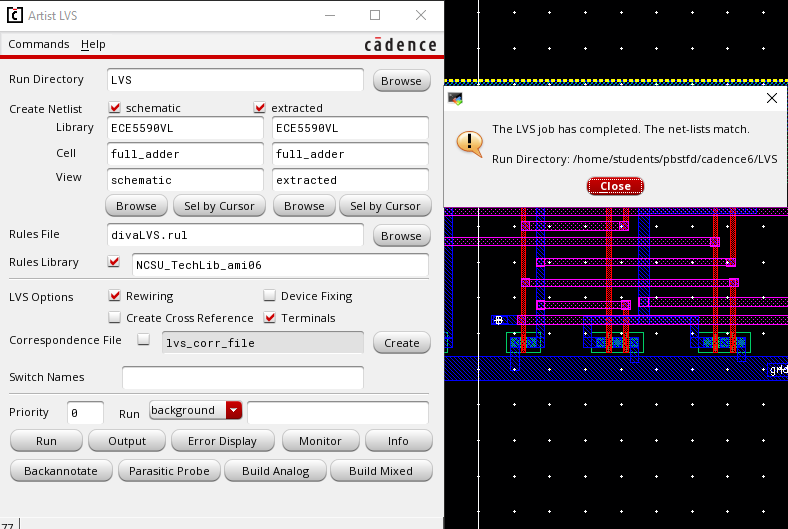


1. Simulation **Full Adder**

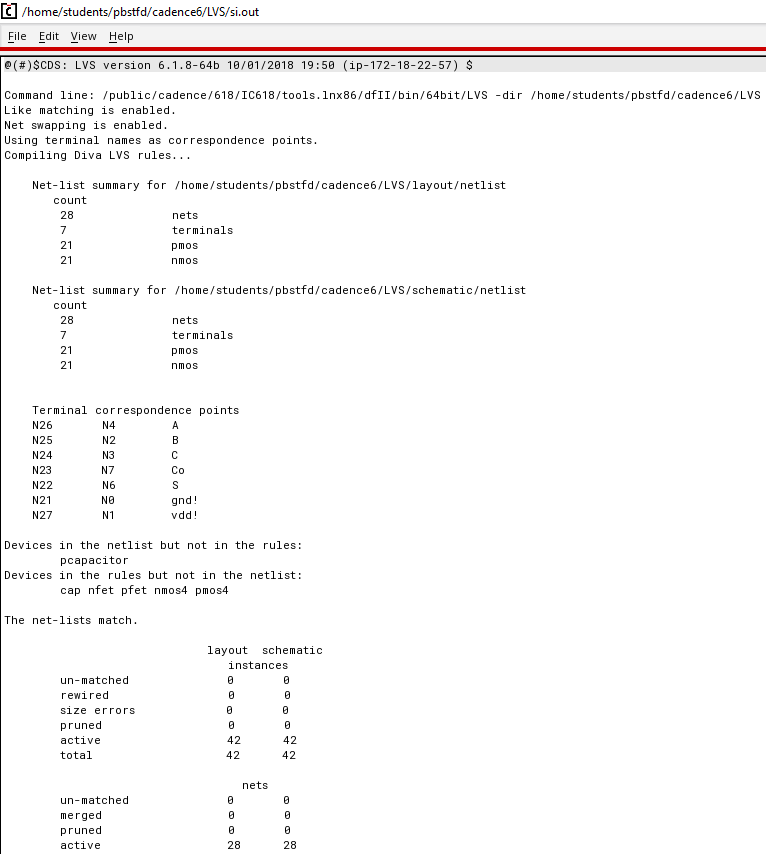




1. LVS job done for **Full Adder**



1. LVS output **Full Adder**



# Discussion of Result:

The waveforms of simulations of OR gate and Full Adder match with the truth table for all the combinations. Also, the layout works perfectly after changing simulation environment to “extracted”. Initially the LVS check was showing mismatch with extra net in the layout. The “via” for one of the poly and metal2 was wrong. After correcting it, the LVS check matched.

# Conclusion:

In this lab session we learned how to re-use the schematic and layout to create schematic and layout of a module. Full Adder is module comprises of two Half Adders and the OR gate. Hence, these two modules can be re-used to create Full Adder instead to building everything from scratch. Layout was complicated due to two half adders.