Course Number: EC-ENGR 5590VL-0001 Special Topics in ECE

Tutorial: 5

(Lab report + Homework)

**TITLE**

Schematic, Symbol and Layout in Cadence Virtuoso for Half Adder

Date of Performing Experiment: 8th October 2019

Due Date: 15th October 2019

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# Objective:

To create schematic, symbol and layout in Cadence Virtuoso for Half Adder using XOR and the AND gate. So first objective is to create schematic, symbol and layout for AND gate and utilize the previously created XOR gate to design the Half Adder.

# Theory:

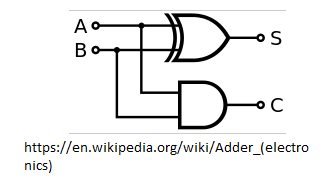
The half adder has only two inputs. It adds the current inputs only without considering the previous carry. The SUM is basically the “XOR” function of the two inputs and Carry is the “AND” function of the two inputs.

Truth Table:

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | Sum | Carry |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

Equations:

The Half Adder can be implemented as below:



# Procedure for Creating Schematic and Symbol:

1. Open Virtuoso as per earlier tutorial. Open MobaXterm, new TUX cluster window. Type password.

ls

CadenceSetup(Enter)

CDKSetup(Enter)

Cd cadence6

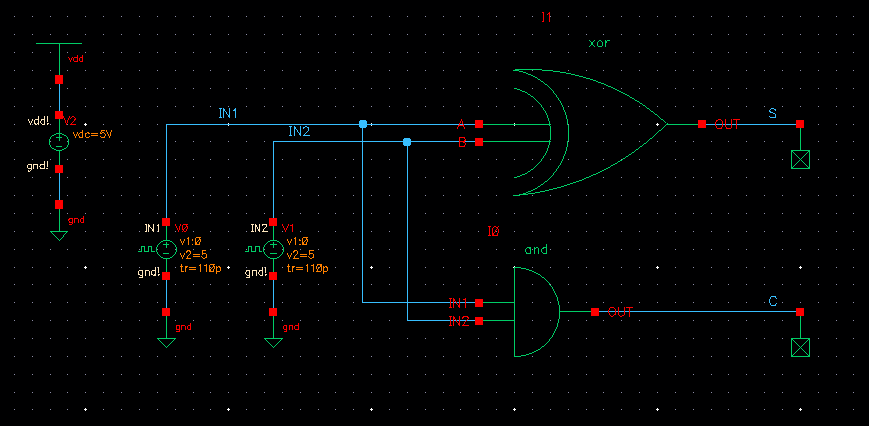
Virtuoso &

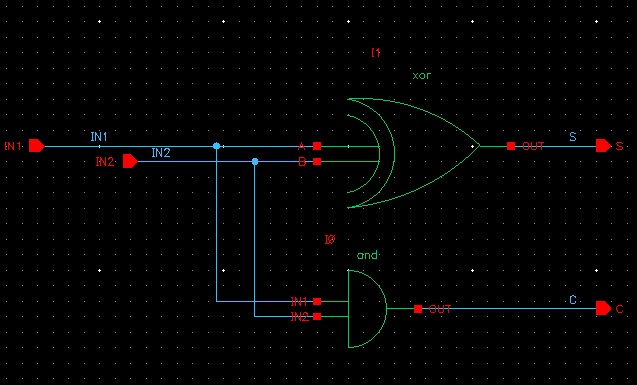
1. Select the created library in 1st tutorial. First create AND gate.
2. Go in File🡪 New🡪 Cellview🡪 Name the schematic as “and”
3. Create the schematic for AND gate by re-using the NAND gate created earlier. Open the NAND gate schematic and copy paste the schematic into AND schematic. Add a NMOS and PMOS to create an inverter.
4. Simulate the circuit to check if it’s working.
5. Now, Delete the VDD, GND, the two Vpulse signals and 5V voltage source.
6. Click on Create 🡪 Pin. And pins to the input and output.

A close up of a red light at night

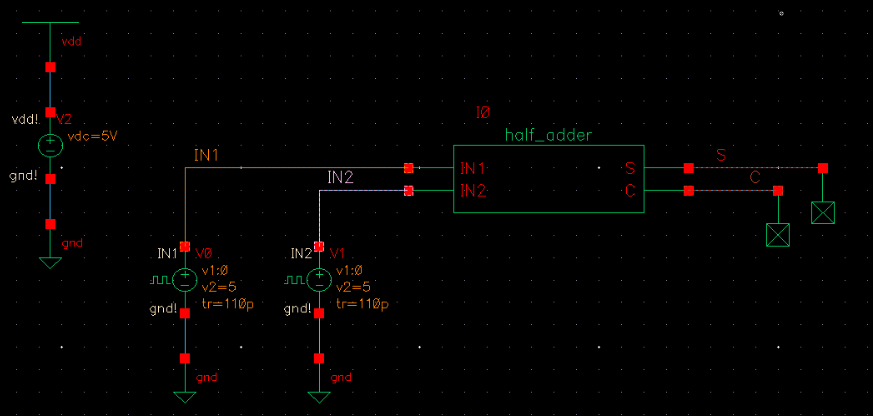
Description automatically generated

1. Click on Create 🡪 Cellview🡪 from Cellview. Create a symbol and simulate the schematic of symbol to verify its truth table by Launch🡪 ADE L.
2. Now create a new schematic by File🡪 New🡪 Cellview. Name it “half\_adder”. Go in Create🡪 Instance🡪 select your created library. It will show the symbols that have been created in previous tutorials.
3. Place the XOR gate symbol and the AND gate symbol. Connect the input outputs to get an Half Adder with Sum and Carry outputs.
4. Simulate it to check the output. Then remove the sources and place the input/output Pins in schematic.



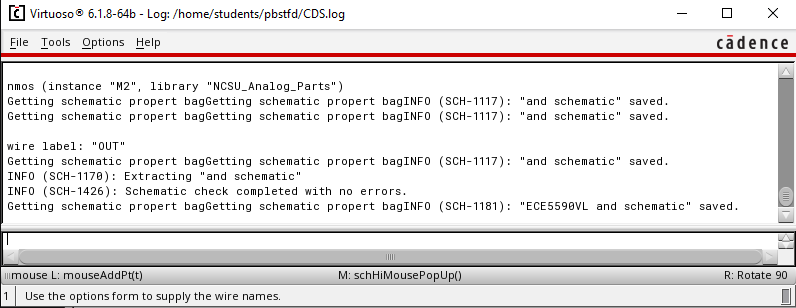


1. Now create the symbol for Half Adder by Create 🡪 Cellview🡪 from Cellview. Save it.
2. Open a new schematic window and create a schematic using the Half Adder symbol. Simulate it to verify the output.

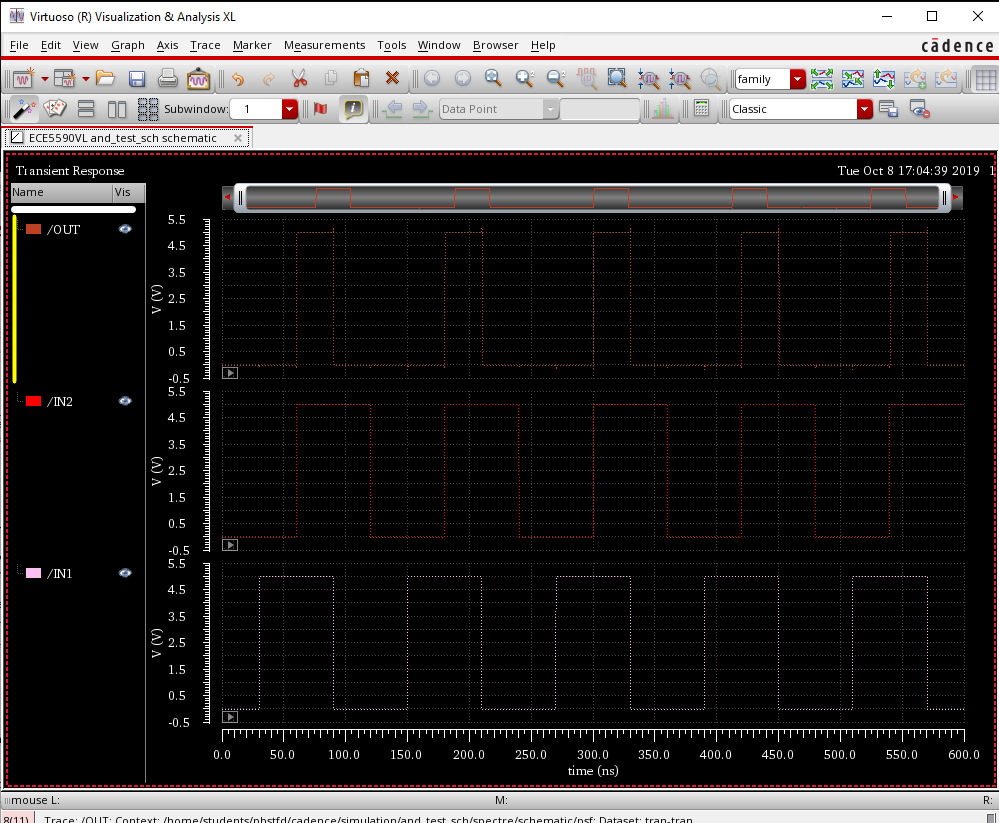


# Tables/Graphs for Half Adder Schematic and Symbol:

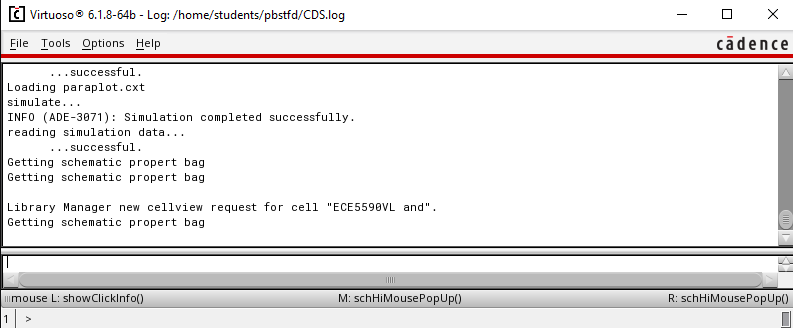
1. Log of Schematic for **AND** gate



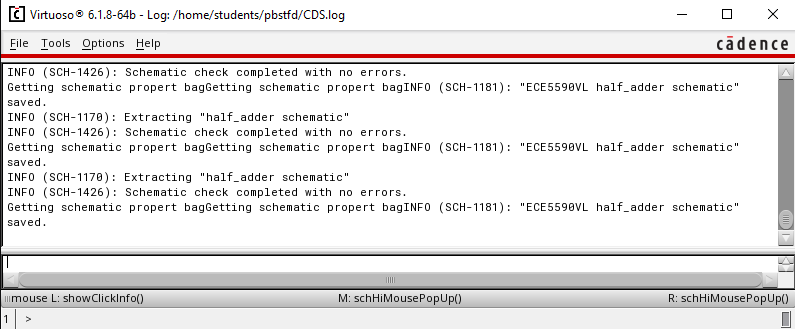
1. Simulation using **AND** symbol



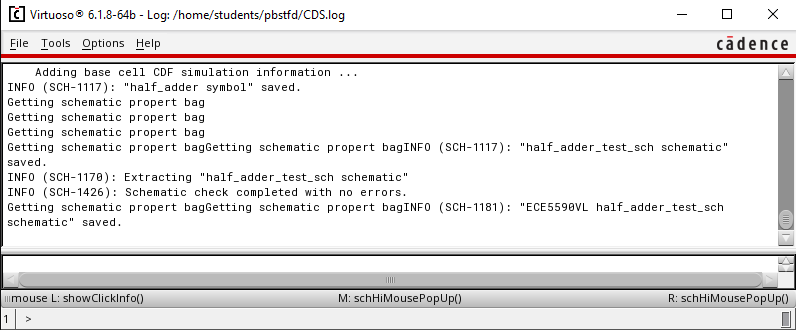
1. Simulation log **AND**



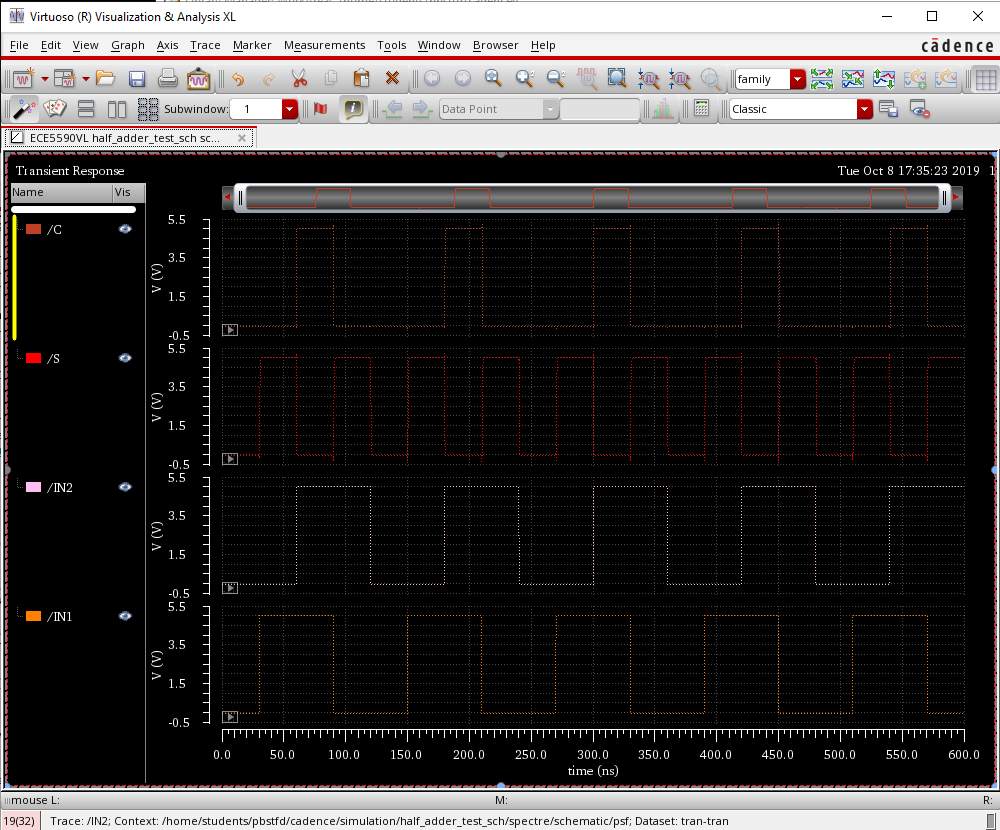
1. Log of Schematic for **Half Adder**

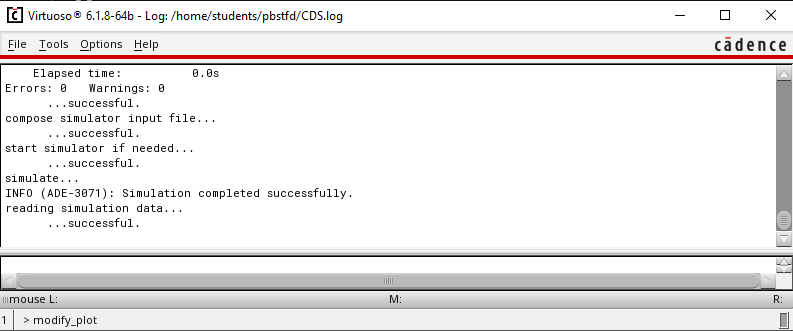


1. Log of Schematic test circuit for **Half Adder**



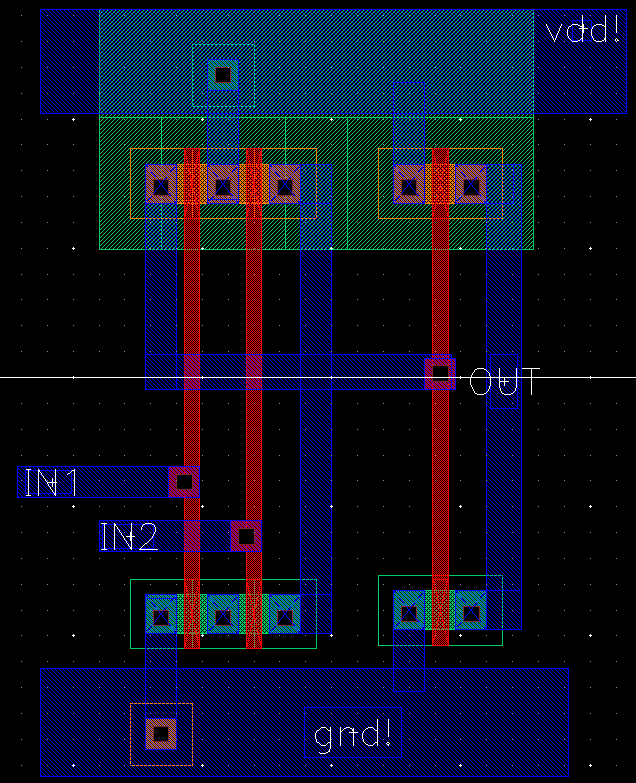
1. Simulation of **Half Adder**



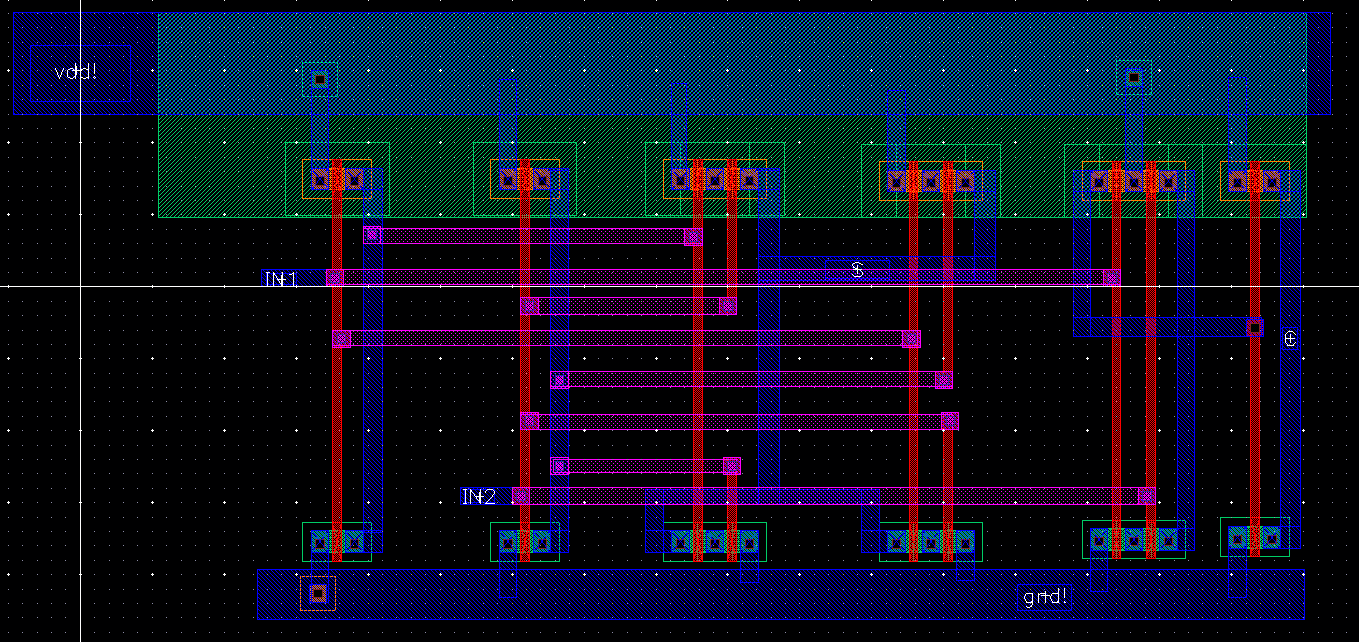


# Procedure for Creating Half Adder Layout:

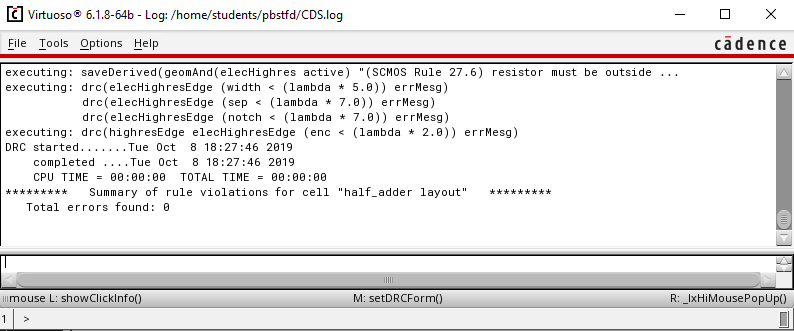
1. First create layout for **AND** gate.
2. In CIW window, in File🡪 New🡪 cellview🡪 give cell name same as that was given for the schematic and symbol, “and” and select the layout option in application.
3. Open the “nand” layout and copy paste the entire layout in “and” layout file.
4. We have to add an inverter ahead of NAND gate.
5. Go in Create🡪 Instance and in NSCU\_TechLib\_ami06, add the PMOS and NMOS transistors with the properties same as the instances in schematic.
6. Press Shift + f for viewing the layout of the instances.
7. Use “metal1” to connect the wires and “poly” to connect the polysilicon gates. These options are available in “Layer” tab at the left side of screen.
8. Extend the VDD and GND metals. Extend the n-well to connect it to VDD.
9. To connect different layers, go in Create🡪 Via. Use “M1\_Poly” to connect Poly with Metal, “M1\_N” to connect N-well to VDD and “M1\_P” to connect GND.
10. Change the output pin at the output of inverter.
11. Layout must look as below:



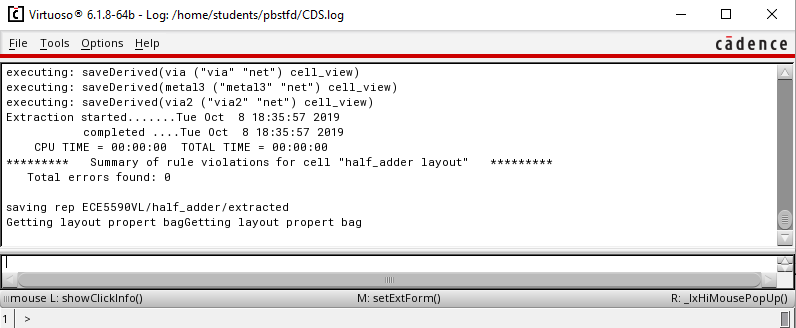
1. Simulate it with extracted environment. Verify the LVS check to match the schematic with the layout. Results are in Graphs section.
2. After verifying layout of AND gate, proceed for the Half Adder layout.
3. Copy the layout of XOR gate and the AND gate in the layout window “half\_adder”.
4. Use Metal2 layer to connect horizontally like in XOR gate layout. Use Via “M1\_M2” overlapped with “M1\_Poly” to connect to connect Metal2 with Poly.
5. Now, select metal1 and go in Create🡪 Pin and as per below image, create pin for vdd! gnd! and IN1, IN2, S and C. Select I/O type as “output” for the OUT pin. Place the pins on the layout at appropriate locations.
6. Adjust the layout so as to have common n-well , VDD and GND.
7. The layout should look as below.



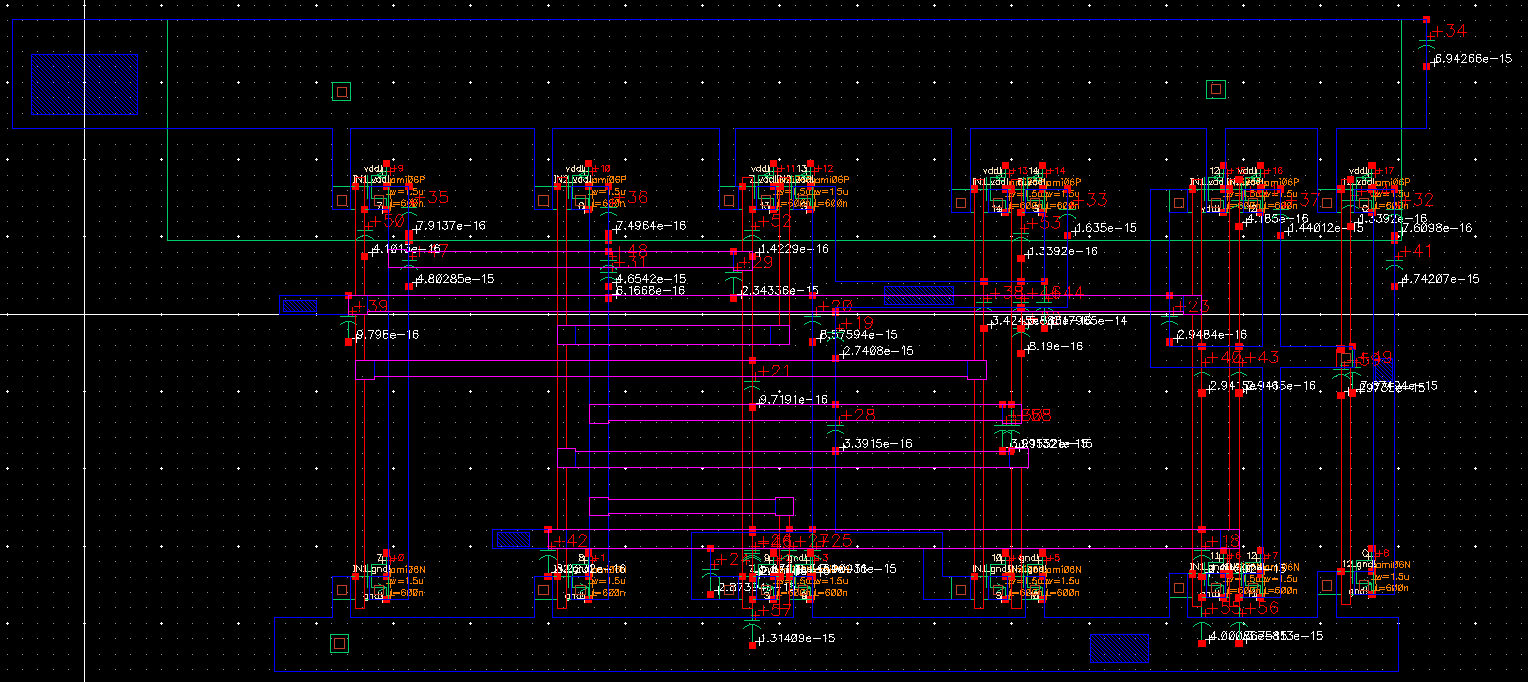
1. Go in Verify🡪 DRC to check if any errors. Errors will be shown by white lines. Correct them and again verify using DRC check. Following window must show 0 errors.



1. Then click on the Verify🡪 Extract and check if field are as per below image. Click Set Switches and select the “Extract\_parasitic\_caps” option. Click on “OK”
2. After extraction, errors shown must be 0. “Half\_adder” extracted view must be saved.



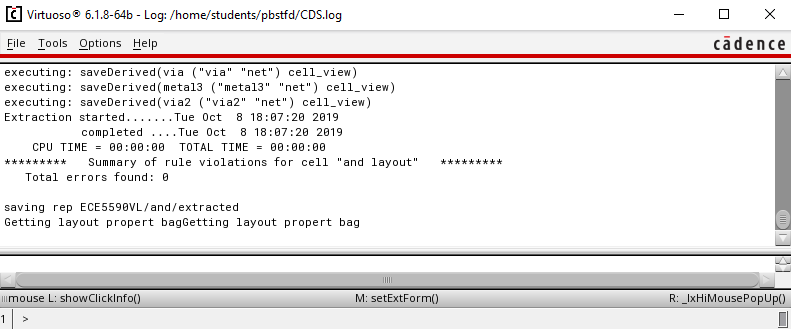
1. Save design and close all other window except CIW and library manager. In library manager window, click on “half\_adder” and you must see all 3 files: schematic, layout and symbol.
2. Open the extracted file to view the capacitances.



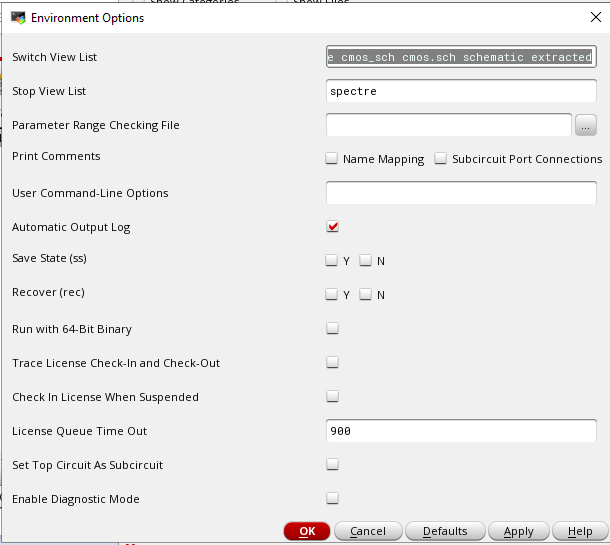
1. Open the file to simulate the symbol along with layout.
2. Go in Launch🡪 ADE l and follow the procedure done for schematic simulation with one additional step.
3. Go in Setup🡪Environment and change “veriloga” to “extracted”.
4. Run Simulation and capture waveform. CIW window must show successful simulation.
5. Verify the LVS check to match the schematic and layout.

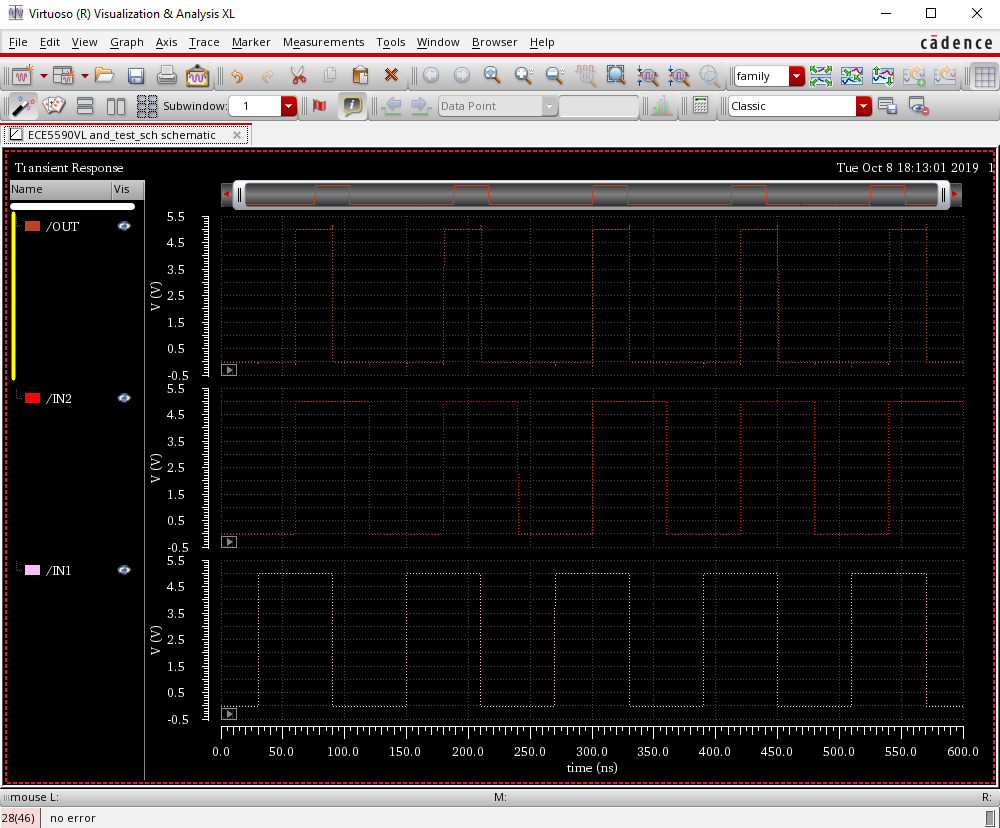
# Tables/Graphs for Half\_Adder Layout:

1. DRC Check for Layout and extracted layout saved for **AND** gate.

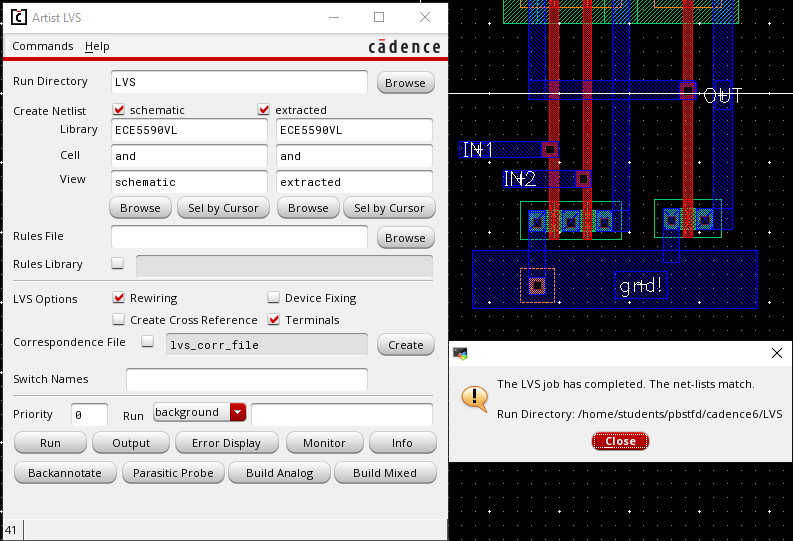


1. Simulation of Layout **AND**:

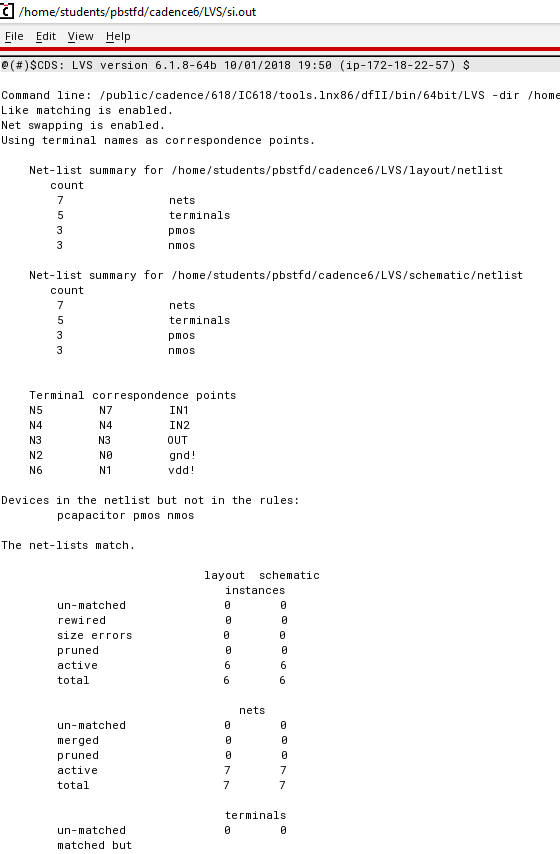




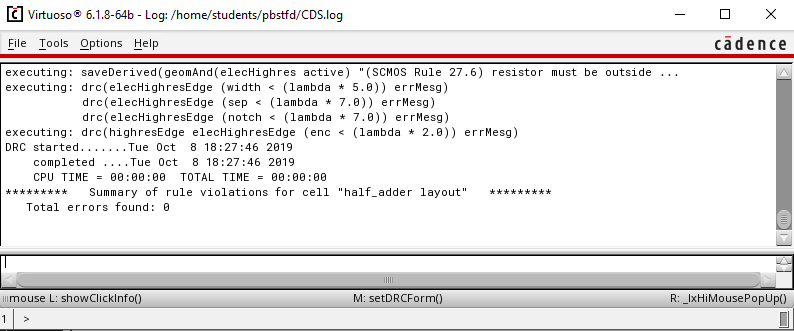
1. LVS Job done **AND**:



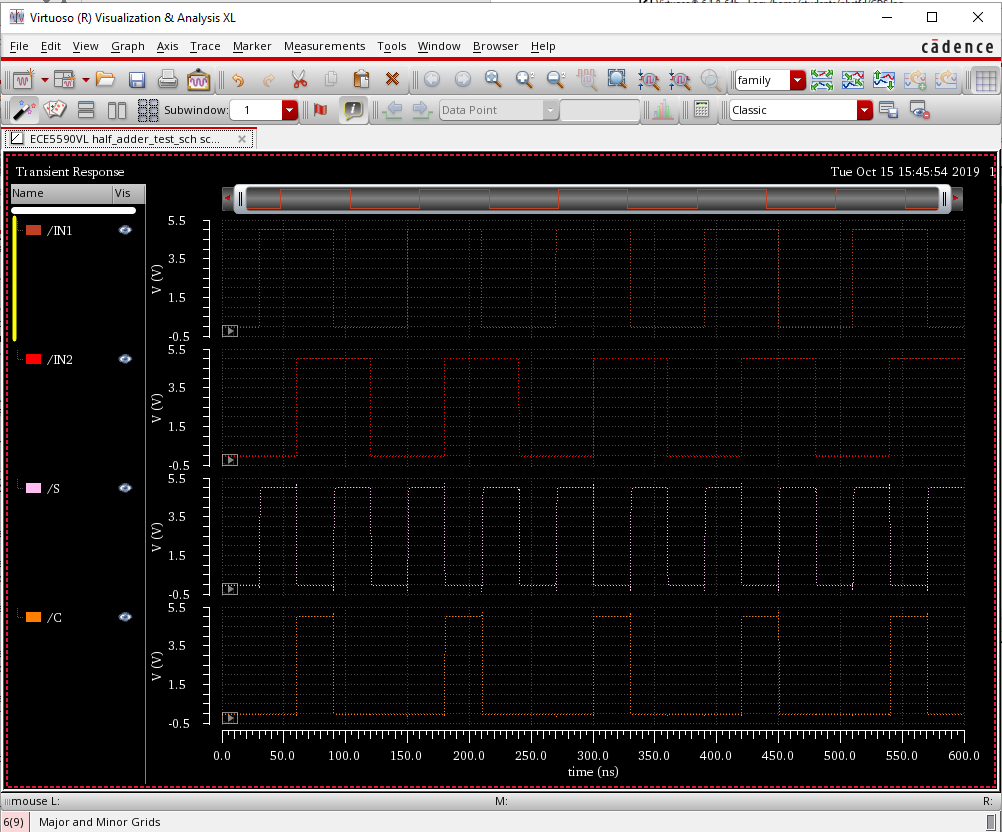
1. LVS Output **AND**:



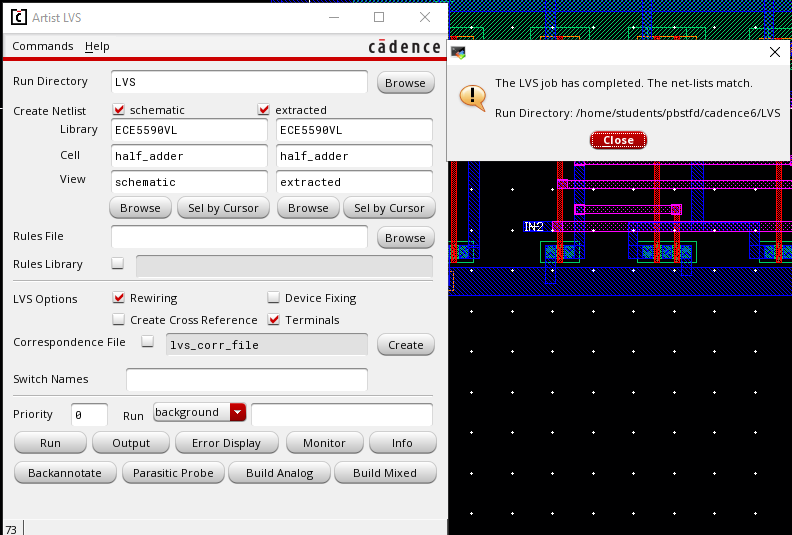
1. DRC Check for **Half Adder**



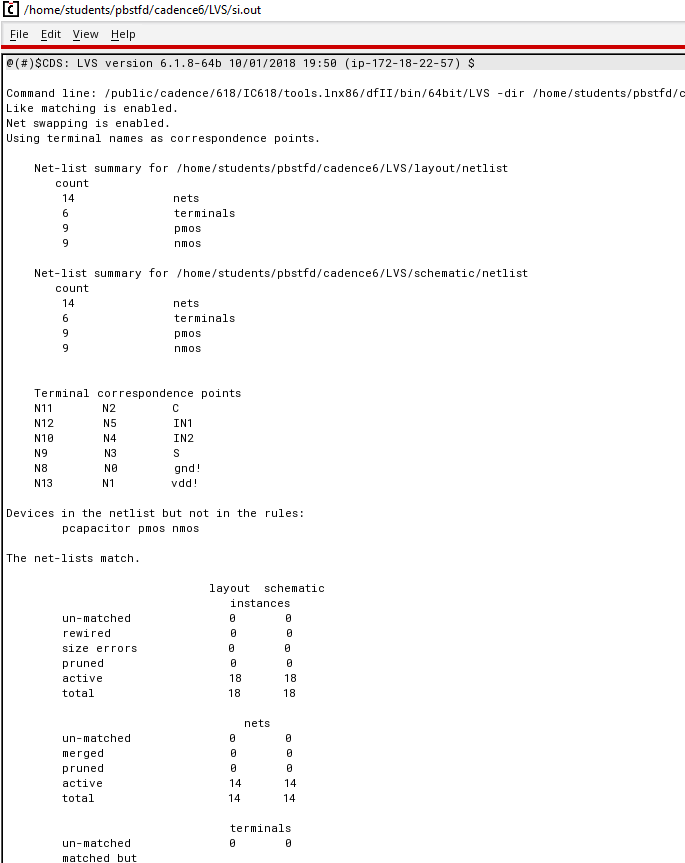
1. Simulation **Half Adder**



1. LVS job done for **Half Adder**



1. LVS output **Half Adder**



# Discussion of Result:

The waveforms of simulations of AND gate and Half Adder match with the truth table for all the combinations. Also, the layout works perfectly after changing simulation environment to “extracted”. Initially the LVS check for Half Adder was showing mismatch in schematic and layout. While copy pasting the XOR layout and the AND schematic, two separate N-well were created. This was creating problem. When the N-well was made common to all the PMOS transistors, the LVS showed the schematic and layout match.

# Conclusion:

In this lab session we learned how to re-use the schematic and layout to create schematic and layout of a module. Half Adder is module comprising of XOR gate and the AND gate. Hence, these two gates can be re-used to create Half Adder instead to building everything from scratch.