Course Number: EC-ENGR 5590VL-0001 Special Topics in ECE

Tutorial

Lab report

**TITLE**

Simulation using HSPICE for Half Adder gate using Sub-circuit

Date of Performing Experiment: 15th October 2019

Due Date: 22nd October 2019

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# Objective:

To run HSPICE on Linux platform, to create netlist and simulation of Half Adder gate using the sub-circuit approach.

# Theory:

In HSPICE we can re-use the circuits created earlier in simulating circuits of higher hierarchy. The circuits must be created as sub-circuits for its re-usability. This method is convenient to simulate large circuits. For creating a Half Adder in CMOS logic, XOR gate generates the SUM output and the AND gate is used to generate the CARRY output. Hence, we can first create sub-circuit of XOR gate and the AND gate and use it to design Half Adder.

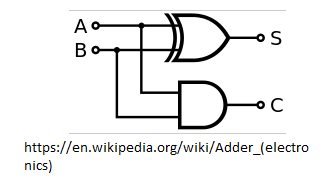
The half adder has only two inputs. It adds the current inputs only without considering the previous carry.

Truth Table:

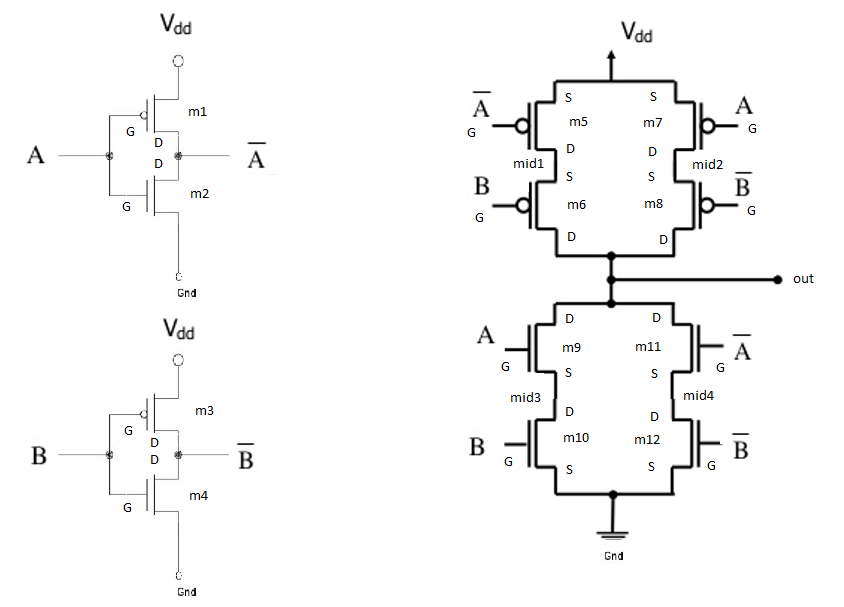
|  |  |  |  |
| --- | --- | --- | --- |
| A | B | Sum | Carry |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

Equations:

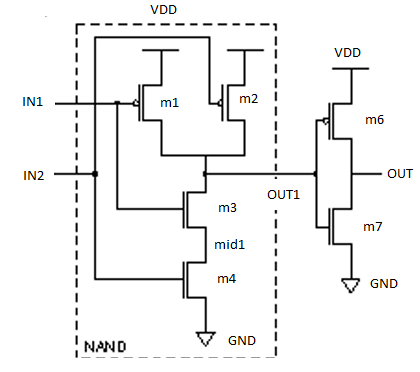
The Half Adder can be implemented as below:



# CMOS implementation: XOR gate



# CMOS implementation: AND gate



# Procedure to Simulate in HSPICE:

1. Start MobaXterm like previous tutorials. Open New Cluster and enter password.
2. Enter the directory hspice.
3. Type below commands:

Cd hspice

gedit &

1. We require the input netlist file in HSPICE and has to be created beforehand and saved at a location where HSPICE is installed. Hence gedit is used to write a netlist input.
2. Type the netlist for sub-circuits, AND gate and the XOR gate. For AND gate, use netlist of NAND gate and add an inverter at its output. Use the CMOS implemenations in the figures above to implement the netlist.
3. For creating XOR gate, there are 2 methods. Since, the XOR gates has inputs A and A\_bar, B and B\_bar, the inverted inputs can be generated by using sub-circuit of NOT gate or can be directly implemented in the XOR sub-circuit.
4. Define the voltage sources and nets for the main Half Adder block. Save it in the HSPICE folder by name “ha.sp”. Extension “sp” is for input netlist.
5. The MobaXterm will show some error but still the file gets saved. Close the TUX and Open a new TUX window. Enter password and directly type:

cd hspice

ls

Here you will find the file created.

1. The model files “ami06\_models.txt” are already in the folder.
2. To create an output listing, type below command:

hspice ha.sp > ha.lis

(inputfilename.sp > outputfilename.lis)

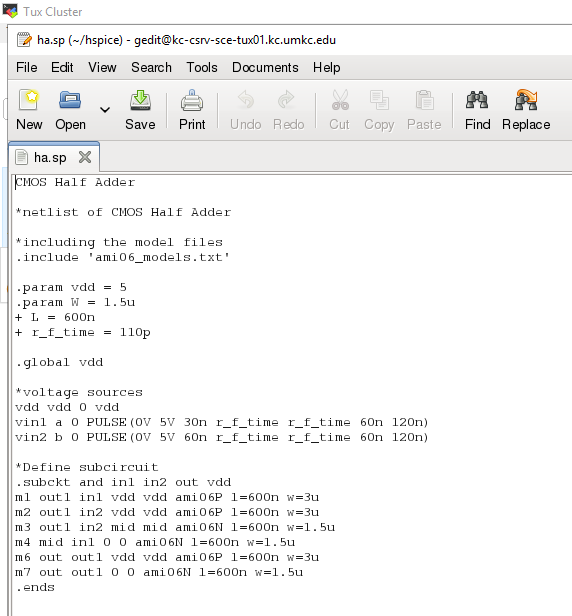
1. After this command you must get “hspice job concluded”. This means there are no errors. To check what errors are in the .sp file, open gedit🡪 open the .lis file
2. Now, simulate the netlist using CosmosScope. Type below command:

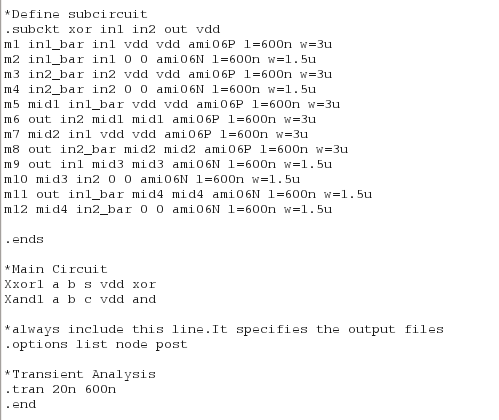
cscope &

1. The simulator window will open. Click on File🡪 Open🡪Plotfiles.
2. Open the “ha.tr” file. This file is the transient analysis graph data.
3. Select the inputs and outputs of main module V(a) and V(b) and click on Plot. Verify the graphs with truth table.

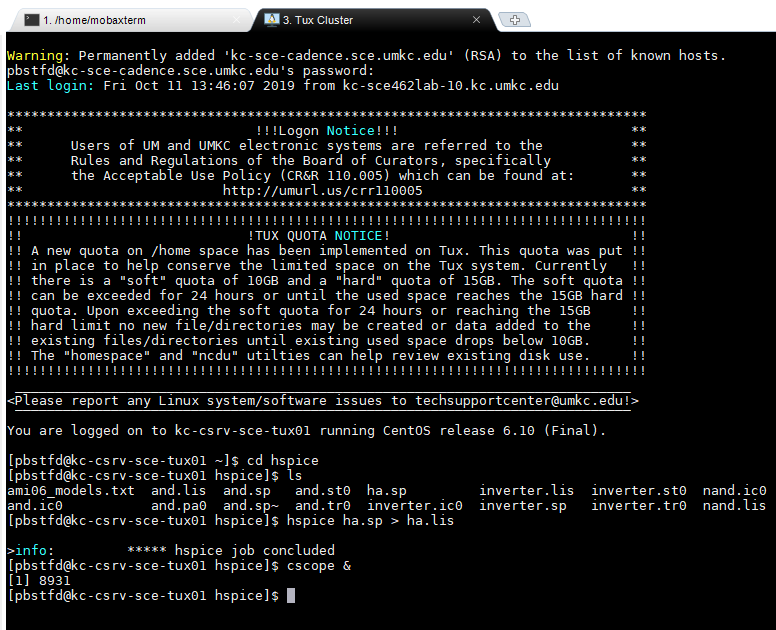
# Tables/Graphs for Half Adder Schematic

1. Gedit Code

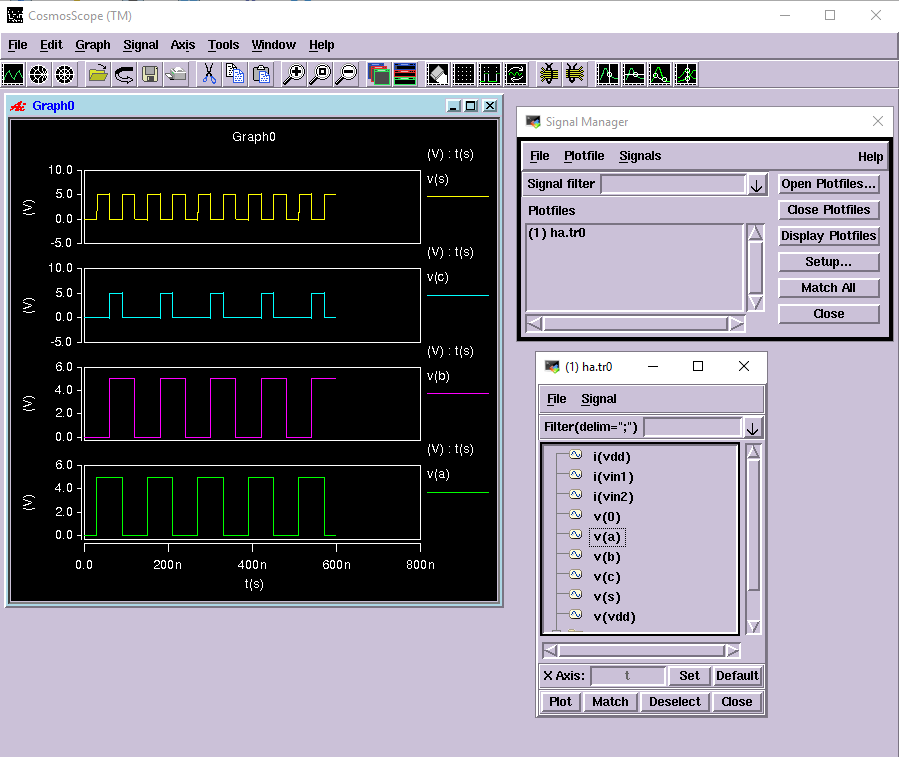




1. MobaXterm Job Done. Netlist successfully



1. CosmosScope output



# Discussion of Result

Half Adder Gate: The SUM is basically the XOR function of the two inputs. Carry is the AND function of the two inputs. In XOR, total 12 transistors are used and in the AND function, total 7 transistors are used.

# Conclusion

Through this lab tutorial we conclude that to implement a complicated circuit, we can break it down into smaller modules and use sub-circuit approach to build bigger modules. Half adder can be built using XOR and the AND sub-circuits. Total sub-circuits required are NAND, NOT and XOR.