Military Institute of Science and Technology

Department of Electrical, Electronics and Communication Engineering

Course Name: Communication Systems I Laboratory

Course code: EECE-310

Group - 07

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Phase Shift Keying Demodulation

1. Abstract

This project focuses on the design, simulation, and hardware implementation of a coherent Phase Shift Keying (PSK) demodulation circuit. PSK is a widely used digital modulation technique that encodes data by varying the phase of a carrier signal. Coherent demodulation, which requires synchronization of the receiver's local oscillator with the incoming carrier, is essential for accurately recovering the transmitted data. The project involved designing a demodulation circuit comprising a local oscillator, phase detector, low-pass filter, and decision-making circuitry. The circuit was simulated using Proteus and MATLAB to validate its functionality and robustness in the presence of noise. Following successful simulation, the circuit was implemented in hardware using discrete components, and its performance was verified using an oscilloscope. The results demonstrated that the circuit effectively demodulated the PSK signal, recovering the original data with high accuracy. This project highlights the practical application of coherent PSK demodulation in communication systems and provides a foundation for further exploration of advanced demodulation techniques.

2. Introduction

Phase Shift Keying (PSK) is a digital modulation technique that uses a reference signal's (the carrier wave) phase shift to transmit data. Because of its effectiveness in terms of both power and bandwidth, PSK is frequently utilized in communication systems. The design, simulation, and hardware implementation of a PSK demodulation circuit are the main objectives of this project. In order to verify the design, the circuit was first constructed in hardware after being simulated using Proteus, simulink and MATLAB.

3. Objectives

- To design a PSK demodulation circuit.
- To simulate the circuit using Proteus and MATLAB.
- To implement the circuit in hardware and verify its functionality.
- To analyze the performance of the demodulation circuit.

4. Methodology

4.1. PSK Coherent Demodulation Theory

- **Carrier Recovery:** The receiver must generate a local carrier signal that is synchronized in frequency and phase with the incoming carrier. This can be achieved using a Phase-Locked Loop (PLL) or other synchronization techniques.
- **Phase Detection**: The incoming PSK signal is mixed with the recovered carrier in a phase detector. The output of the phase detector is a signal that represents the phase difference between the incoming signal and the local carrier.
- **Low-Pass Filtering:** The output of the phase detector contains high-frequency components that need to be filtered out. A low-pass filter (LPF) is used to retrieve the baseband signal, which corresponds to the original digital data.
- **Decision Making:** The filtered signal is passed through a comparator or decision circuit to determine the transmitted bits. The decision threshold is set to distinguish between the different phase states (e.g., 0 and 1 in BPSK).

4.2. Circuit Components

The PSK demodulation circuit consists of the following key components:

- **Local Oscillato**r: Generates a reference signal synchronized with the carrier.
- **Phase Detector**: Compares the phase of the incoming signal with the reference signal.
- **Low-Pass Filter (LPF)**: Filters out high-frequency components to retrieve the baseband signal.
- **Comparator**: Converts the analog signal to digital form.

4.3. Circuit Diagram

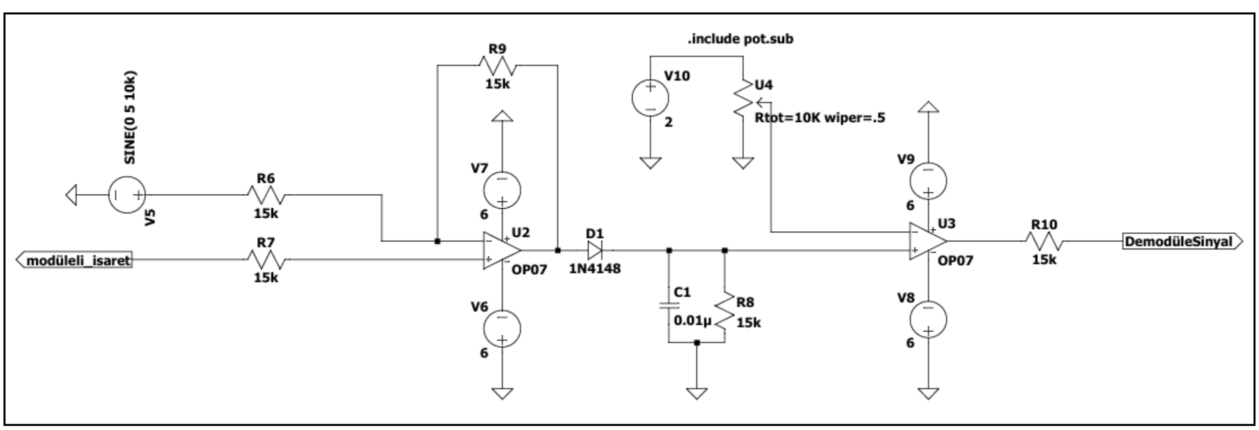


Figure 1: PSK Demodulation Circuit Diagram

4.4. Simulation

4.4.1. Proteus simulation

The circuit was first simulated using Proteus to verify its functionality. The simulation involved generating a PSK modulated signal and passing it through the demodulation circuit. The output was observed to ensure correct demodulation.

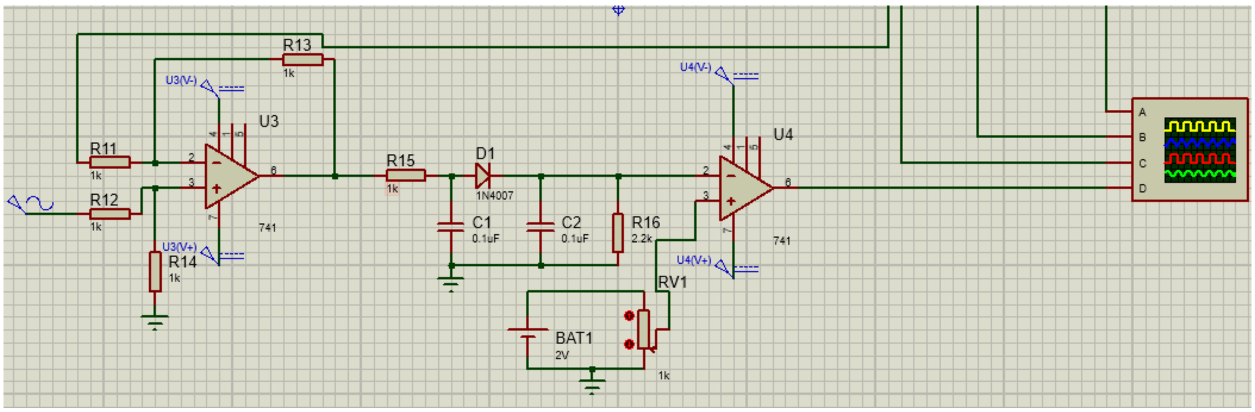
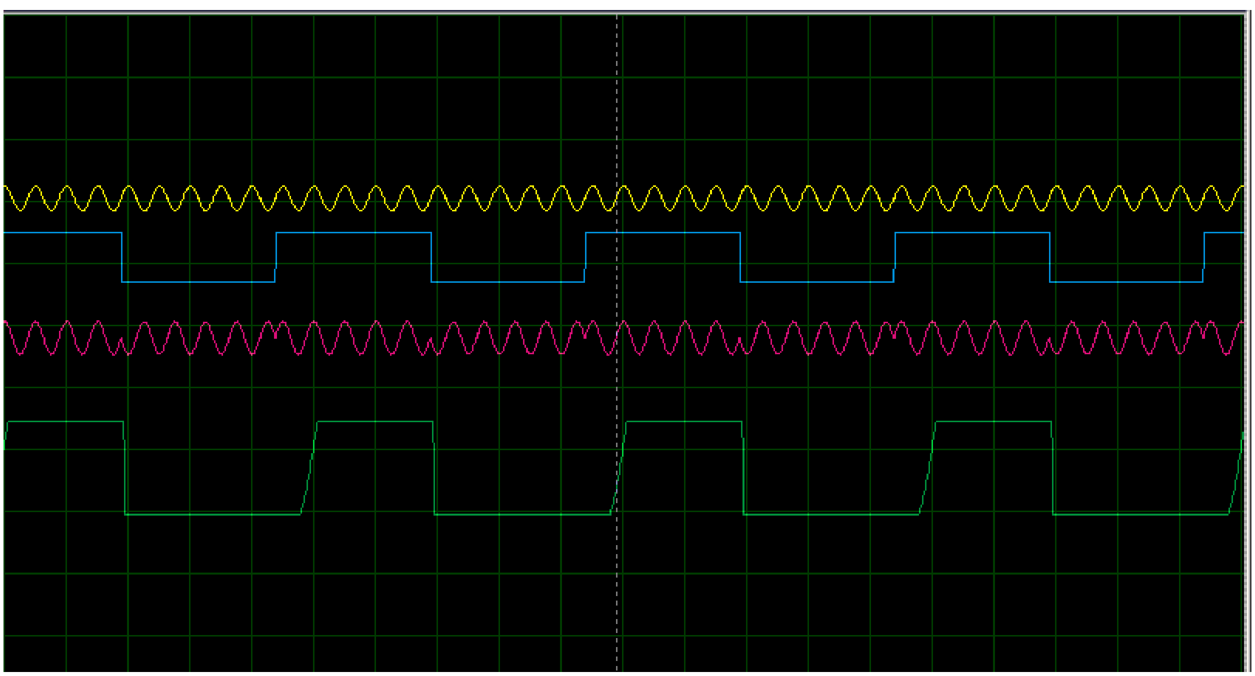


Figure 2: Proteus Simulation Circuit



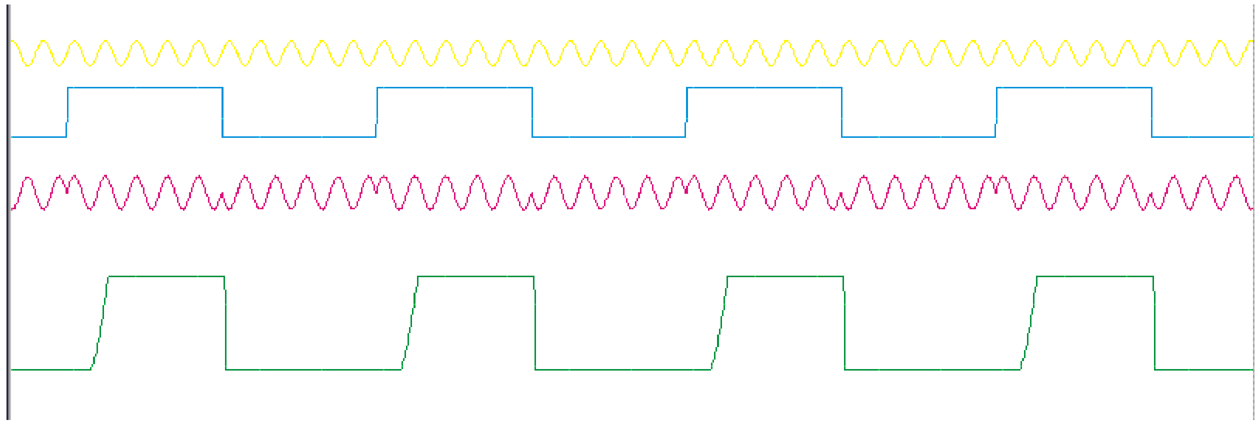


Figure 3: Proteus Simulation Output

4.4.2. MATLAB Simulation

MATLAB was used to simulate the PSK demodulation process. The simulation included generating a PSK signal, adding noise, and demodulating the signal using a coherent detector.

Code:

```
clc; clear; close all;

% Parameters
fs = 100;   % Sampling frequency per bit
fc = 10;    % Carrier frequency (Hz)
N = 10;     % Number of bits
T = 1;      % Bit duration (sec)
t = linspace(0, T, fs); % Time vector for one bit
time_axis = linspace(0, N*T, N*fs); % Full signal time axis

% Generate random bit sequence (0s and 1s)
bits = randi([0 1], 1, N);

% Generate Square Wave Input
square_wave = [];
for i = 1:N
    square_wave = [square_wave, bits(i) * ones(1, fs)];
```

```
end

% BPSK Modulation: Map 0 -> -1, 1 -> +1
bpsk_signal = 2*bits - 1;

% Modulated signal
modulated_signal = [];
for i = 1:N
    modulated_signal = [modulated_signal, bpsk_signal(i) * cos(2 * pi * fc
* t)];
end

% BPSK Demodulation (Perfect Channel)
demodulated_bits = [];
received_signal = modulated_signal .* cos(2 * pi * fc * time_axis); %
Coherent detection
for i = 1:N
    bit_energy = sum(received_signal((i-1)*fs + 1 : i*fs)); % Integrate
over bit duration
    demodulated_bits = [demodulated_bits, bit_energy > 0];
end

figure;
subplot(3,1,1);
plot(time_axis, square_wave, 'LineWidth', 1.5);
ylim([-0.5, 1.5]);
xlabel('Time (s)');
ylabel('Amplitude');
title('Original Square Wave Bit Sequence');
grid on;

subplot(3,1,2);
plot(time_axis, modulated_signal, 'LineWidth', 1.5);
xlabel('Time (s)');
ylabel('Amplitude');
title('BPSK Modulated Signal');
grid on;

subplot(3,1,3);
stair(demodulated_bits);
ylim([-0.5 1.5]);
xlabel('Bit Index');
ylabel('Bit Value');
```

```
title('Demodulated Bit Sequence');
grid on;
```

Output:

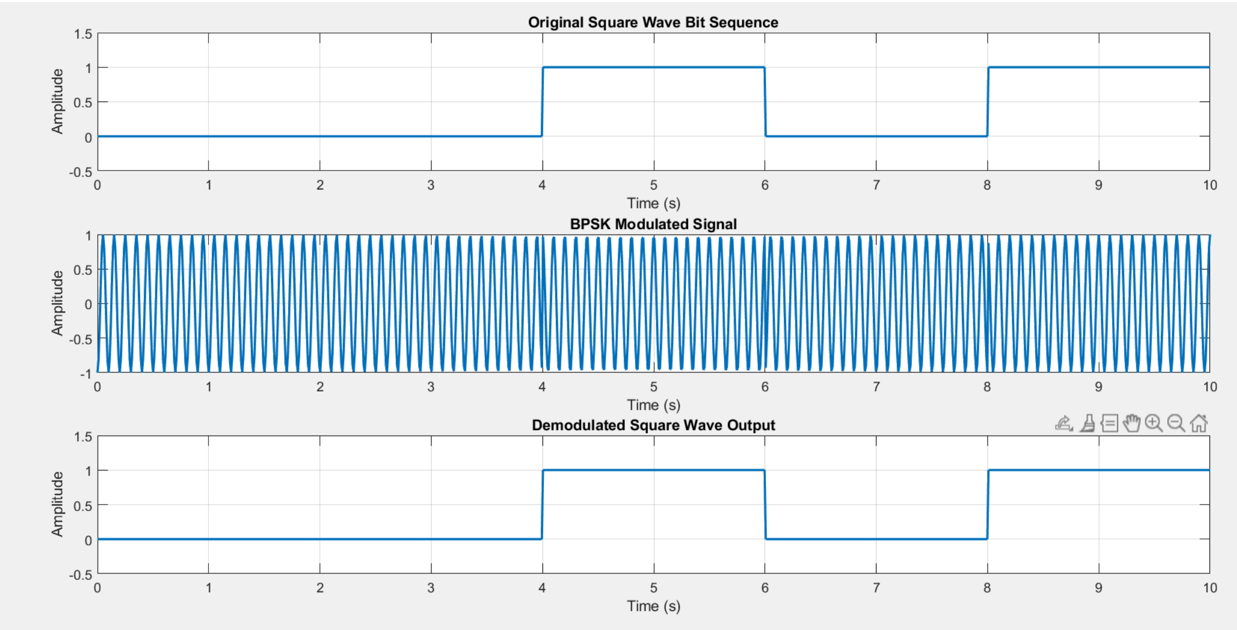


Figure 4: MATLAB Simulation Results

4.3. SIMULINK Simulation

The original message signal is successfully transmitted and recovered thanks to the Simulink model's demonstration of BPSK modulation and demodulation, which includes carrier multiplication and filtering.

Diagram:

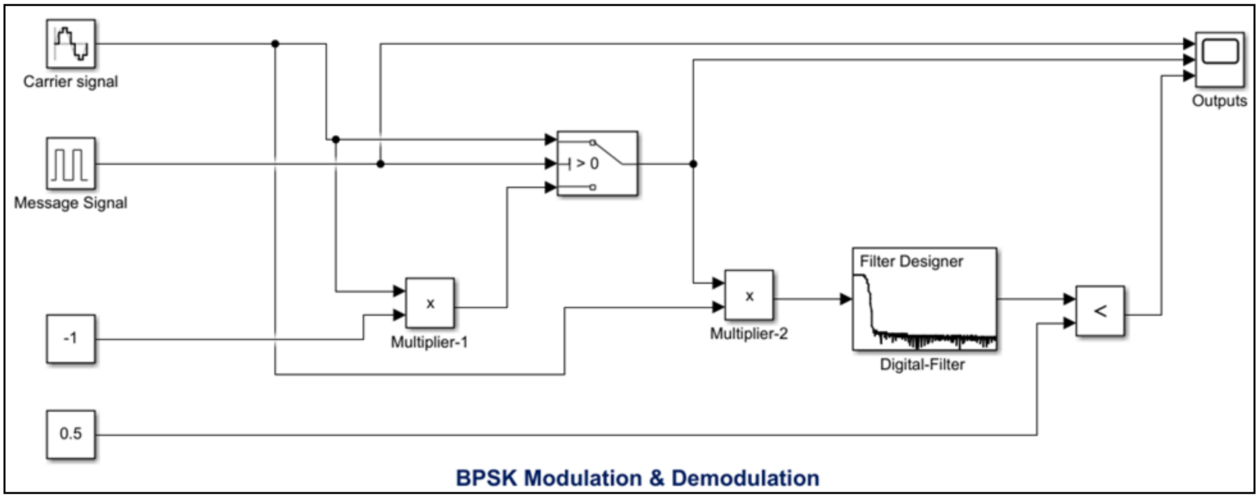


Figure 5: SIMULINK Simulation Circuit

Output:

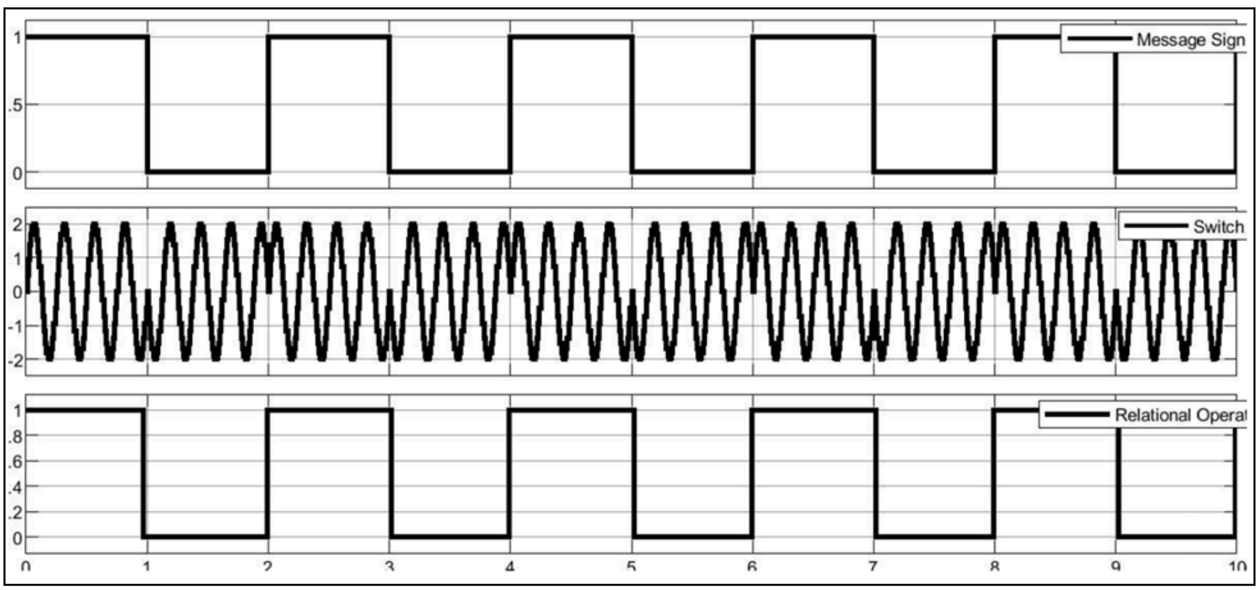


Figure 6: SIMULINK Simulation Results

4.5. Hardware Implementation

The PSK demodulation circuit was implemented on a breadboard using discrete components. The local oscillator was realized using a function generator, and the phase detector was implemented using a 741 op-amp configured as a subtractor. The subtractor was used to subtract the carrier from the modulated signal, leaving the out-of-phase part of the modulated signal.

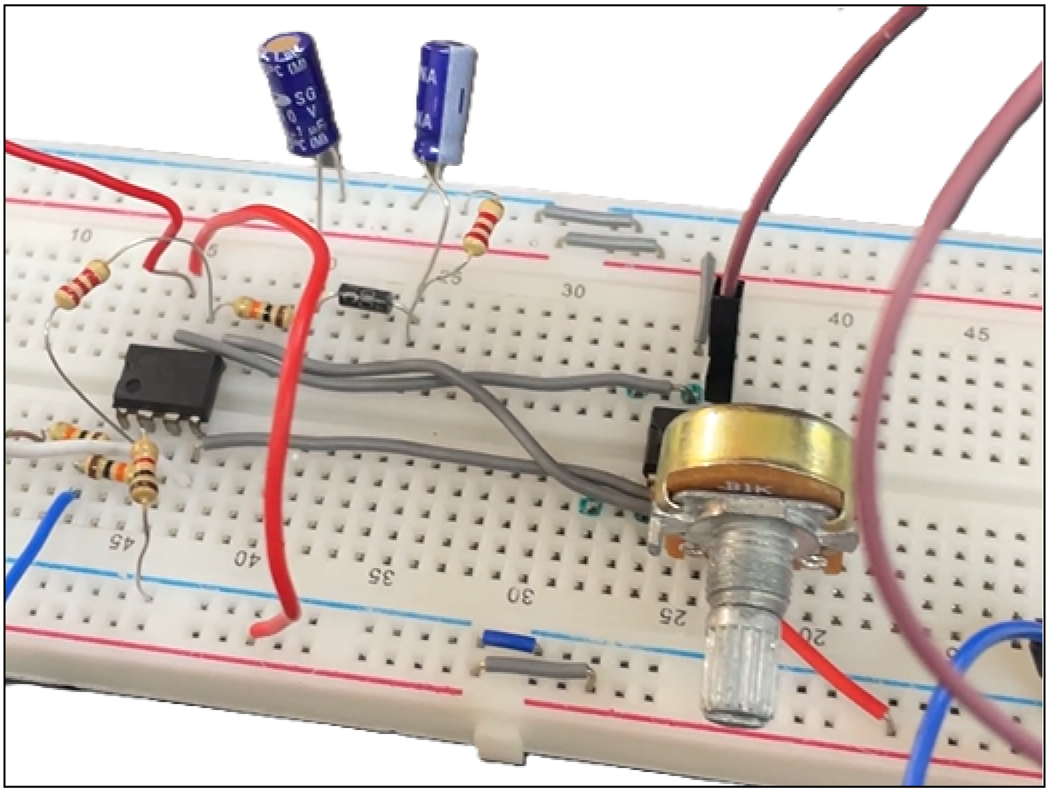


Figure 5: Hardware Implementation Setup

4.5.1. Phase Detector

The phase detector was designed using a 741 op-amp configured as a subtractor. The subtractor removes the in-phase component of the carrier, leaving the out-of-phase component of the modulated signal.

4.5.2. Low-Pass Filter

An RC low-pass filter was designed to cut off high-frequency components (around 2 kHz). The filter used a diode (1N4007), a 0.1 μF capacitor, and a 2.2 kΩ resistor.

4.5.3. Comparator

The same 741 op-amp was used as a comparator, with a reference voltage of 0 volts. The comparator converts the filtered analog signal into digital form, representing the original data.

7. Results and Analysis

7.1. Simulation Results

The Proteus and MATLAB simulations confirmed that the demodulation circuit correctly extracts the original data from the PSK modulated signal. The MATLAB simulation also demonstrated the circuit's robustness in the demodulation.

7.2. Hardware Results

The hardware implementation successfully demodulated the PSK signal, with the output matching the expected digital data. The oscilloscope traces showed clear transitions corresponding to the transmitted bits. However the demodulated signal couldn’t hold the high voltage for a long time due to capacitance issues in the comparator we used so there is up and down in the logic 1 or the high value region.

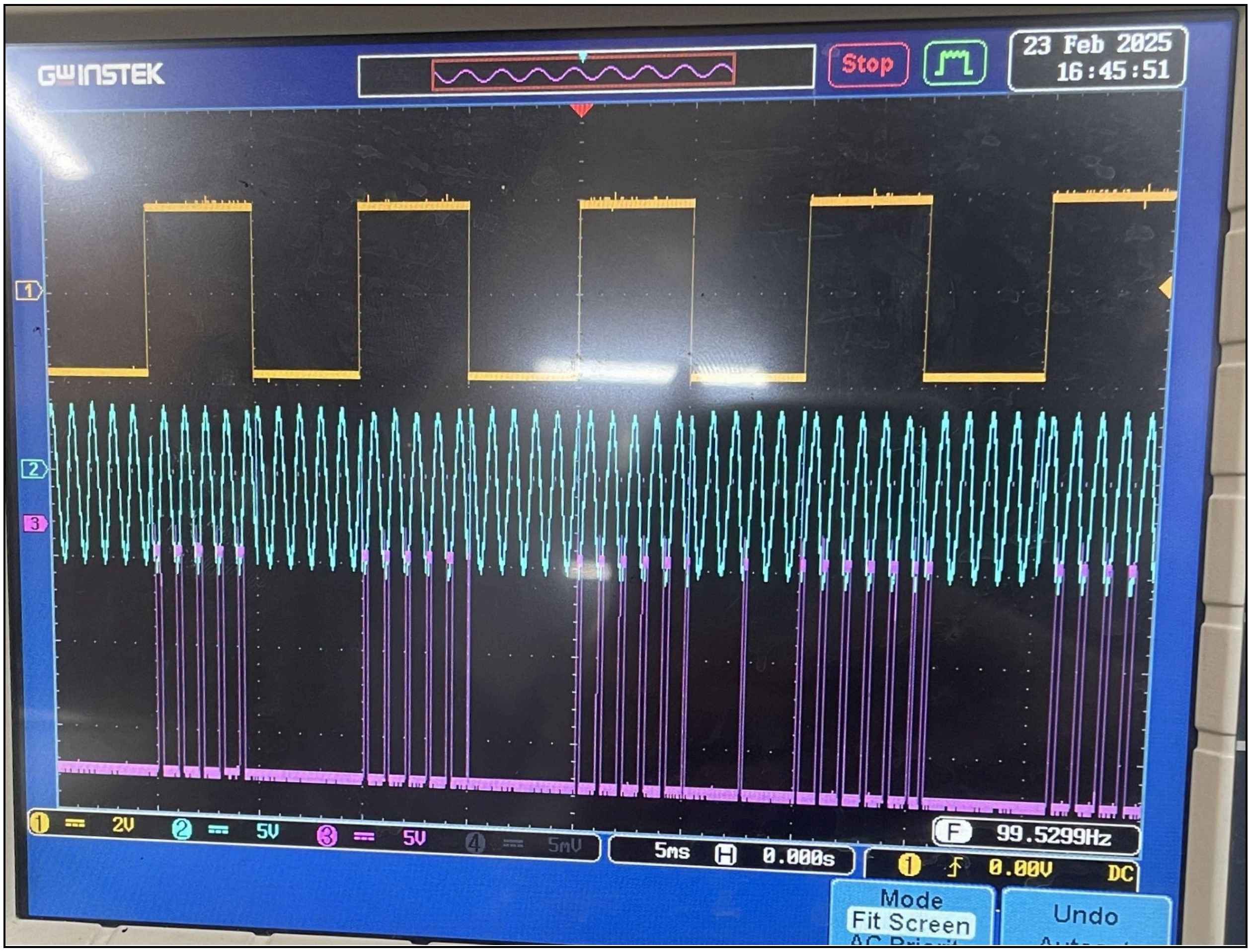


Figure 6: Oscilloscope Output

8. Conclusion

The PSK demodulation circuit was successfully designed, simulated, and implemented in hardware, demonstrating the practical application of coherent demodulation in digital communication systems. The simulations in Proteus and MATLAB validated the circuit's functionality, showing its ability to accurately extract the original data from the PSK modulated signal, even in the presence of noise. The hardware implementation, using a 741 op-amp as a subtractor for phase detection, an RC low-pass filter for noise reduction, and the same op-amp as a comparator for decision-making, confirmed the feasibility of the design.

However, during the hardware implementation, a limitation was observed in the comparator stage. The demodulated signal exhibited fluctuations in the high voltage region (logic 1), likely due to capacitance issues in the 741 op-amp used as a comparator. This caused the signal to not hold a stable high value for an extended period, leading to variations in the output. Despite this issue, the circuit successfully demodulated the PSK signal, and the output matched the expected digital data, as verified by oscilloscope measurements.

Overall, the project successfully demonstrated the principles of coherent PSK demodulation and provided valuable insights into the challenges and considerations involved in hardware implementation. It serves as a foundation for further exploration and optimization of digital communication systems.

9. Future Work

- To boost performance, implement the circuit using integrated circuits.
- Examine more complex demodulation methods like differential PSK (DPSK).
- Assess the circuit's functionality in an actual communication system.

10. References

- Steber, J. Mark. "PSK demodulation (Part 1)." WJ Tech Notes 11.2 (1984).
- Proakis, J. G., & Salehi, M. (2008). **Digital Communications**. McGraw-Hill.
- Haykin, S. (2001). **Communication Systems**. John Wiley & Sons.
- MATLAB Documentation.

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