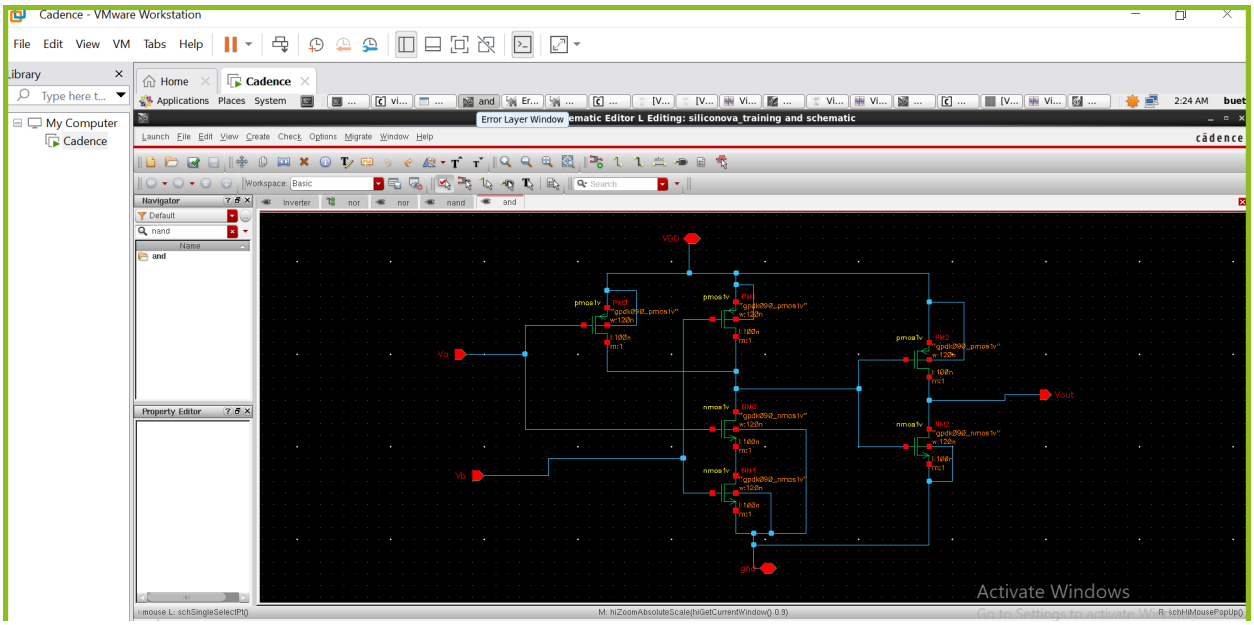
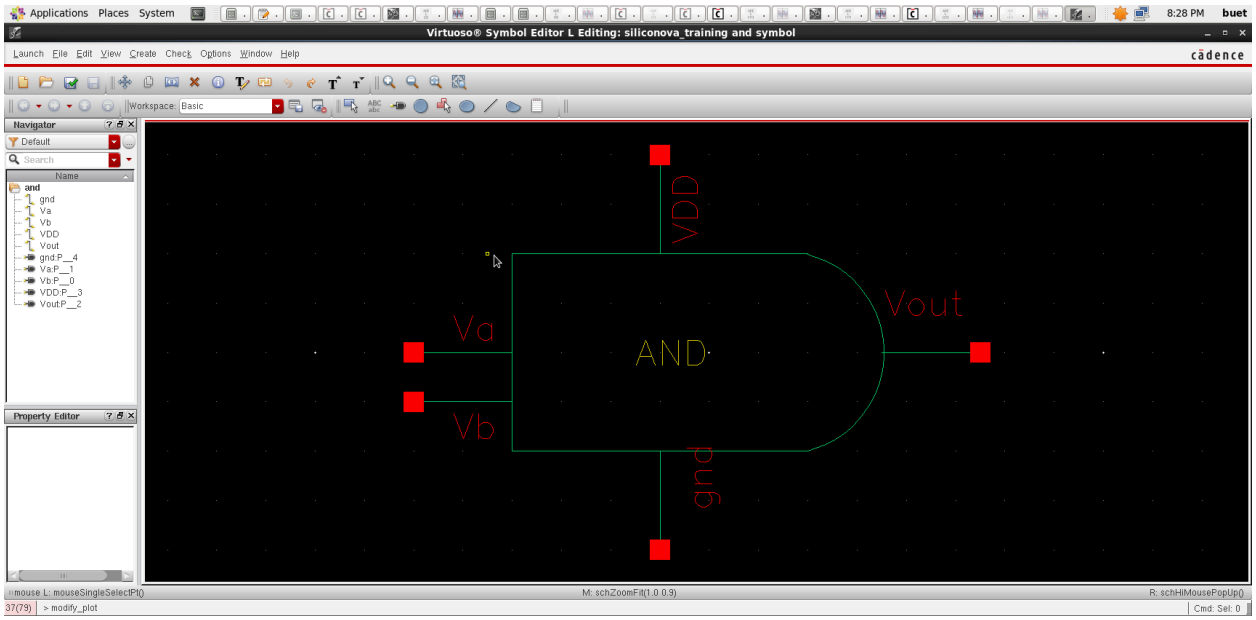
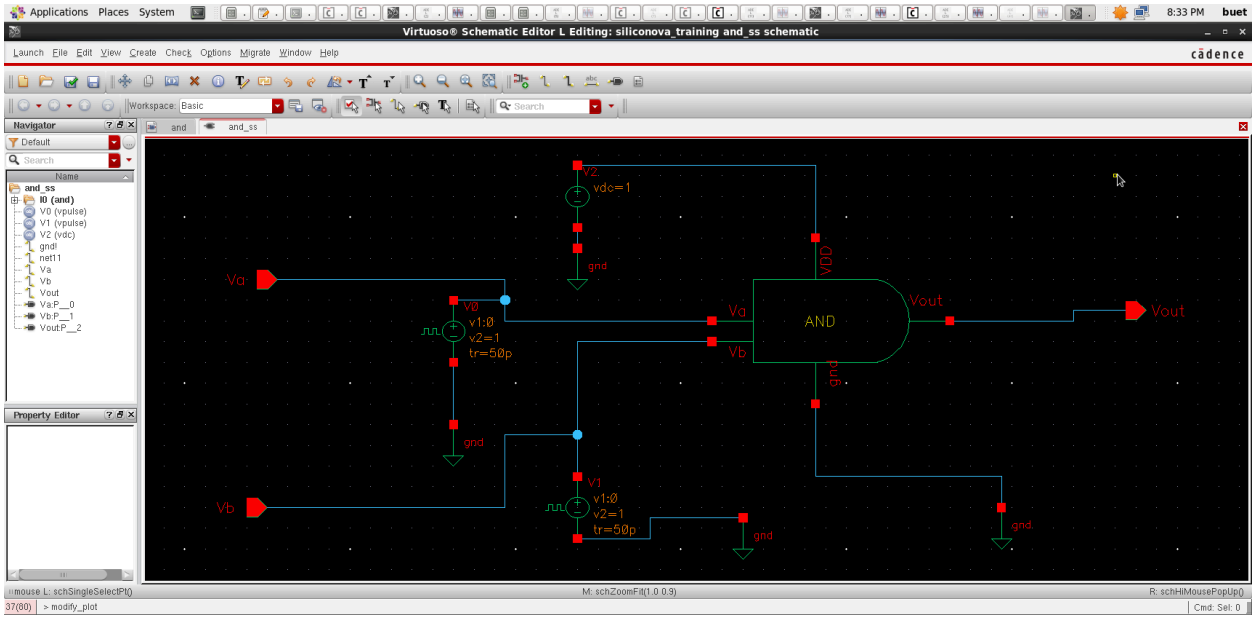
AND Gate



Symbol of AND Gate:

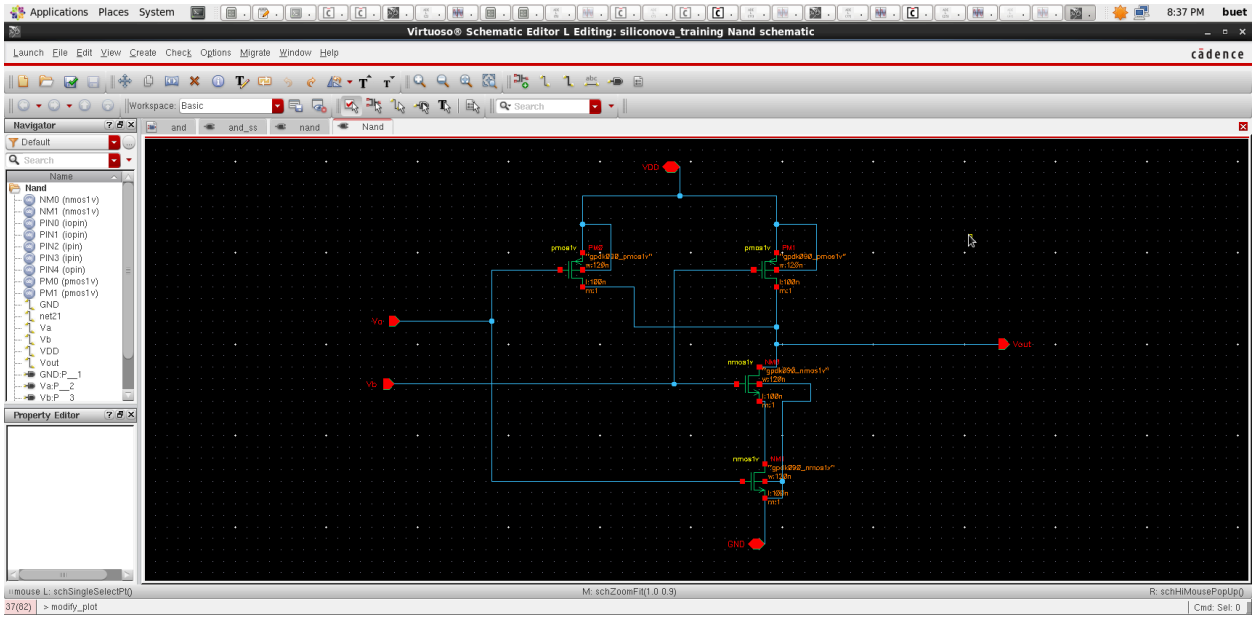


Testbench Diagram:

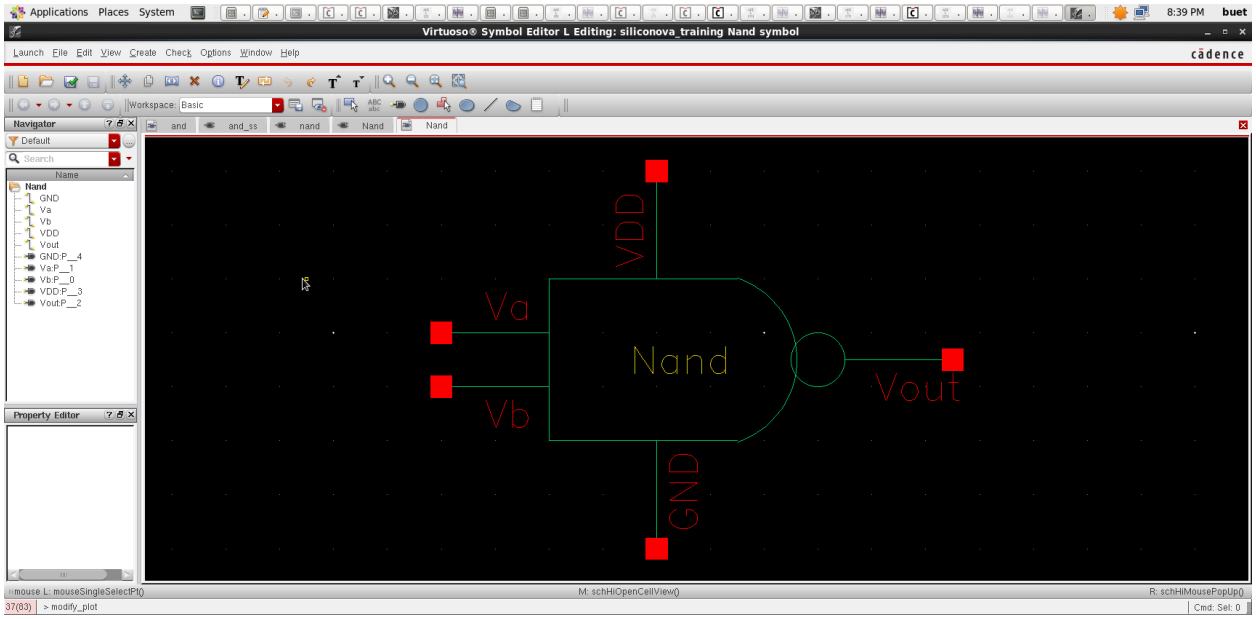


Output of Testbench Diagram in Transient Response:

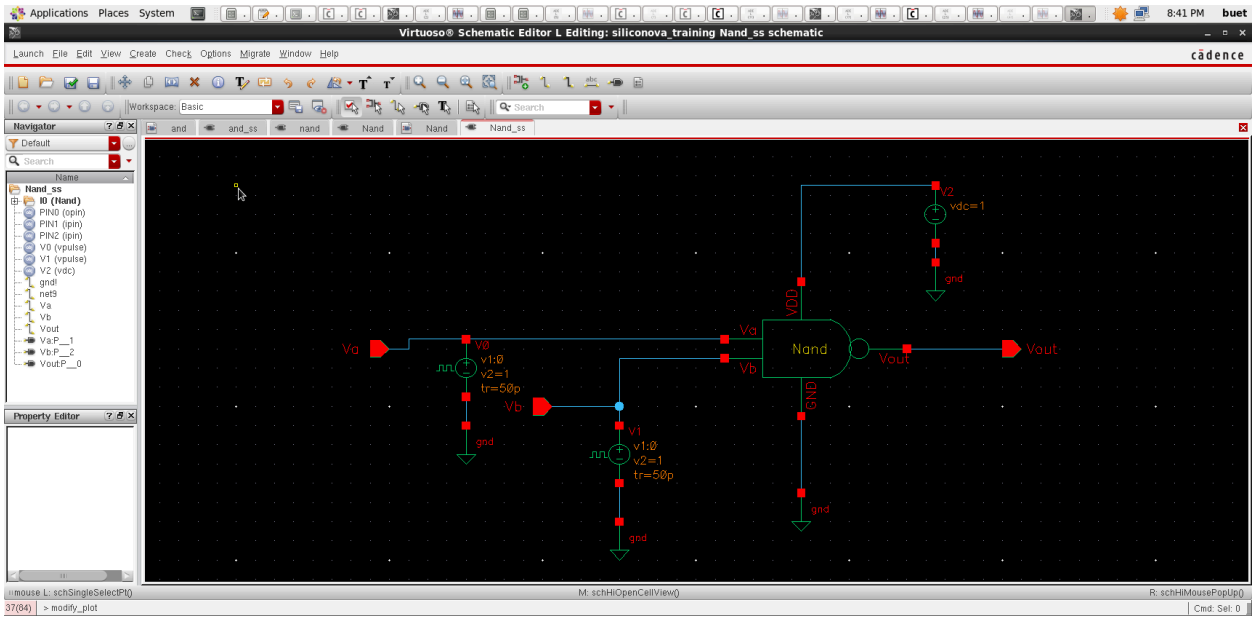
NAND Gate



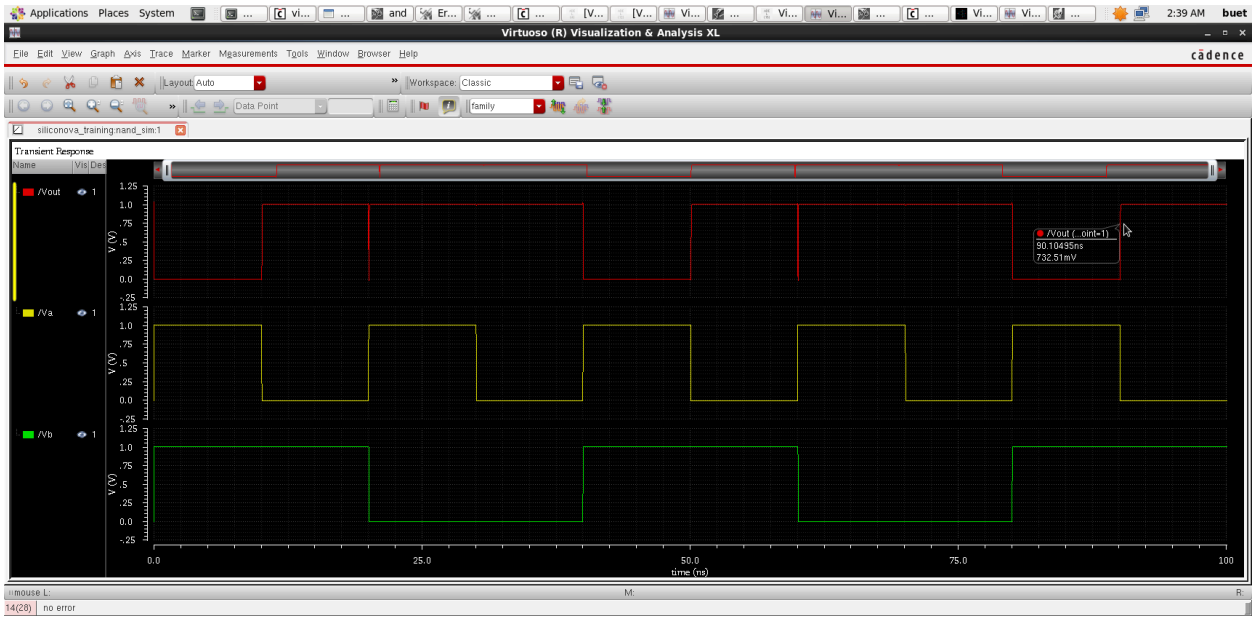
Symbol of NAND Gate:



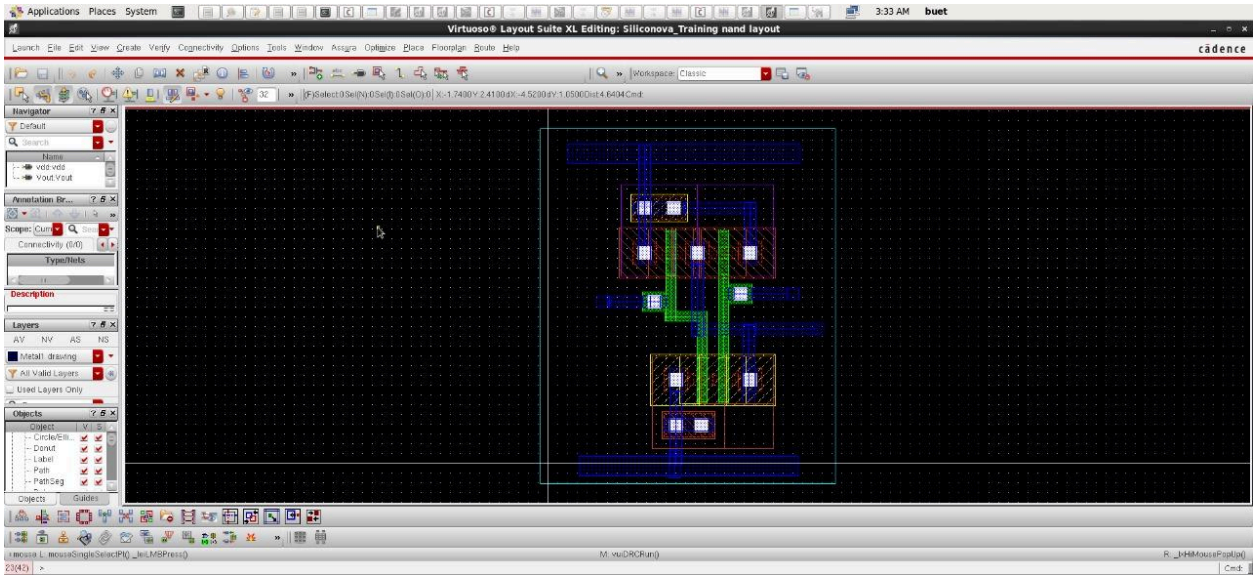
Schematic Diagram of testbench:



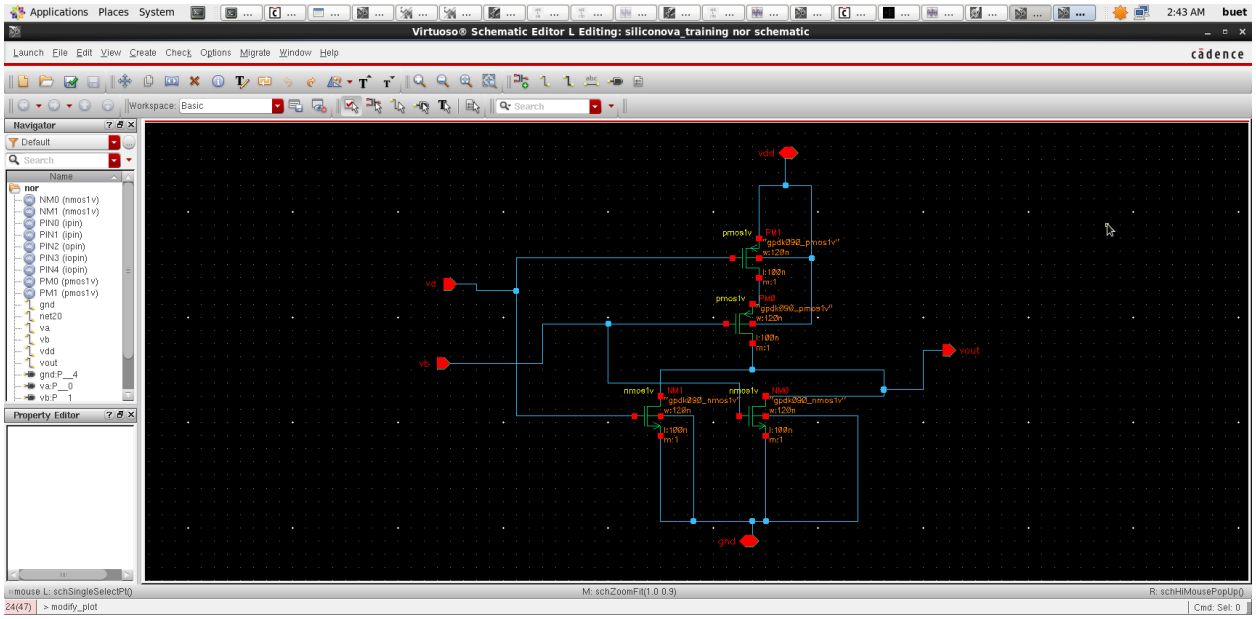
Output:



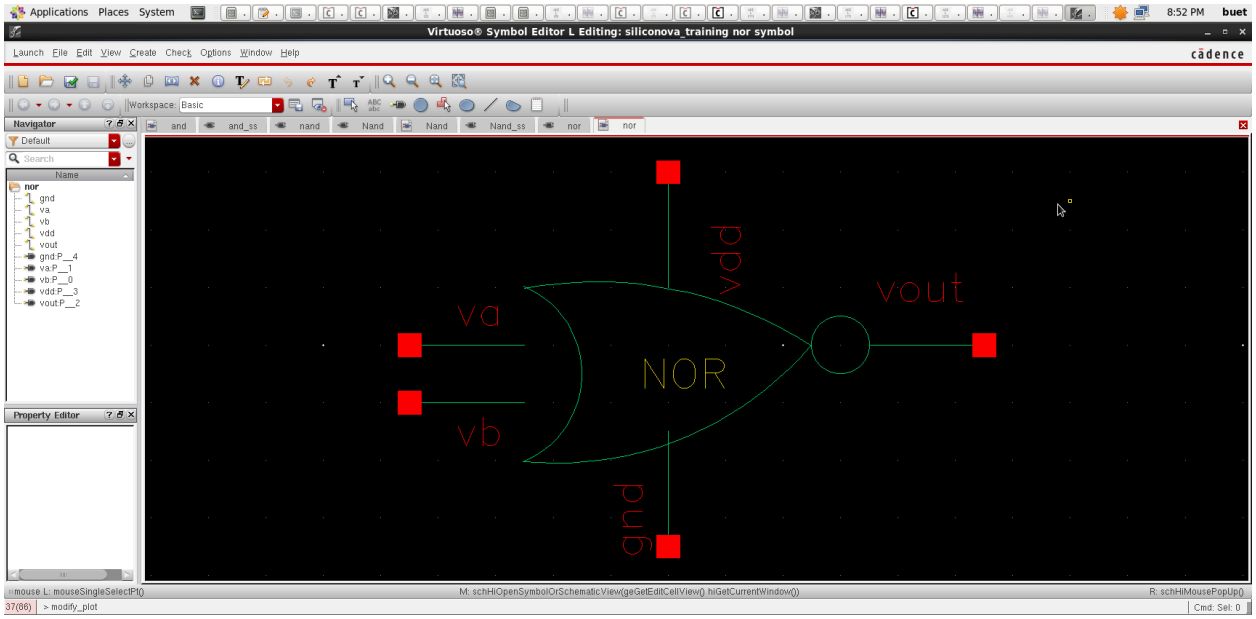
Layout: layout of Nand gate



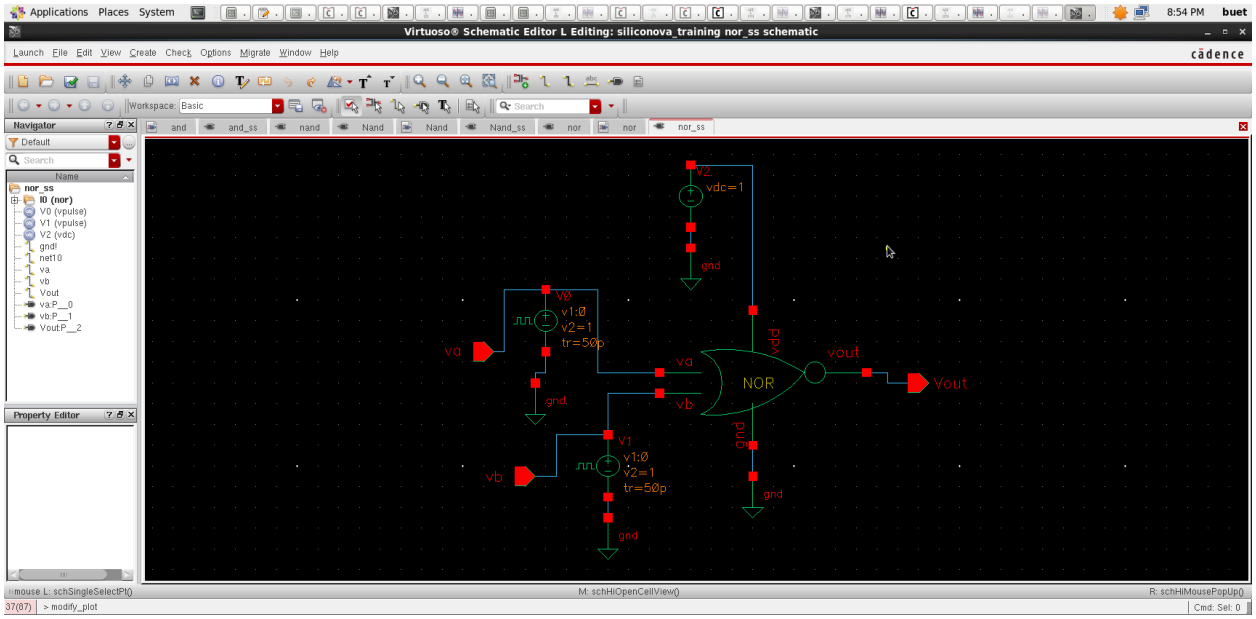
NOR Gate



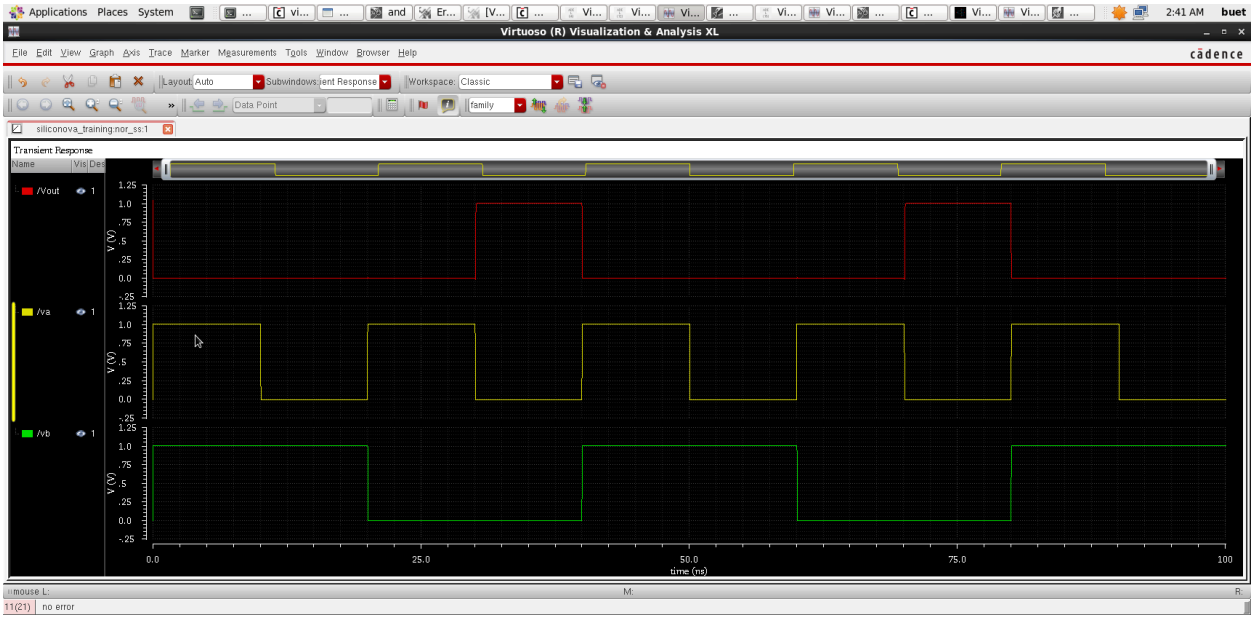
Symbol of NOR Gate:



Schematic diagram of testbench:



Output:



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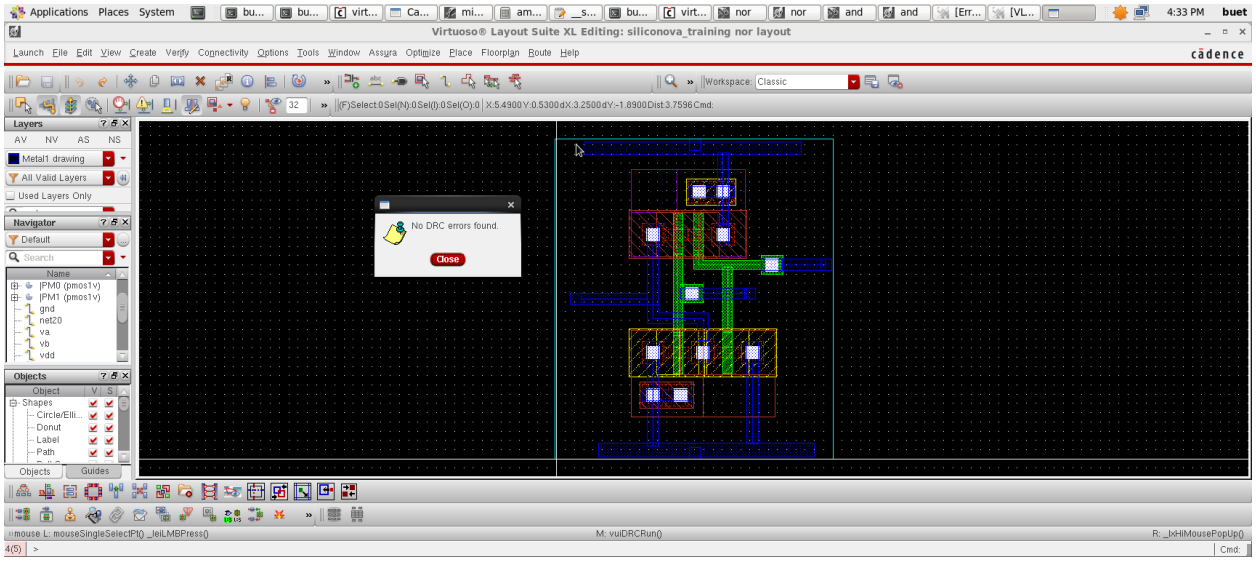
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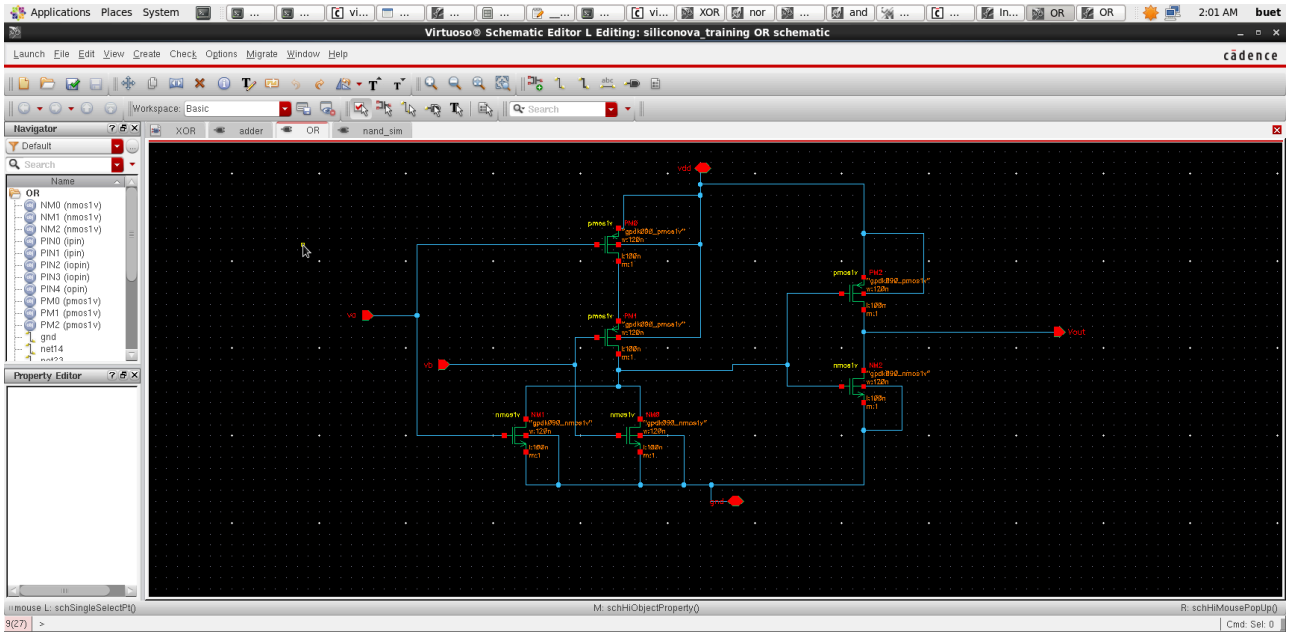
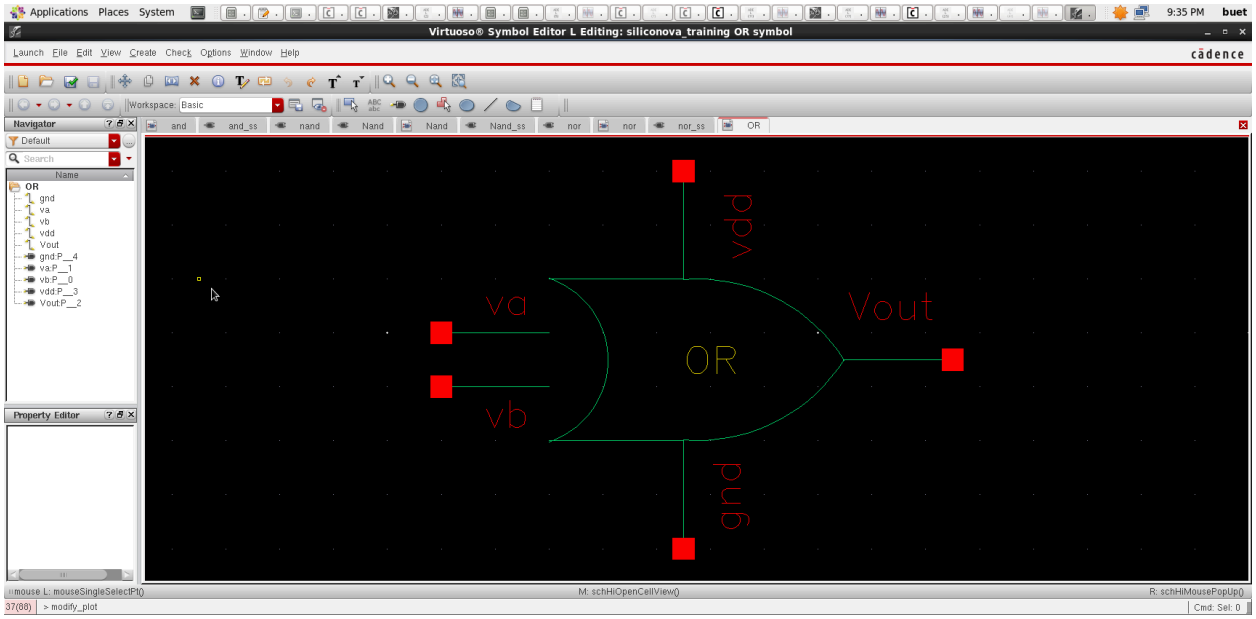
No DRC errors found.
Close

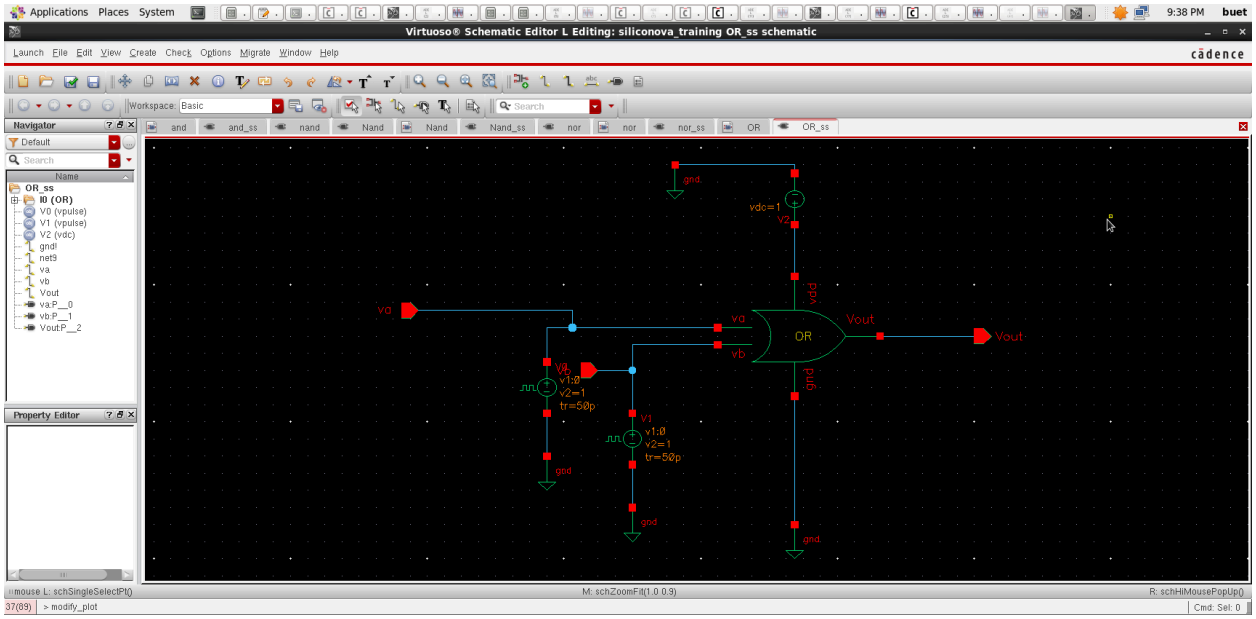
OR Gate



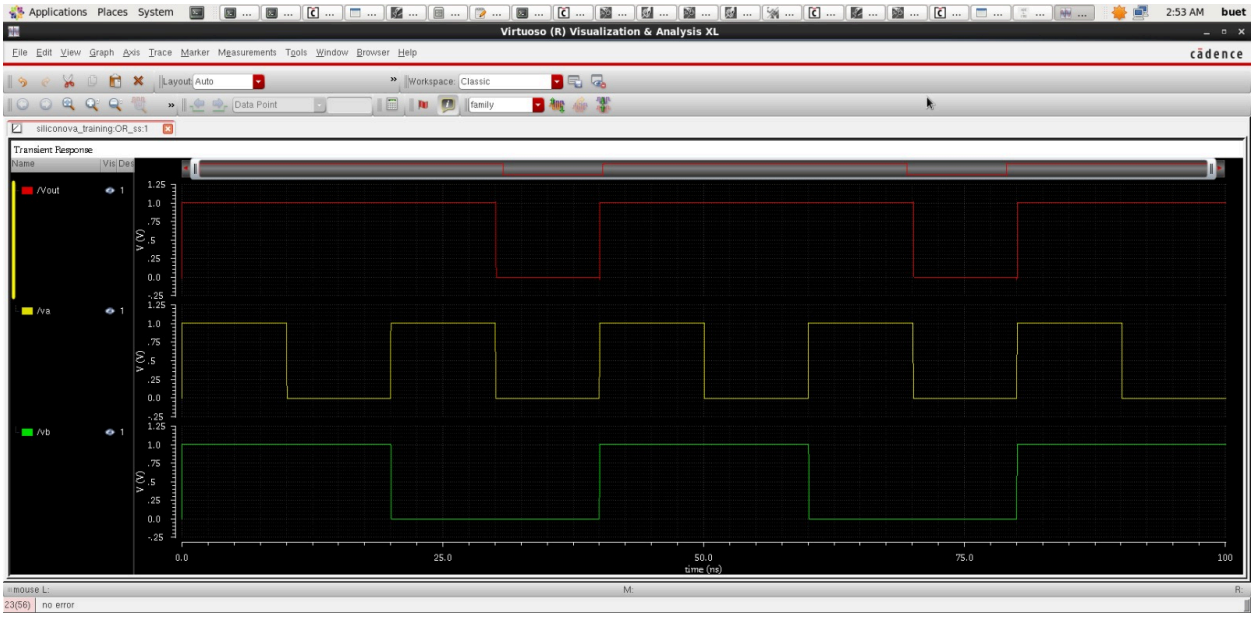
Symbol:



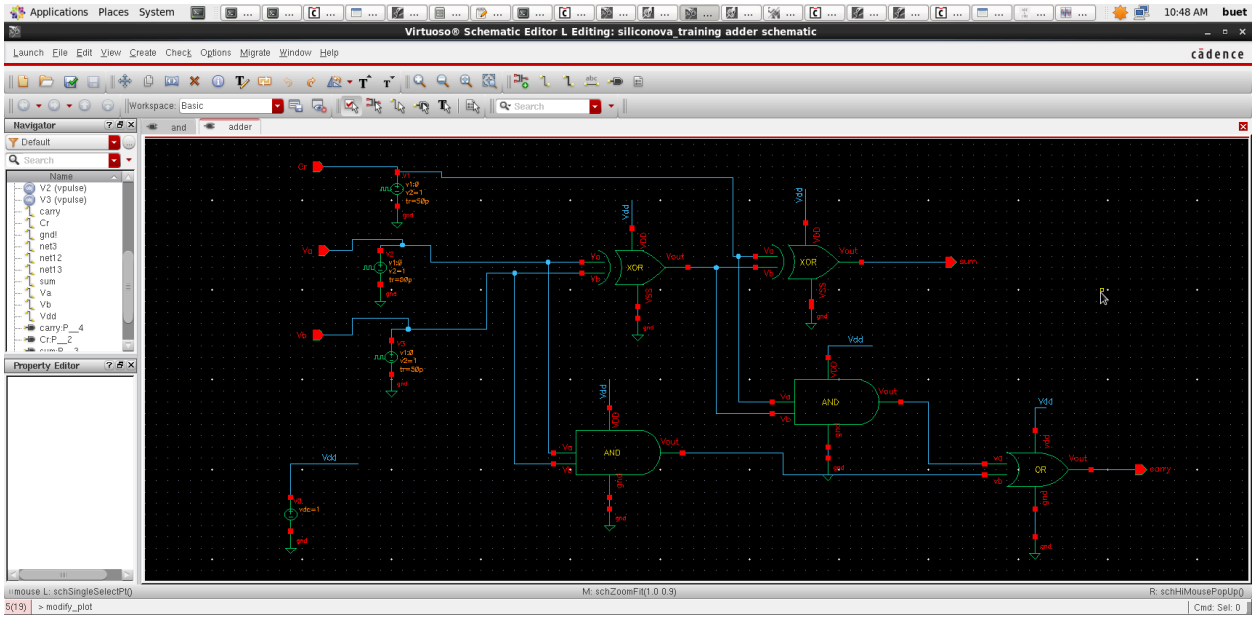
Testbench diagram of OR Gate:



Output:



ADDER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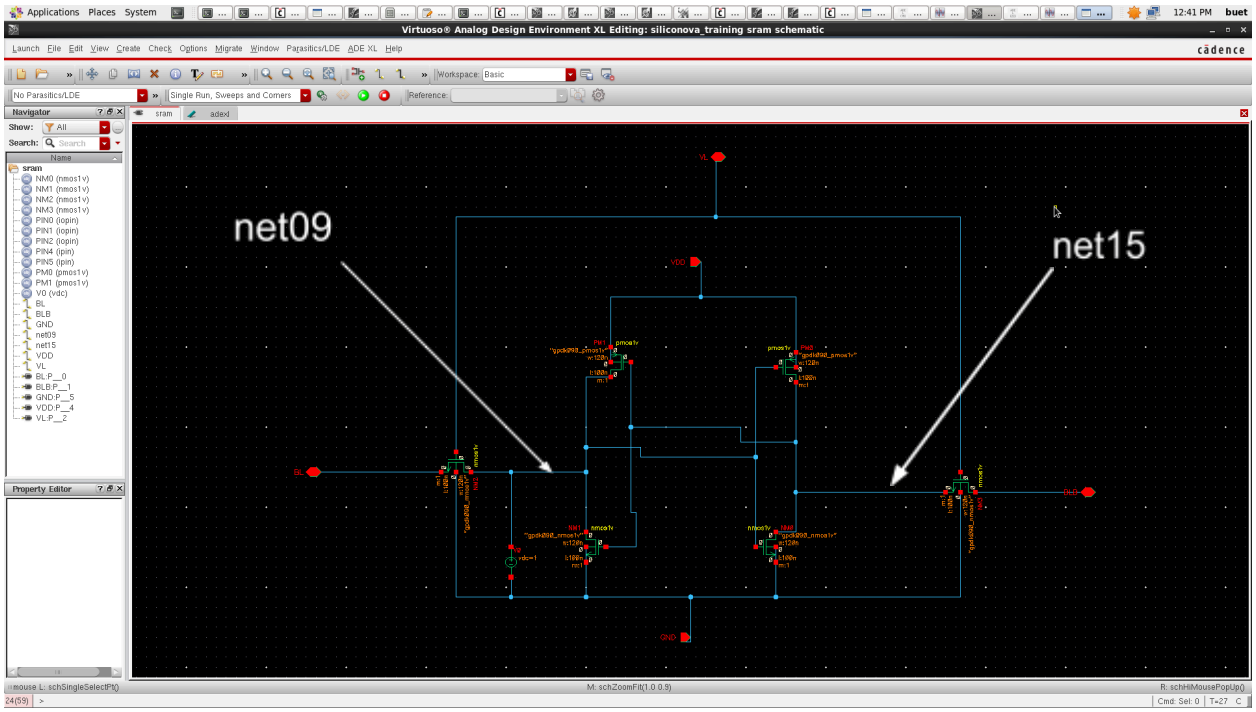
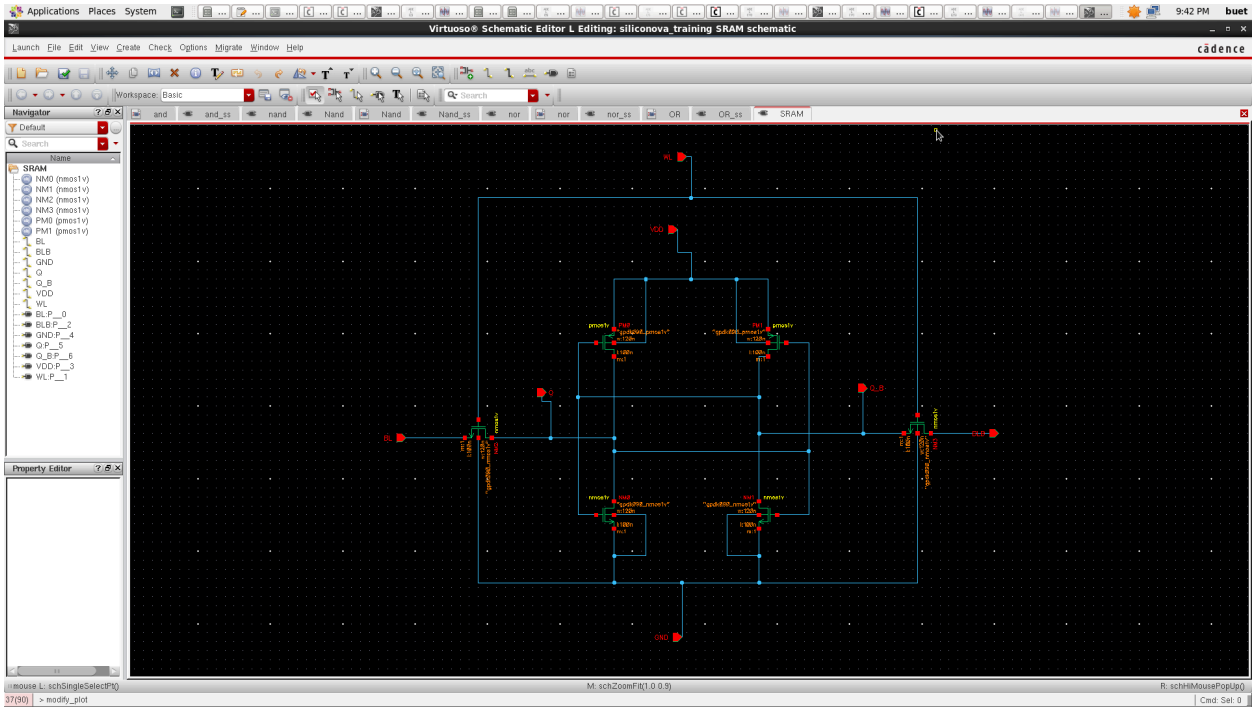
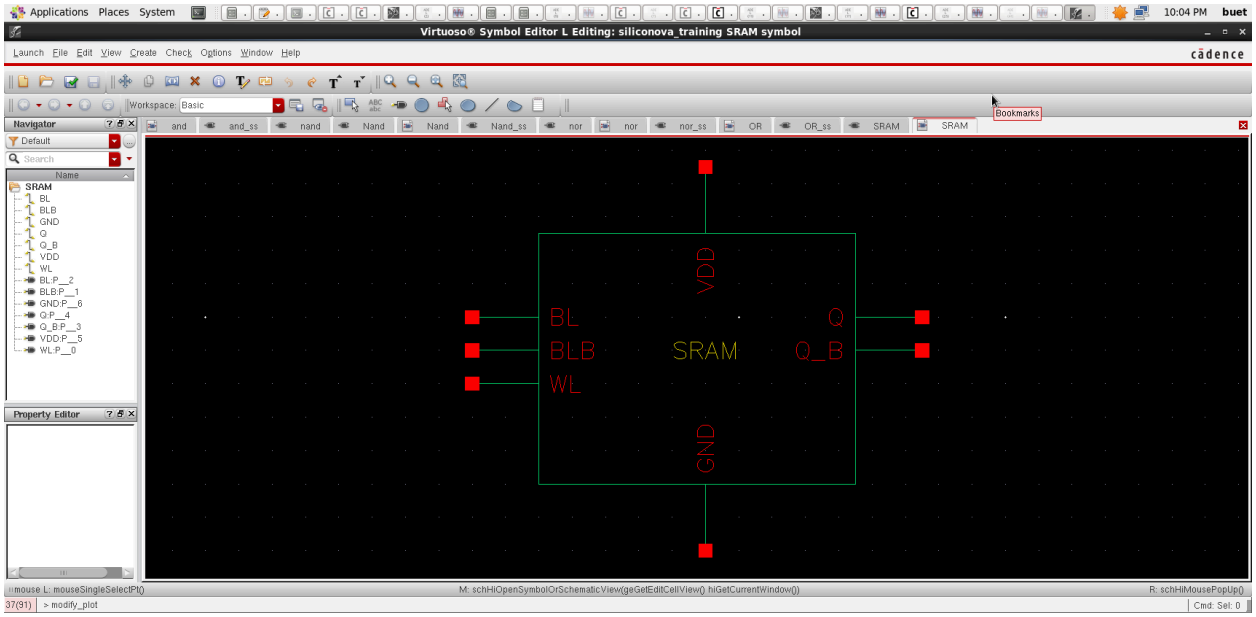
6T SRAM

Schematic of 6 T SRAM:

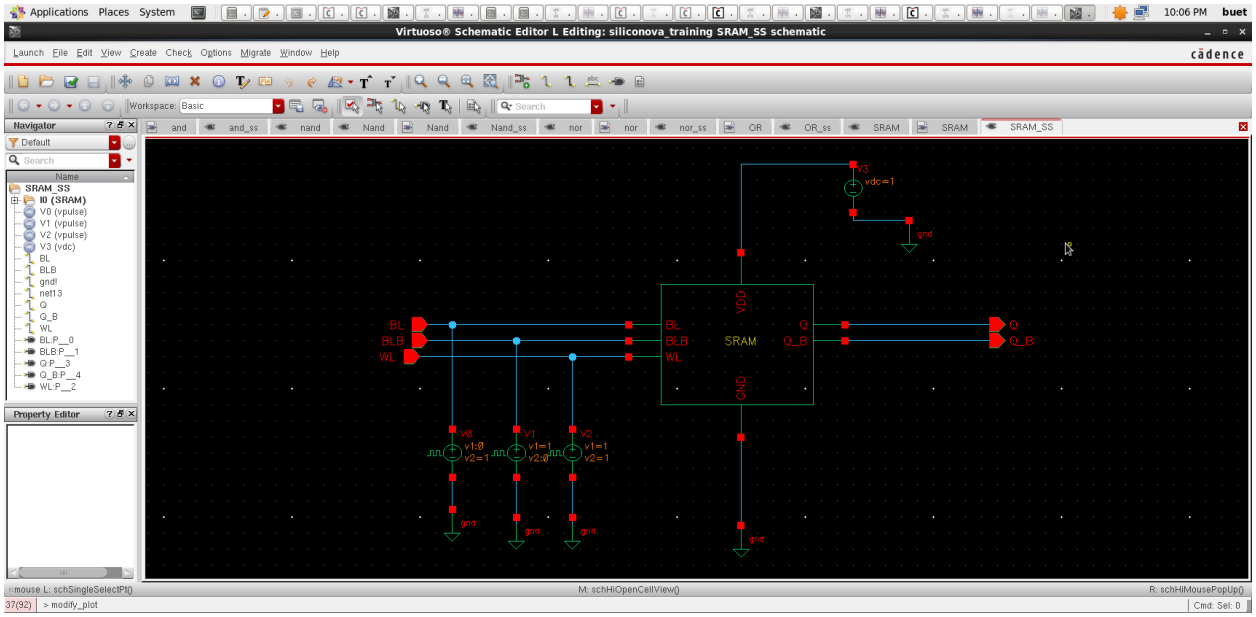




Symbol:

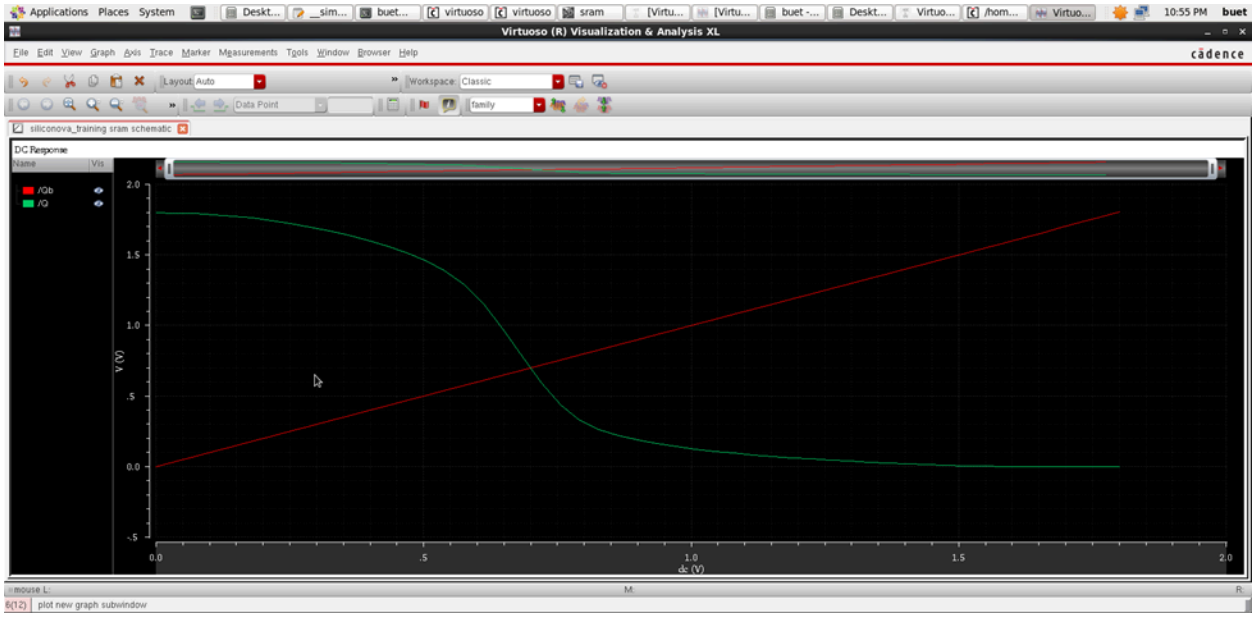


Testbench:

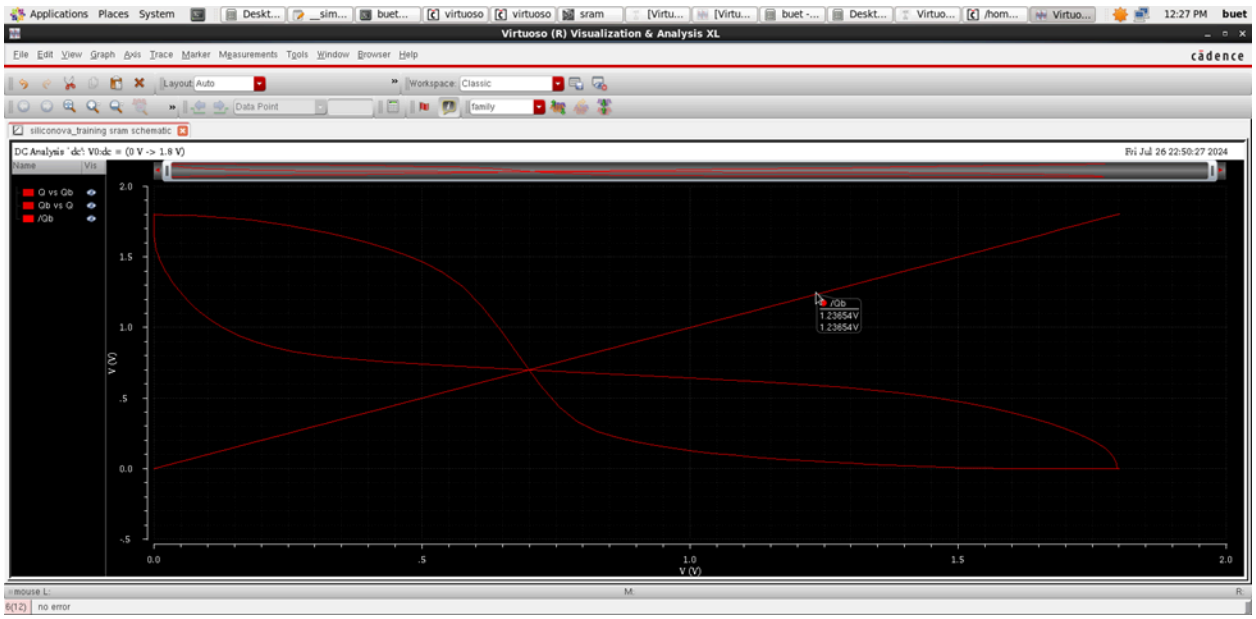


Output: Output of Transient Analysis

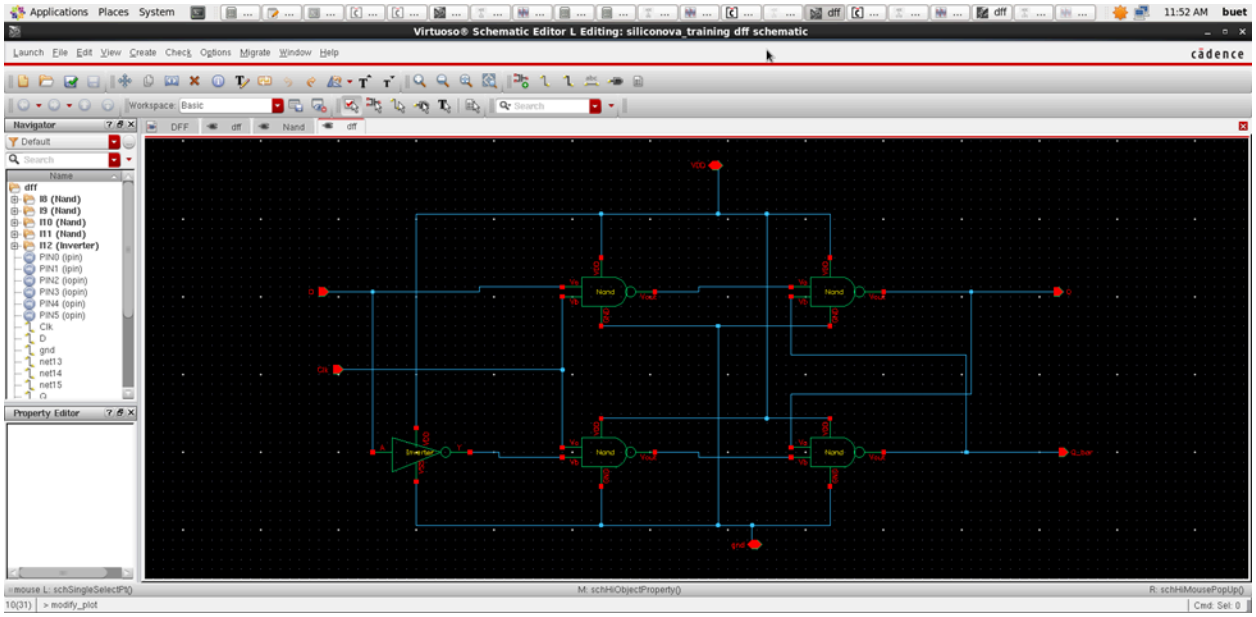
Output: Output for DC analysis



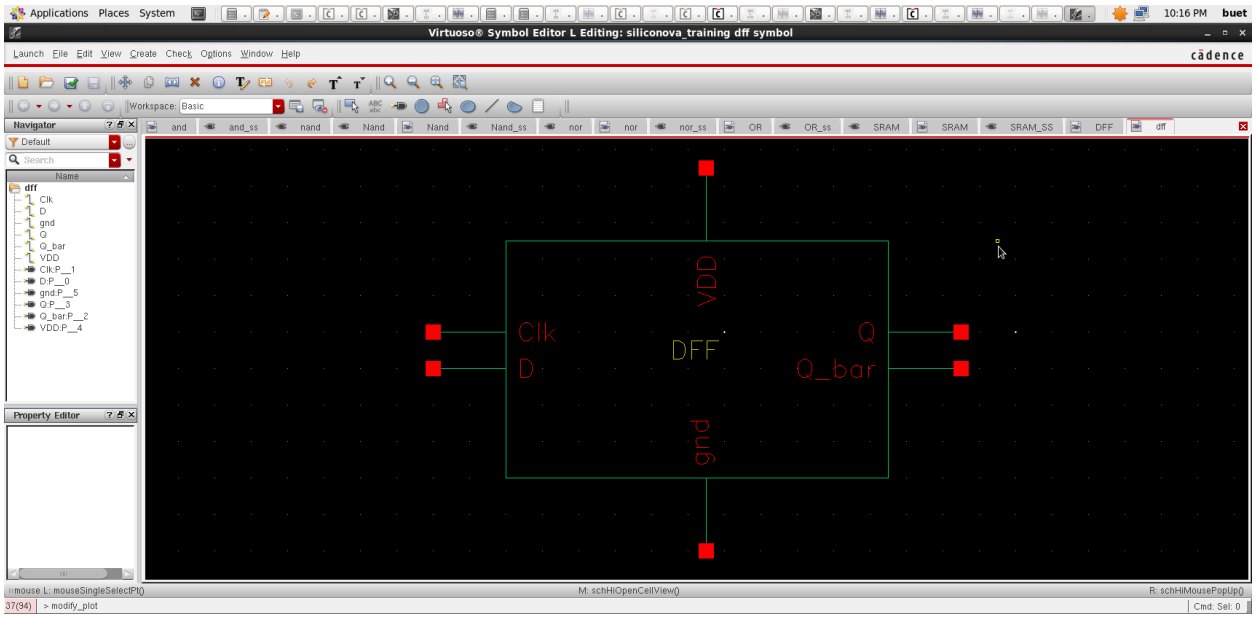
Butterfly Graph:



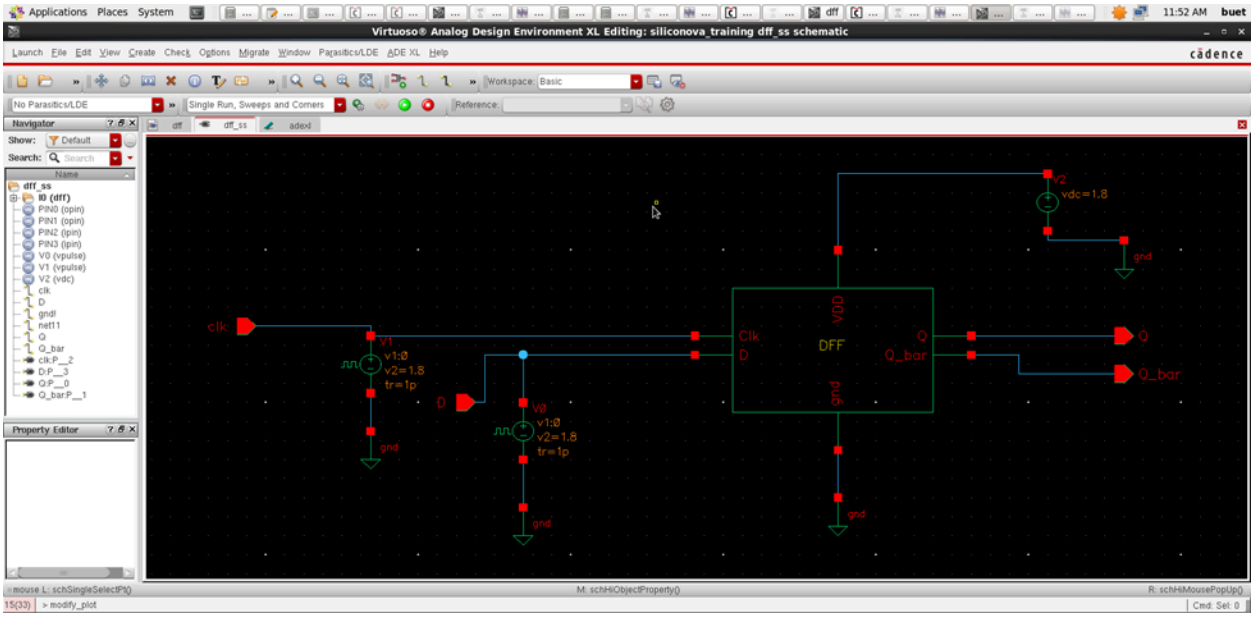
D Flip Flop



Symbol of D Flip Flop:



Testbench



Output: Transient Analysis