KeyStone Architecture
External Memory Interface (EMIF16)

User Guide

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Release History

Release	Date	Chapter/Topic	Description/Comments
Revision A	May 2011	"Introduction"	In the "Features" section, updated the description of features not supported and added additional information about the 64MB limit.
1.0	January 2011	All	Initial Release

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Preface

About This Manual

This document describes the operation of the External Memory Interface (EMIF16) module in the KeyStone DSP family (refer to the device data manual for applicability to a particular part). The EMIF16 module is accessible across all the cores and all system masters that are not cores.

Notational Conventions

This document uses the following conventions:

- Commands and keywords are in **boldface** font.
- Arguments for which you supply values are in *italic* font.
- Terminal sessions and information the system displays are in `screen font`.
- Information you must enter is in **`boldface screen font`**.
- Elements in square brackets ([ ]) are optional.

Notes use the following conventions:

Note—Means reader take note. Notes contain helpful suggestions or references to material not covered in the publication.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

CAUTION—Indicates the possibility of service interruption if precautions are not taken.

WARNING—Indicates the possibility of damage to equipment if precautions are not taken.

Related Documentation from Texas Instruments

TMS320C6000 DSP and Instruction Set Reference Guide	SPRU189
TMS320C6000 Programmer's Guide.	SPRU198
TMS320C6000 Code Composer Studio Forum	Forum
C66x CorePac User Guide	SPRUGW0

Trademarks

Chapter 1

Introduction

This manual describes the External Memory Interface peripheral utilizing a 16-bit bus (EMIF16). This manual describes the purpose, features, architecture, operating modes, and registers of the EMIF16.

This chapter provides the following information:

1.1 Purpose of the Peripheral

The EMIF16 module is intended to provide a glue-less interface to a variety of asynchronous memory devices like ASRAM, NOR and NAND memory. A total of 256M bytes of any of these memories can be accessed at any given time via four chip selects with 64M byte access per chip select. NOR Flash can be used for boot purposes. These memories can also be used for Data Logging purposes.

Synchronous memories such as DDR1 SDRAM, SDR SDRAM and Mobile SDR are not supported. Refer to the data manual for a particular KeyStone part for information on the number of instances of this peripheral supported.

1.2 Features

The EMIF16 module supports the following features:

- Up to 256MB asynchronous address range over 4 chip selects
- 8-bit and 16-bit data widths
- Programmable cycle timings for each chip select
- Extended wait support (if available model supports)
- Select Strobe mode support (if available model supports)
- Page/Burst mode read support for NOR Flash
- 1-bit ECC for 8-bit and 16-bit NAND Flash (Does not support error correction)
- 4-bit ECC for 8-bit and 16-bit NAND Flash (Does not support error correction)
- Big and little endian operation

The EMIF16 module does not support the following features:

- Synchronous devices such as SDR DRAM, DDR1 SDRAM and Mobile SDR
- 32-bit mode operation
- OneNAND and PCMCIA interfaces
- NAND Flash that requires chip select to stay low during $\mathbf{t_R}$ time for reads

Note—The 64MB limit per chip select applies only for asynchronous memories that use the EMIF16 address bus for addressing - typically ASRAM and NOR flash. NAND flash uses the data bus as a multiplexed data/address bus and does not use EMIF16 address pins for addressing (Only CLE and ALE signals use the address bus. Refer to Section 3.1 "NAND Flash Mode" for more details). So NAND Flash > 64MB can be supported on one chip select.

Chapter 2

Architecture

This chapter contains the following topics:

2.1 EMIF16 Signal Descriptions

A basic block diagram of the EMIF16 asynchronous interface is shown in Figure 2-1. Table 2-1 below lists the asynchronous signals of the EMIF16 module.

Figure 2-1 Basic Block diagram for EMIF16

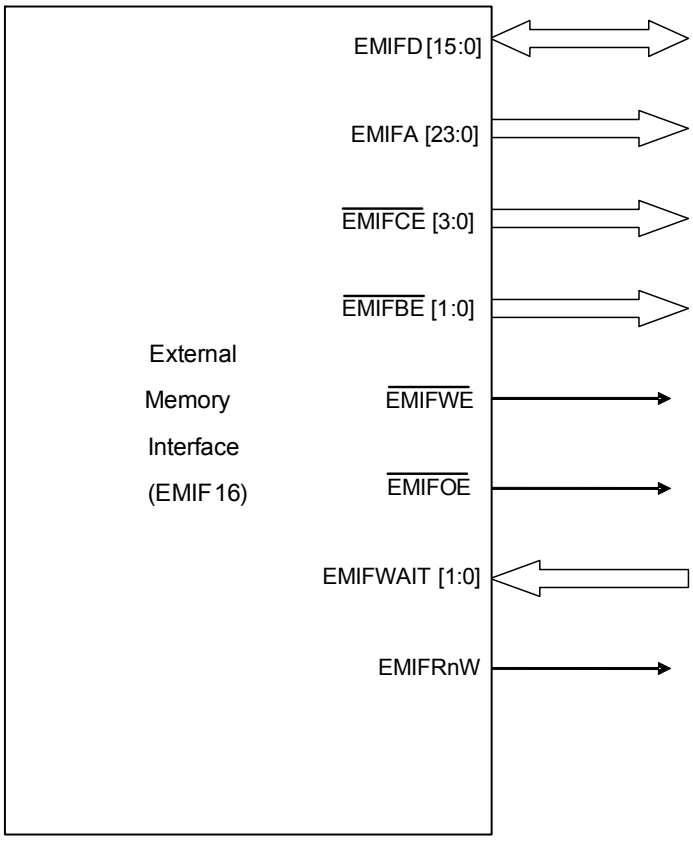


Table 2-1 EMIF16 Signal Descriptions

Pin	Description
EMIFD [15:0]	Data I/O. Input for data reads and output for data writes.
EMIFA [23:0]	External address output.
EMIFCE0	External CE0 chip select. Active-low chip select for CE space 0.
EMIFCE1	External CE1 chip select. Active-low chip select for CE space 1.
EMIFCE2	External CE2 chip select. Active-low chip select for CE space 2.
EMIFCE3	External CE3 chip select. Active-low chip select for CE space 3.
EMIFBE[1:0]	Byte enables.
EMIFWAIT [1:0]	Used to insert wait states into the memory cycle.
EMIFWE	Write enable - active low during a write transfer strobe period
EMIFOE	Output enable-active low during the entire period of a read access.
EMIFRnW	Read-write enable
End of Table 2-1	

2.2 Memory Organization

For information describing the device memory organization, see the device-specific data manual.

2.3 Supported Modes

The EMIF16 module supports asynchronous interface with ASRAM, NAND and NOR.

2.4 Configuring the EMIF16 for Asynchronous Access

EMIF16 can operate in the following modes:

- WE Strobe Mode
- Select Strobe Mode

EMIF16 is clocked at CPU/6 frequency. So, for a device running at 1GHz, EMIF16 is clocked at 166.67 MHz. All references to clock/clock cycles are in terms of EMIF16 clock cycles.

In WE Strobe mode, the byte enables $\overline{\text{EMIFBE}}$[1:0] can be used as write strobes for the current active chip select space. The $\overline{\text{EMIFCEx}}$ (x=0,1,2,3) chip select signal will remain active throughout the duration of the asynchronous access. The main advantage of this mode is that it allows two 8-bit devices to be connected to the same chip select. In this mode, the bytes enables are connected to the write strobes of the two 8-bit devices. WE strobe mode is the default mode supported on CE3. WE strobe mode is not supported for CE0 - 2.

The Select Strobe (SS) mode is activated by setting the 'ss' bit in the Async Config Register for the chip select under consideration. There is one Async Config Register for each chip select. For more details on the Async Config Register, refer to Section 4.4. In SS mode, the chip select acts as the strobe signal. So the chip select $\overline{\text{EMIFCEx}}$ will follow $\overline{\text{EMIFOE}}$ for reads and $\overline{\text{EMIFWE}}$ for writes and is active only during the strobe period. $\overline{\text{EMIFBE}}$[1:0] act as byte enables. SS mode is supported for all 4 chip selects.

WE strobe mode cannot be used along with Select Strobe mode. Select Strobe mode overrides WE Strobe mode.

EMIF16 also supports an Extended Wait mode that allows the device to extend the strobe period beyond strobe cycles during an asynchronous access. Refer to Section 3.8 for more details on Extended Wait mode.

2.5 ASRAM/NOR Flash Interface

EMIF16 connection diagrams for 16-bit and 8-bit SRAM/NOR Flash connected to chip select0 are shown in Figure 2-2 & Figure 2-3 respectively.

Figure 2-2 Connecting to 16-bit ASRAM (see note below)

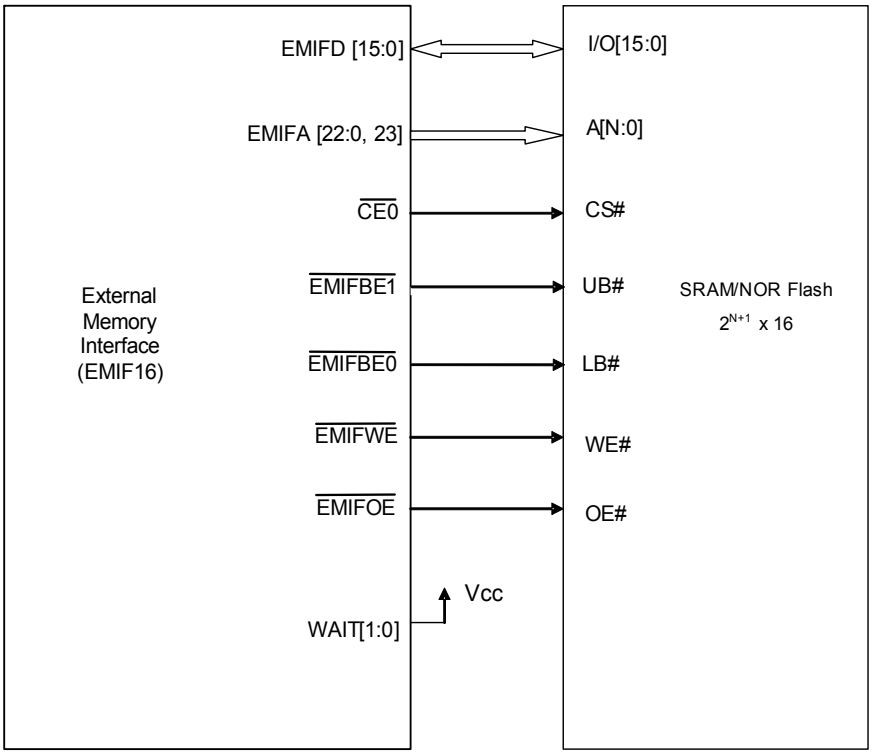
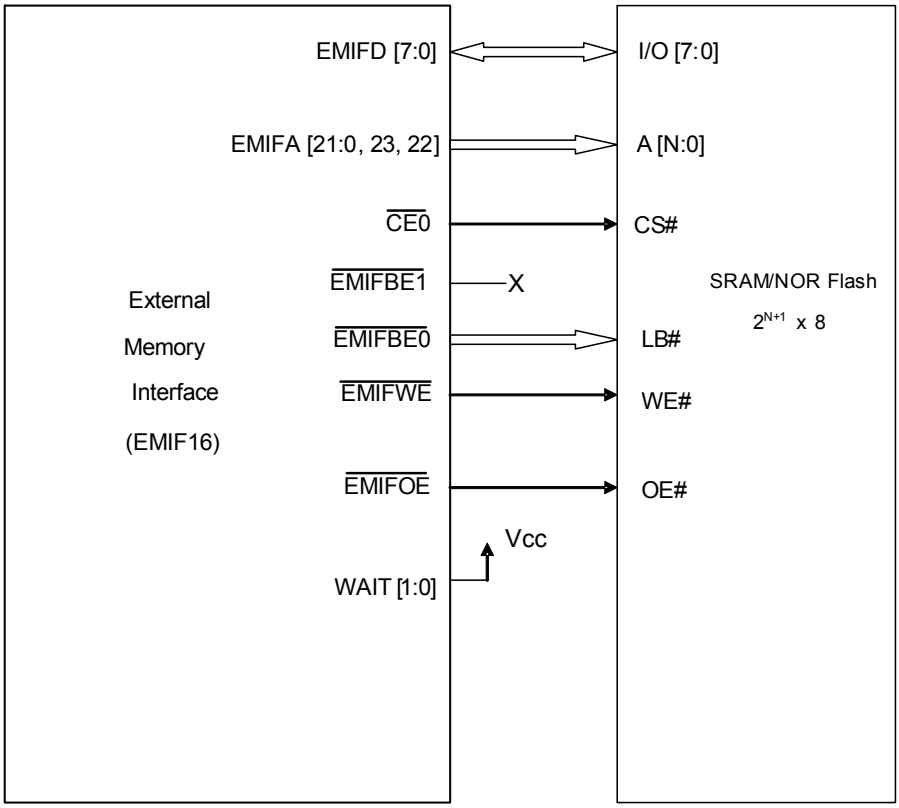


Figure 2-3 Connecting to 8-bit ASRAM



Note—EMIFA[23:22] behave as address selects. For 16-bit interface, EMIFA23 is connected to address pin A0 of the ASRAM/NOR Flash. For 8-bit interface, EMIFA[23:22] are connected to address pins A[1:0] of the ASRAM/NOR Flash.

2.5.1 EMIF16 Signal Description – ASRAM/NOR Flash

Table 2-2 ASRAM/NOR Flash Interface Signals

EMIF16 Pin	ASRAM Pin	Description
EMIFD [15:0] /EMIFD[7:0]	I/O [15:0]/ I/O[7:0]	Data I/O pins. 16/8-bit bidirectional data path for I/O.
EMIFA [23:0]	A[N:0]	External address outputs.
$\overline{\text{EMIFCE}}$[3:0]	CS#	Chip select for CE space. Active-low chip select for memory spaces 0 to 3.
$\overline{\text{EMIFBE}}$[1:0]	UB#/LB#	Active-low byte enables (Upper and lower). Individual bytes or half-words can be selected.
$\overline{\text{EMIFOE}}$	OE#	Active-low output enable. Low during read access period.
$\overline{\text{EMIFWE}}$	WE#	Active-low write enable. Low during write transfer strobe period.
EMIFRnW	—	Read-write enable.
End of Table 2-2		

$\overline{\text{EMIFCE}}$, $\overline{\text{EMIFWE}}$, $\overline{\text{EMIFOE}}$, $\overline{\text{EMIFBE}}$[1:0] are the control signals that determine the start and end of the read/write cycles. Figure 2-4 and Figure 2-5 show reads and writes initiated by different control signals.

For writes, EMIFCE, EMIFWE, EMIFBE[1:0] must be active in order to initiate a write cycle. Active status of these control signals for write is defined as EMIFCE = LOW, EMIFWE = LOW and EMIFBE1 = LOW and/or EMIFBE0 = LOW. If any one of these goes inactive, the write cycle will be terminated.

For reads, EMIFCE = LOW, EMIFWE = HIGH, EMIFOE = LOW, EMIFBE1 = LOW and/or EMIFBE0 = LOW in order to successfully initiate a read cycle. Any of these signals going inactive will terminate the read cycle.

The data input setup and hold timing must be referenced to the edge of the signal that initiates or terminates a read or write. The truth table in Table 2-3 shows various control signals and the resulting operating mode.

2.5.2 Programmable EMIF16 Parameters

EMIF16 module allows the user to program various parameters for all four chip selects:

- **Setup** - Time between the beginning of a memory cycle (chip select low, address valid) and the activation of read or write strobe. Minimum value is 1 (0 treated as 1).
- **Strobe** - Time between the activation and deactivation of the read (EMIFOE) or write (EMIFWE) strobe. Minimum value is 1 (0 treated as 1).
- **Hold** - Time between the deactivation of the read or write strobe and the end of the cycle (which may be either an address change or the deactivation of the chip select signal. Minimum value is 1 (0 treated as 1).
- **Turnaround** - Cycles between the end of one asynchronous memory access and the start of another asynchronous memory access minus one cycle. This delay is not incurred between a read followed by read or a write followed by a write to same chip select.
- **Data width** - Width of the asynchronous device's data bus (8/16-bit).

The setup, strobe and hold parameters are in terms of EMIF16 clock cycles. Note that EMIF16 is clocked at CPU/6 (166.67 MHz for 1 GHz CPU frequency). The setup, strobe and hold values for reads can be calculated as follows (assume CPU=1 GHz).

Determine the read cycle time from device datasheet (tRC). Now tRC = r_setup + r_strobe + r_hold. For example, if tRC = 86ns, 86 = r_setup + r_strobe + r_hold. Since each of the 3 parameters are in terms of CPU/6, (86/6) = r_setup + r_strobe + r_hold. This should be rounded off to the next higher integer, in this case 15. Determine from the memory device datasheet timing diagrams what each of the 3 parameters should be. After rounding off, always add the extra memory cycle(s) to the strobe. Similarly, w_setup, w_strobe and w_hold can be determined.

2.5.3 EMIF16 Truth Table

Table 2-3 Control Signal Truth Table (Part 1 of 2)

EMIFCE	EMIFWE	EMIFOE	EMIFBE[1]	EMIFBE[0]	I/O	Operating Mode
H	X	X	X	X	High-Z	Deselect/Power Down
X	X	X	H	H	High-Z	Deselect/Power Down
L	H	L	L	L	Data In on EMIFD[15:0]	Read
L	H	L	H	L	Data In on EMIFD[7:0]	Read
L	H	L	L	H	Data In on EMIFD[15:8]	Read
L	H	H	L	L	High-Z	Output disabled

Table 2-3 Control Signal Truth Table (Part 2 of 2)

EMIFCE	EMIFWE	EMIFOE	EMIFBE[1]	EMIFBE[0]	I/O	Operating Mode
L	H	H	L	H	High-Z	Output disabled
L	H	H	H	L	High-Z	Output disabled
L	L	X	L	L	Data Out on EMIFD[15:0]	Write
L	L	X	H	L	Data Out on EMIFD[7:0] High-Z EMIFD[15:8]	Write
L	L	X	L	H	Data Out on EMIFD[15:8] High-Z on EMIFD[7:0]	Write
End of Table 2-3						

2.5.4 Switching Waveforms

This section describes the read and write asynchronous cycles and associated switching waveforms for different operating modes.

2.5.4.1 Asynchronous Reads

An asynchronous read cycle proceeds as follows (see Note— 1 and 2 below):

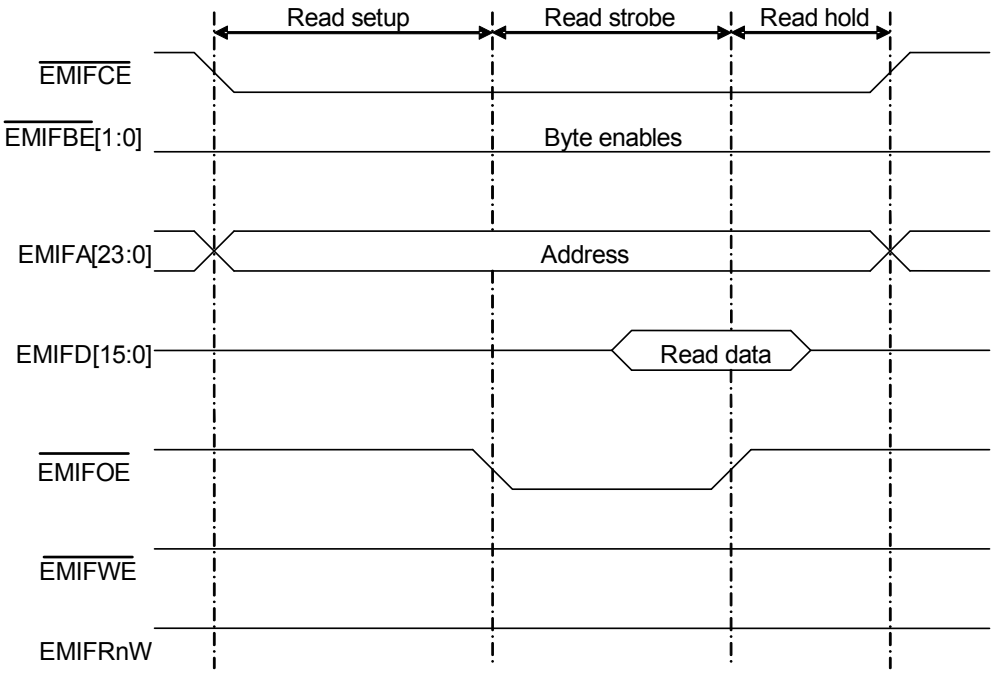
- At the start of the setup period:
  - Setup, strobe, and hold values are set according to the R_SETUP, R_STROBE, and R_HOLD values programmed in the Async 1/2/3/4 Config Register
  - EMIFCE becomes active (LOW) if not already active from previous asynchronous access
  - EMIFBE1/EMIFBE0 become active (LOW)
  - Address on address lines EMIFA[23:0] become valid
- At the start of the strobe period, EMIFOE becomes active (LOW).
- At the start of the hold period:
  - EMIFOE becomes inactive (HIGH)
  - Data is sampled on clock rising edge concurrent with the beginning of the hold period (and end of strobe)
- At the end of the hold period:
  - EMIFCE goes inactive (HIGH) only if no read/write access to the chip select space is still pending.
  - EMIFBE[1:0] become inactive.
  - Address on address lines EMIFA[23:0] become invalid.

Note—1: In case an asynchronous request cannot be serviced in a single asynchronous access cycle, multiple cycles will be needed to complete the single read or write request. In this case, the EMIF16 enters the setup phase directly without incurring turnaround cycles.

Note—2: If the entire read or write access has completed and there are more requests pending, the EMIF16 enters turnaround state and waits for programmed turnaround cycles.

The read cycle as described above is shown in the Figure 2-4. Refer to device datasheet for timing characteristics.

Figure 2-4 Asynchronous Read Timing Diagram



2.5.4.2 Asynchronous Writes

An asynchronous write cycle proceeds as follows (see Note— 1, 2 below):

- At the start of the setup period:
  - Setup, strobe and hold values are set according to the W_SETUP, W_STROBE and W_HOLD values programmed in the Async 1/2/3/4 Config Register
  - EMIFCE becomes active, if not already active from a previous access.
  - EMIFBE[1:0] become valid
  - Address on address lines on EMIFA[23:0] become valid.
  - Data on EMIFD[15:0] is driven
  - EMIFRnW becomes active (LOW).
- At the start of the strobe period, EMIFWE becomes active.
- At the start of the hold period, EMIFWE becomes inactive.
- At the end of the hold period
  - Address on address lines EMIFA[23:0] become invalid.
  - EMIFD[15:0] becomes inactive.
  - EMIFCE becomes inactive (if no additional read/write accesses to the same chip select space are pending).

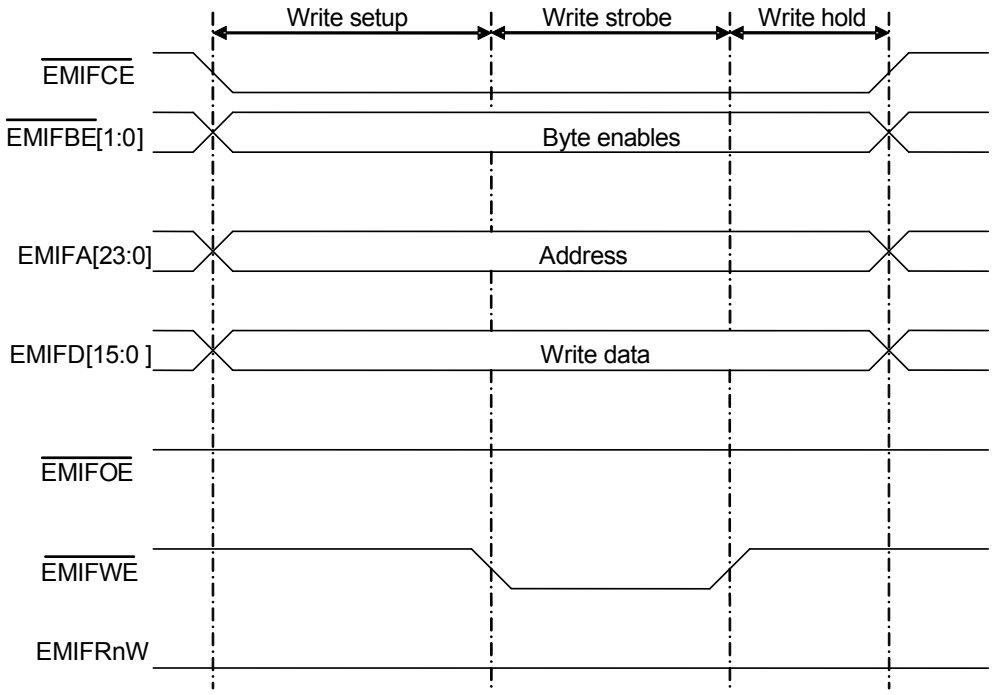
Bus contention is addressed by having a programmable turnaround time inserted between back-to-back accesses to the same or different CE spaces (See Section 2.5.2 for turnaround cycles).

Note—1: In case an asynchronous request cannot be serviced in a single asynchronous access cycle, multiple cycles are needed to complete the single read or write request. In this case, the EMIF16 enters the setup phase directly without incurring turnaround cycles.

Note—2: If the entire read or write access has completed and there are more requests pending, the EMIF16 enters turnaround state and waits for programmed turnaround cycles.

Figure 2-5 shows a write cycle initiated as described above. Refer to the device datasheet for timing characteristics.

Figure 2-5 Asynchronous Write Timing Diagram



2.5.5 Select Strobe Mode

The Select Strobe (SS) Mode is selected when the 'ss' bit in Async Wait Cycle Config Register (AWCCR) is set to '1'. SS mode overrides the WE strobe mode when 'ss' = 1.

In SS mode, $\overline{\text{EMIFBE}}$[1:0] act as byte enables. However the chip select $\overline{\text{EMIFCE}}$ behaves as the strobe and is active only during the strobe period.

2.5.5.1 Asynchronous Reads in SS Mode

An asynchronous read cycle in SS mode proceeds as follows (see Note— 1, 2 below):

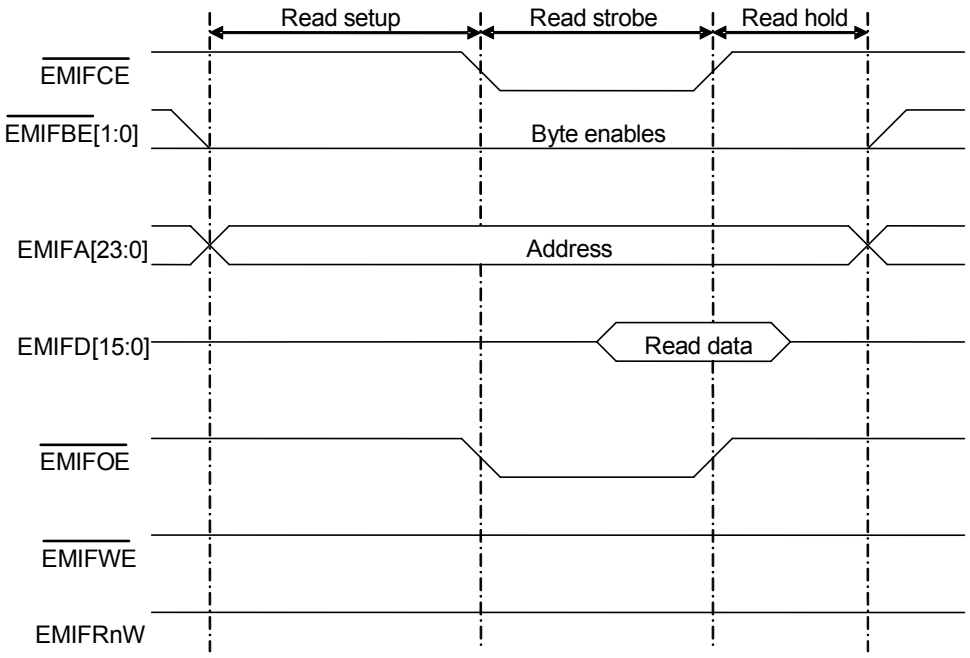
- At the start of the setup period:
  - Setup, strobe and hold values are set according to the R_SETUP, R_STROBE and R_HOLD values programmed in the Async 1/2/3/4 Config Register
  - $\overline{\text{EMIFBE}}$[1:0] become active (LOW) as byte enables
  - Address on address lines EMIFA[23:0] become valid
- At the start of the strobe period, $\overline{\text{EMIFCE}}$ and $\overline{\text{EMIFOE}}$ become active (LOW) at the same time.
- At the start of the hold period:
  - $\overline{\text{EMIFCE}}$ and $\overline{\text{EMIFOE}}$ become inactive (HIGH).
  - Data is sampled on clock rising edge concurrent with the beginning of the hold period (and end of strobe)
- At the end of the hold period:
  - $\overline{\text{EMIFBE}}$[1:0] become inactive.
  - Address on address lines EA[23:0] become invalid.

Note—1: In case an asynchronous request cannot be serviced in a single asynchronous access cycle, multiple cycles will be needed to complete the single read or write request. In this case, the EMIF16 enters the setup phase directly without incurring turnaround cycles.

Note—2: If the entire read or write access has completed and there are more requests pending, the EMIF16 enters turnaround state and waits for programmed turnaround cycles.

Figure 2-6 shows the switching waveform for asynchronous reads in SS mode. Refer to the device datasheet for device timing specifications.

Figure 2-6 Asynchronous Read Cycle (Select Strobe mode)



2.5.5.2 Asynchronous Writes in SS Mode

An asynchronous write cycle proceeds as follows (see Note— 1, 2):

- At the start of the setup period:
  - Setup, strobe and hold values are set according to the W_SETUP, W_STROBE and W_HOLD values programmed in the Async 1/2/3/4 Config Register
  - $\overline{\text{EMIFBE}}$[1:0] become valid
  - Address on address lines on EMIFA[23:0] become valid.
  - Data on EMIFD[15:0] is driven
  - EMIFRnW becomes active (LOW).
- At the start of the strobe period, $\overline{\text{EMIFCE}}$ and $\overline{\text{EMIFWE}}$ become active.
- At the start of the hold period, $\overline{\text{EMIFCE}}$ and $\overline{\text{EMIFWE}}$ become inactive.
- At the end of the hold period:
  - Address on address lines EMIFA[23:0] become invalid.
  - EMIFD[15:0] becomes invalid.

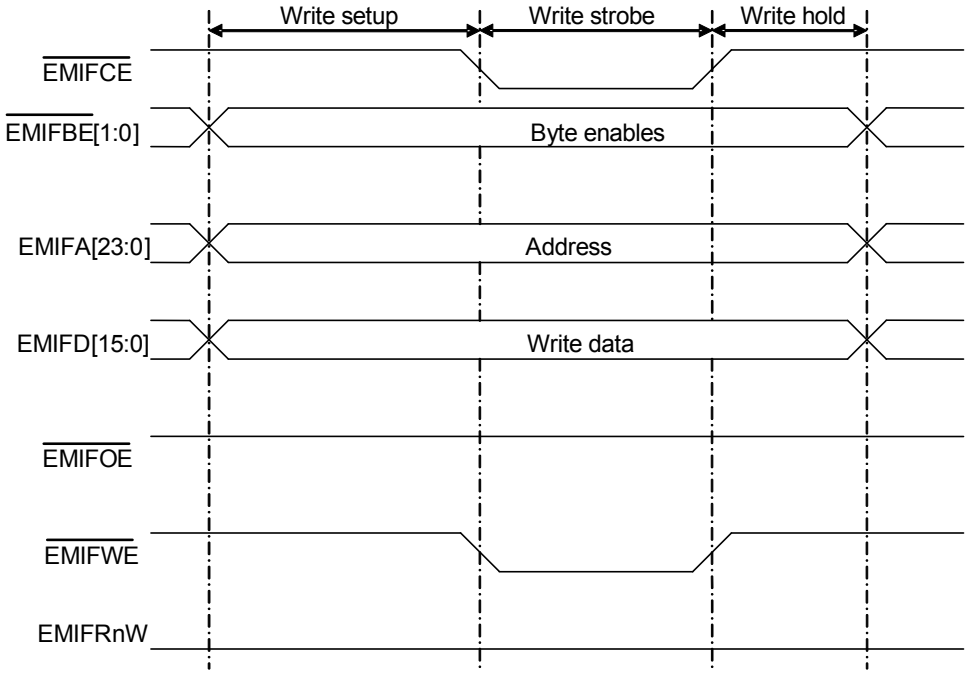
Note—[1] In case an asynchronous request cannot be serviced in a single asynchronous access cycle, multiple cycles will be needed to complete the single read or write request. In this case, the EMIF16 enters the setup phase directly without incurring turnaround cycles.

Note—[2] If the entire read or write access has completed and there are more requests pending, the EMIF16 enters turnaround state and waits for programmed turnaround cycles.

Bus contention is addressed by having a programmable turnaround time inserted between back-to-back accesses to the same or different CE spaces (See Section 2.5.2 for turnaround cycles).

Figure 2-7 shows the switching waveform for asynchronous writes in SS mode. Refer to the device datasheet for device timing specifications.

Figure 2-7 Write Cycle (Select Strobe Mode)



2.5.6 WE Strobe Mode

In the WE strobe mode (Figure 2-8), the byte enables act as write strobes. This mode is useful for combining two 8-bit devices to create a 16-bit data bus, allowing the EMIF16 to perform byte writes to two 8-bit devices which do not have byte enable inputs. In WE strobe mode, the byte enables are connected to the write strobes of the 8-bit devices. This mode cannot be used with the Select strobe (SS) mode as SS mode overrides WE strobe mode. WE strobe mode is supported only on CE3.

Figure 2-8 Asynchronous Writes (WE Strobe Mode)

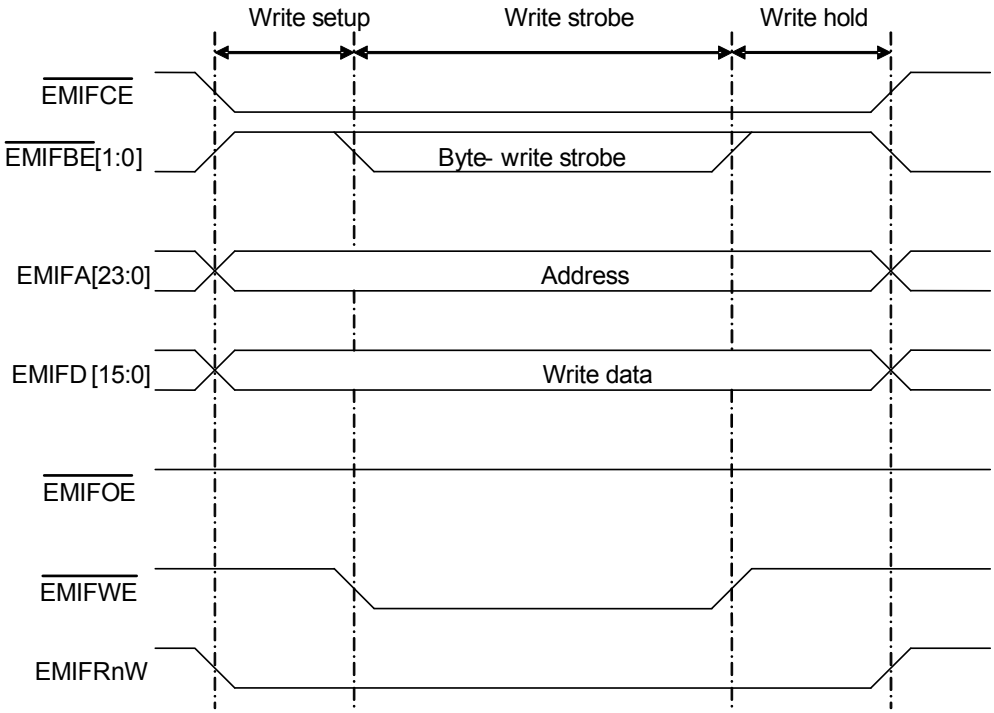
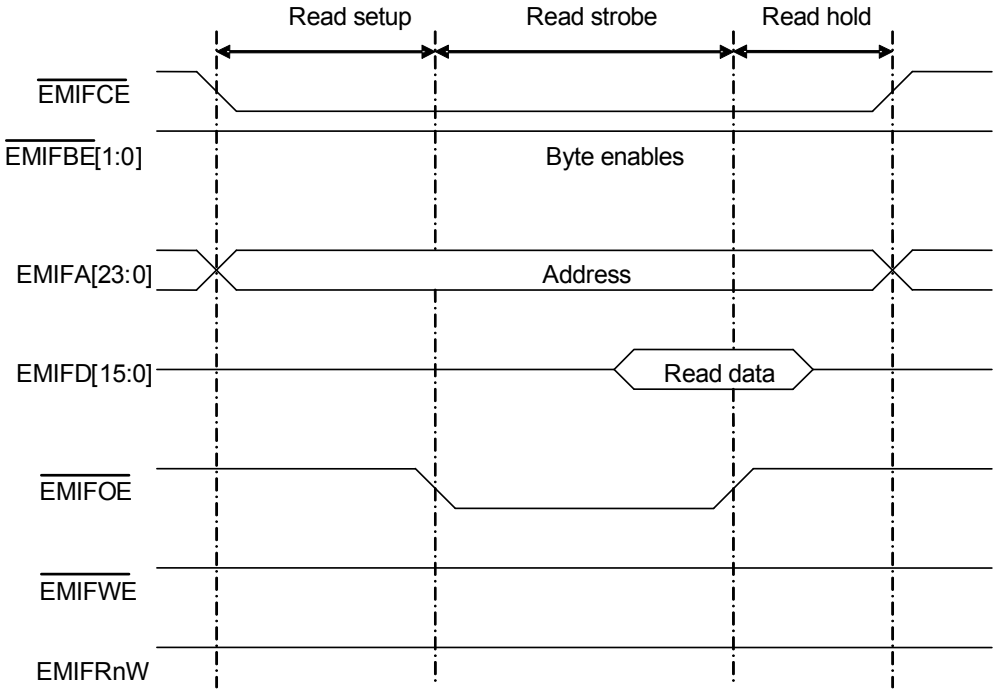


Figure 2-9 Asynchronous Reads (WE Strobe Mode)



Chapter 3

Operating Modes

This chapter describes the following topics:

3.1 NAND Flash Mode

EMIF16 supports NAND Flash mode. To enable NAND flash mode, the corresponding chip select's **csN_use_nand** bit must be set in the NAND Flash Control Register (NANDFCR). The NAND Flash timing values must be programmed in the chip select's Async Configuration Register. For more details on these registers refer to Registers.

NAND Flash mode also supports both 1-bit and 4-bit error correction code (ECC) calculation. 4-bit ECC can only be used for one chip select at a time. See Section 3.7 for details on ECC functionality and support.

A NAND access cycle consists of command, address and data phases in order to complete a NAND Flash transfer. All NAND Flash operations can be divided into single asynchronous cycles which can be executed using software.

The following sections describe connecting to a NAND Flash device, configuring EMIF16 registers for NAND Flash mode, command set, ECC support and so on.

3.1.1 Connecting to NAND Flash

Figure 3-1 and Figure 3-2 show how to connect to 8-bit and 16-bit NAND Flash respectively.

Figure 3-1 Connecting to 8-bit NAND Flash

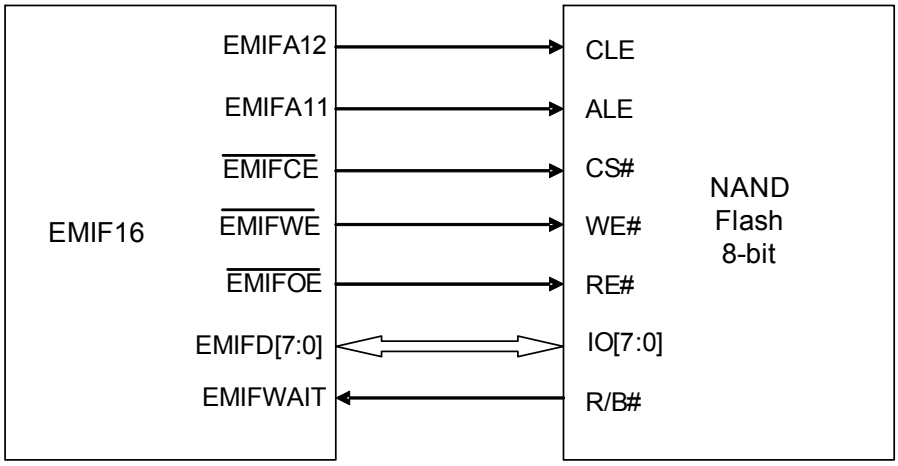
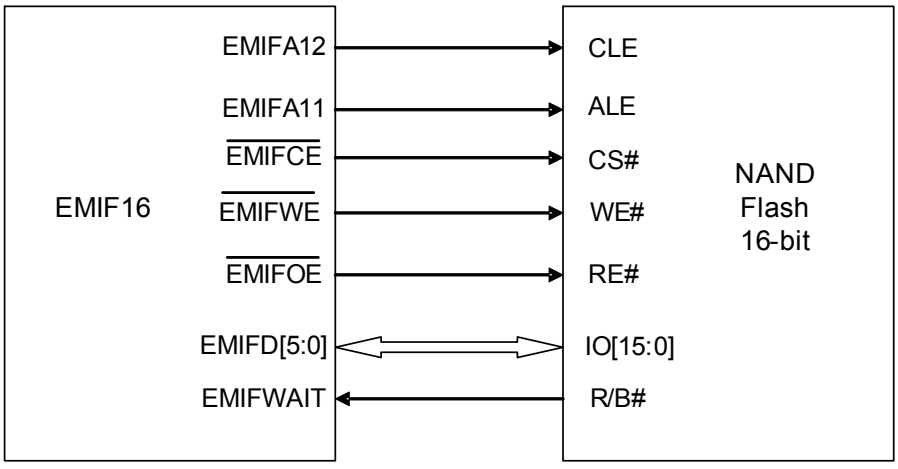


Figure 3-2 Connecting to 16-bit NAND Flash



3.2 Configuring EMIF16 in NAND Flash Mode

EMIF16's memory-mapped registers must be programmed to configure NAND mode. In addition to configuring the fields in the Async Config Register for the chip select under consideration, the NAND Flash Control Register (NANDFCR) also needs to be configured.

Note—Due to legacy considerations, CS2 will refer to chip select 0 (CE0), CS3 will refer to chip select 1(CE1), CS4 will refer to chip select 2(CE2) and CS5 will refer to chip select 3(CE3) in this document.

3.3 EMIF16 Signal Description – NAND Flash

NAND Flash devices have a single multiplexed path for command, address and data phases of the access cycle. The control signals Address Latch Enable (ALE), Command Latch Enable (CLE), Chip Select (CS#), Write Enable (WE#) and Read Enable (RE#) are used by the NAND to distinguish between command, address, and data-read/write phases.

Table 3-1 describes signals that define the NAND Flash interface.

Table 3-1 NAND interface signal description

NAND Flash Pin	Type	Description
ALE	Input	During the time ALE is HIGH, address information is transferred from EMIFD[7:0] to on-chip address register upon a LOW-HIGH transition on WE#. When address information is not being latched, ALE should be driven low.
CLE	Input	During the time CLE is HIGH, information is transferred from EMIFD[7:0] to on-chip command register on rising edge of $\overline{\text{EMIFWE}}$. When command information is not being latched, CLE should be driven low.
CS#	Input	Chip Select. Gates transfers between host and NAND Flash.
WE#	Input	Gates transfers from host to NAND device.
RE#	Input	Gates transfers from NAND device to host.
IO[15:0]/IO[7:0]	I/O	Bidirectional pins: Used to transfer command, data and address information between host and NAND device.
R/B#	Output	Read/Busy pin: Used to indicate if NAND device is busy performing a PROGRAM or ERASE operation.
End of Table 3-1		

3.4 Using ALE and CLE

If using EMIFA11 and EMIFA12 as ALE and CLE respectively for CE0, choose the following addresses. The base address for CE0 space is 0x70000000.

Table 3-2 CE0 Addressing when EMIFA11 and EMIFA12 are used as ALE and CLE respectively

Address	ALE	CLE	Phase
0x7000 0000	LOW	LOW	Data Phase
0x7000 2000	HIGH	LOW	Address Phase
0x7000 4000	LOW	HIGH	Command Phase
End of Table 3-2			

The base addresses for chip selects CE1, CE2 and CE3 are 0x7400 0000, 0x7800 0000 and 0x7C00 0000 respectively. The addresses for ALE and CLE can thus be derived for CE1-3 spaces as well.

During the command phase, a command on EMIFD[7:0] is latched into the device's internal command register. During the address phase, an address on EMIFD[7:0] is latched into the device's internal address register. During the data phase, data on EMIFD[15:0] is read out off or latched into the device's internal data register for reads and writes respectively.

3.5 NAND Read and Program Operations

A NAND access cycle is composed of multiple single asynchronous cycles that must be executed by software. The chip select does not remain active for the entire duration of the access, but becomes inactive during the period between two asynchronous cycles. After a read command is issued, it takes time t_R for the read data to be driven on the IO pins.

Note—Since chip select is inactive during this time, EMIF16 does not support NAND devices that require the chip select to be low during t_R.

Each NAND operation starts off with issuing a command cycle. The command is placed on EMIFD[7:0], chip select $\overline{\text{EMIFCE}}$ is driven low and CLE goes high. Write enable $\overline{\text{EMIFWE}}$ behaves as a clock – commands, address, or data are clocked into the NAND device on the rising edge of $\overline{\text{EMIFWE}}$.

Most commands require multiple address cycles followed by a second command cycle. While the NAND is busy carrying out a Program/Erase operation a new command should not be issued until the NAND device is ready to accept new commands. See Section 3.6 for details. The exceptions to this are the RESET and READ STATUS commands which can be issued even when the NAND device is busy. The READ STATUS command is used to obtain the 'ready' status of the device.

For specific details on command cycle, address cycles, and data read/write phases refer to the device datasheet.

3.6 Checking the Status of Operation

The NAND Flash status register (NANDFSR) can be used to check the status of the WAIT pin while in NAND Flash Mode. This is accomplished by connecting the WAIT pin to the R/B# pin. For reads, the R/B# signal goes low and remains low while the NAND Flash retrieves the data requested. R/B# signal goes high to indicate that the data requested by the EMIF16 is ready to be read. During a write/program operation, the R/B# goes low and remains low while the NAND Flash programs the device with the write data from the EMIF16. Once the device is free to accept the next transaction, the R/B# signal goes high. Thus, software can use the NANDFSR to determine the status of the Flash device and determining when to submit the next transaction. The Wait Rise (WR) interrupt in the Interrupt Raw Register (IRR) can also be used to check for a rising edge on the appropriate WAIT pin. For details on interrupt support and handling refer to Section 3.10.

3.7 ECC Support

For data integrity purposes, NAND Flash supports ECC. EMIF16 supports 1-bit ECC calculation for up to 512 Bytes and 4-bit ECC calculation for up to 518 Bytes.

1-bit ECC calculation for NAND device connected to a specific chip select is set off by writing a '1' to the CSN_ECC_START bit of the NAND Flash Control Register (NANDFCR). 1-bit ECC calculation for each chip select is independent of other chip selects. Once the 1-bit ECC is calculated for a chip select, it can be read from the corresponding chip select's NAND Flash 1-bit ECC Register. Reading this register clears the CSN_ECC_START bit. Software is responsible for initiating the ECC calculation before starting to write or read data from the NAND Flash.

It is also the responsibility of the software to read the calculated 1-bit ECC from the NAND Flash 1-Bit ECC register for the corresponding chip select after writing or reading the required number of data bytes from the NAND Flash. If the software writes or reads greater than 512 bytes before reading the NAND Flash ECC register, the value of the 1-bit ECC will be incorrect.

Figure 3-3 shows how 1-bit ECC calculation is performed on a 512 Byte block of data for an 8-bit NAND Flash device.

Figure 3-3 1-bit ECC calculation for 8-bit NAND device

<table>
<tr><td>Byte 1</td><td>Bit0</td><td>Bit1</td><td>Bit2</td><td>Bit3</td><td>Bit4</td><td>Bit5</td><td>Bit6</td><td>Bit7</td><td>p8e</td><td>p16e</td><td rowspan="4">p32e</td><td rowspan="13">…</td><td rowspan="5">p2048e</td></tr>
<tr><td>Byte 2</td><td>Bit0</td><td>Bit1</td><td>Bit2</td><td>Bit3</td><td>Bit4</td><td>Bit5</td><td>Bit6</td><td>Bit7</td><td>p8o</td></tr>
<tr><td>Byte 3</td><td>Bit0</td><td>Bit1</td><td>Bit2</td><td>Bit3</td><td>Bit4</td><td>Bit5</td><td>Bit6</td><td>Bit7</td><td>p8e</td><td>p16o</td></tr>
<tr><td>Byte 4</td><td>Bit0</td><td>Bit1</td><td>Bit2</td><td>Bit3</td><td>Bit4</td><td>Bit5</td><td>Bit6</td><td>Bit7</td><td>p8o</td></tr>
<tr><td>.
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.</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td rowspan="8">p2048o</td></tr>
<tr><td>Byte 509</td><td>Bit0</td><td>Bit1</td><td>Bit2</td><td>Bit3</td><td>Bit4</td><td>Bit5</td><td>Bit6</td><td>Bit7</td><td>p8e</td><td>p16e</td><td rowspan="4">p32o</td></tr>
<tr><td>Byte 510</td><td>Bit0</td><td>Bit1</td><td>Bit2</td><td>Bit3</td><td>Bit4</td><td>Bit5</td><td>Bit6</td><td>Bit7</td><td>p8o</td></tr>
<tr><td>Byte 511</td><td>Bit0</td><td>Bit1</td><td>Bit2</td><td>Bit3</td><td>Bit4</td><td>Bit5</td><td>Bit6</td><td>Bit7</td><td>p8e</td><td>p16o</td></tr>
<tr><td></td><td>Bit0</td><td>Bit1</td><td>Bit2</td><td>Bit3</td><td>Bit4</td><td>Bit5</td><td>Bit6</td><td>Bit7</td><td>p8o</td></tr>
<tr><td>Byte 512</td><td>p1o</td><td>p1e</td><td>p1o</td><td>p1e</td><td>p1o</td><td>p1e</td><td>p1o</td><td>p1e</td></tr>
<tr><td></td><td colspan="4">p20</td><td colspan="2">p2e</td><td colspan="2">p20</td><td colspan="2">p2e</td></tr>
<tr><td></td><td colspan="6">p4o</td><td colspan="4">p4e</td></tr>
</table>

In the figure, p1e through p4e are column parities and p8e through p2048e are row parities. This algorithm can be easily extended for 16-bit NAND device. For 16-bit device, column parities will run from p1e through p8e whereas row parities will run from p16e through p2048e.

Note that the above figure applies only for 512 Byte data. To calculate 1-bit ECC for 8-bit NAND device for data less than 512 Bytes, the corresponding parities must be ignored. For example, for 256 Bytes of data, p2048e and p2048o are unnecessary and should be discarded. Similarly, for 128 Bytes, discard p1024e, p1024o, p2048e and p2048o.

EMIF16 also provides 4-bit ECC support for up to 518 Bytes for both 8-bit and 16-bit NAND devices. However, unlike 1-bit ECC, only one chip select can be selected for 4-bit ECC calculation at one time. Chip select can be selected by setting the **4BIT_ECC_SEL** field in the NAND Flash Control Register (NANDFCR). 4-bit ECC calculation for the selected chip select can be started by setting the **4BIT_ECC_START** bit in the NANDFCR (Table 3-3). Refer to Section 4.12 for details on NANDFCR.

Table 3-3 4-bit ECC calculation bits in NAND Flash Control Register

Bit	Value	Description
4BIT_ECC_SEL	0x0	4-bit ECC calculation for CS2 (CE0)
	0x1	4-bit ECC calculation for CS3 (CE1)
	0x2	4-bit ECC calculation for CS4 (CE2)
	0x3	4-bit ECC calculation for CS5 (CE3)
4BIT_ECC_START	0x1	Start 4-bit ECC calculation for selected chip select. Bit is cleared after reading any of the NAND Flash 4-Bit ECC 1-4 registers. Writing a 0 has no effect.
End of Table 3-3		

Once 4-bit ECC calculation is complete, the calculated syndrome for reads and parity for writes can be read from the NAND Flash 4-Bit ECC 1-4 registers. On reading any of these registers, the **4BIT_ECC_START** bit is cleared. The contents of NAND Flash 4-Bit ECC 1-4 registers are cleared when 4-bit ECC calculation is started by setting **4BIT_ECC_START**.

The 4-bit ECC algorithm uses 10 bits. 4-bit ECC calculation in EMIF16 however uses 8-bit values for both 8-bit and 16-bit devices. The 8-bit value is converted to 10 bits and the upper 2 bits of the 10-bit value are zeroed out by EMIF16. Typically, spare area in NAND is used to store ECC-related information. For example, after a write, for the 10-bit parity values read from the NAND Flash 4-Bit ECC 1-4 registers to be stored in the spare area of the NAND device, 10-bit values need to be converted to 8-bit or 16-bit values depending on bus width of the device being used.

Similarly, for reads, the parity values stored in the spare location for the NAND needs to be read for further syndrome calculation. These values will be read as multiple 8-bit or 16-bit values depending on NAND bus width. The 8-bit values for either 8-bit or 16-bit NAND devices should be converted to 10-bit before writing them to the NAND Flash 4-bit ECC Load register. The 8 to 10-bit conversion and vice-versa should be done by software.

Following steps must be taken by software for 4-bit ECC calculation:

Writes

1. Start 4-bit ECC calculation:
   Set the 4BIT_ECC_START bit in the NAND Flash Control Register to 1.
2. Perform Write:
   Write 518 Bytes of data to NAND Flash.
3. Read Parity:
   Read the 10-bit parity values from NAND Flash 4-Bit ECC 1-4 registers.
4. 10-Bit to 8-Bit Conversion:
   Convert the 10-bit parity values to 8-bits or 16-bits depending on width of connected NAND Flash. This can be accomplished by concatenating the 10-bit values together and then breaking them into ten 8-bit or five 16-bit values.
5. Store Parity:
   Store the parity to spare location in the NAND Flash.

Reads

1. Start 4-bit ECC calculation:
   Set the 4BIT_ECC_START bit in the NAND Flash Control Register to 1.
2. Perform Read:
   Read 518 Bytes of data from NAND Flash.
3. Clear 4BIT_ECC_START bit:
   Clear 4BIT_ECC_START bit in NANDFCR by reading any of the NAND Flash 4-Bit ECC registers.
4. Read Parity:
   Read parity stored in the spare location of NAND Flash.
5. 8-Bit or 16-Bit to 10-Bit conversion:
   Convert 8 or 16-bit parity values to 10-bits. This can be accomplished by concatenating ten 8-bit values or five 16-bit values and then breaking them into 8 10-bit values.
6. Write Parity Values:
   Write the 10-bit parity values in the NAND Flash 4-Bit ECC Load Register.
7. Dummy Read:
   Perform a dummy read to EMIF16 Revision Code and Status Register. This ensures sufficient time for syndrome calculation after writing the ECC values in previous step.
8. Read Syndrome:
   Read syndrome from NAND Flash 4-Bit ECC 1-4 Registers. A syndrome value of 0 signifies no bit errors whereas non-zero value implies one or more errors.
   Perform the following steps in case of a non-zero syndrome.
9. Start Address Calculation:
   Set ADDR_CAL_ST bit in NANDFCR to start error address calculation.

10. Wait for State:

    Wait for CORR_STATE in the NAND Flash Status Register to be equal to 0x1, 0x2 or 0x3.

    0x1 – Five or more errors (Errors cannot be corrected).

    0x2 – Error correction complete (Errors on bit 8 and bit 9)

    0x3 – Error correction complete (error exists)

11. Read number of errors:

    The field ERR_NUM in NAND Flash Status Register gives the number of errors.

12. Read Error Address:

    Error address can be read from NAND Flash Error Address 1-2 Registers. Address for the errored word is equal to (Total words read) + 7 – Address value. So, for 518 Bytes, the address will be (518 + 7 – address value) or (525 – address value).

13. Read Error Value:

    Error value from NAND Flash Error Value 1-2 Registers can be read and corrected by XOR – ing the errored word with the error value from NAND Flash Error Value 1-2 Registers.

3.8 Extended Wait Mode

EMIF16 supports Extended Wait Mode. Extended Wait Mode allows the asynchronous device to extend the strobe period longer than the programmed number of clock cycles in the Async 1-4 Config Registers. Extended Wait Mode is enabled by setting the **EW** bit in the Async 1-4 Config Register to 1. Once **EW** has been set, the EMIF16 monitors the EMIFWAIT pin mapped to that chip select to determine if the device wants to extend the strobe period. An assertion on the EMIFWAIT pin causes the EMIF16 to insert additional clock cycles beyond the programmed value and extends the strobe period until the EMIFWAIT pin is deactivated. From here on the EMIF16 resumes normal operation.

A chip select can be mapped to either of the two pins EMIFWAIT[1:0] by appropriately setting the **CS2-5_WAIT** fields in the Async Wait Cycle Config Register (AWCCR). It is also important to correctly set the active polarity of the EMIFWAIT pins by programming the WP0-1 bits in the AWCCR. A '0' means EMIF16 will insert wait cycles when EMIFWAIT is low, and sampled high when polarity is set to 1.

The strobe period in Extended Wait Mode can only be extended up to a certain maximum number of cycles as programmed in the **MAX_EXT_WAIT** field in the AWCCR. If the EMIFWAIT pin under consideration is not deactivated by the time the counter on maximum number of clock cycles expires, EMIF16 proceeds to the hold period regardless of the state of the EMIFWAIT pin. For details on AWCCR, refer to Section 4.3. The expiration of the counter can also be used to set an asynchronous timeout interrupt. For details on how to enable this interrupt, refer to Section 3.10.

Note—In Extended Wait Mode, strobe parameters R_STROBE and W_STROBE must not be set to zero.

3.9 Data Bus Parking

The data bus is always driven to the previous write value when EMIF16 is idle. This feature is called data bus parking. EMIF16 stops driving the data bus when it issues a read command to memory. Once read is complete and EMIF16 latches the last data read, the data bus is immediately parked again.

3.10 Interrupt Support

EMIF16 generates one interrupt to the DSP. The interrupt can be generated due to:

- Asynchronous Time Out
- Rising edge on the WAIT pin

EMIF16 sets the WR bit field in the Interrupt Raw Register on rising edge of the EMIFWAIT pin. Wait polarity bits in the Async Wait Cycle Config register have no effect on the WR bit. The interrupts can be used to indicate ready status of connected NAND Flash devices to respective chip select. As mentioned, the MAX_EXT_WAIT field in the Async Wait Cycle Config Register defines the maximum number of clock cycles for which the strobe period may be extended in Extended Wait mode during which the EMIFWAIT pin must go inactive. If it does not go inactive, the EMIF16 sets the asynchronous time out bit **AT** in the Interrupt Raw Register (IRR), but continues to the hold state. For the interrupt to be enabled and sent to the DSP, the corresponding bit in the Interrupt Mask Set Register (IMSR) **AT_MASK_SET** must be set. The

interrupt can be disabled after enabling by setting the **AT_MASK_CLR** bit in Interrupt Mask Clear Register (IMCR). The enable status of the interrupt can be verified by checking the corresponding bits in the IMSR and IMCR registers. Bits in both registers will be set if enabled and will be 0 if interrupt is disabled.

The interrupt bit in IRR will be set if the interrupt condition occurs. If the interrupt has also been enabled the corresponding bits in IMR will be set. Details on interrupt status and control bits are mentioned in Table 3-4.

Table 3-4 Interrupt status and control bits

Register	Bit Field	Description
Interrupt Raw Register (IRR)	WR	Set on a rising edge on WAIT port. Writing a 1 clears WR as well as WR_MASKED bit in the IMR.
	AT	Set when asynchronous timeout occurs. Writing a 1 clears AT as well as AT_MASKED bit in IMR.
Interrupt Mask Register (IMR)	WR_MASKED	Set on a rising edge on WAIT port only if WR_MASK_SET bit in IMSR is also set.
	AT_MASKED	Set when asynchronous timeout occurs only if AT_MASK_SET bit in IMSR is also set.
Interrupt Mask Set Register (IMSR)	WR_MASK_SET	Writing a 1 enables the wait rise interrupt.
	AT_MASK_SET	Writing a 1 enables the asynchronous timeout interrupt.
Interrupt Mask Clear Register (IMCR)	WR_MASK_CLR	Writing a 1 disables the wait rise interrupt.
	AT_MASK_CLR	Writing a 1 disables the asynchronous timeout interrupt.
End of Table 3-4		

3.11 NOR Flash Page Mode

EMIF16 supports Page Mode reads for NOR Flash on asynchronous memory chip selects. Page Mode can be enabled by writing a '1' to the CSN_PG_MD_EN field in the Page Mode Control Register (PMCR) for chip selected in consideration. For more details on PMCR, refer to Section 4.4.

When page mode is enabled, the page size of the connected device must be programmed in the CSN_PG_SIZE field of the PMCR for chip select in question. Address change to valid read data timing must be programmed in the CSN_PG_DEL field of the PMCR. Other asynchronous memory timings must be programmed in the Async Config Register. For Program/Erase operations and memory organization, refer to the NOR device datasheet.

3.12 Reset Considerations

EMIF16 has two active low resets.

- Power-up reset that resets both the state machine and internal registers
- Soft reset that only resets the state machine and does not reset internal registers except for interrupt registers, CSN_ECC_START bits in NAND Flash Control Register and NAND Flash CS2-5 1-bit ECC registers.

The output enable signal is reset asynchronously. No register accesses can be performed either during power-up reset or soft reset.

Chapter 4

Registers

4.1 Registers Overview

This section details the programmable register fields within the EMIF16's configuration space that can be programmed to configure the EMIF16, and details on memory map and bit positions.

Note—Due to legacy considerations, CS2 will refer to chip select 0 (CE0), CS3 will refer to chip select 1(CE1), CS4 will refer to chip select 2(CE2) and CS5 will refer to chip select 3(CE3) in this document.

Table 4-1 lists the memory-mapped registers for the EMIF16. For the memory address of these registers, see the device-specific data manual.

Table 4-1 EMIF16 Registers

Offset	Acronym	Register Description	Section
00h	RCSR	Revision Code and Status Register	4.2
04h	AWCCR	Async Wait Cycle Config Register	4.3
10h	A1CR	Async 1 Config Register	4.4
14h	A2CR	Async 2 Config Register	4.5
18h	A3CR	Async 3 Config Register	4.6
1Ch	A4CR	Async 4 Config Register	4.7
40h	IRR	Interrupt Raw Register	4.8
44h	IMR	Interrupt Masked Register	4.9
48h	IMSR	Interrupt Mask Set Register	4.10
4Ch	IMCR	Interrupt Mask Clear Register	4.11
60h	NANDFCR	NAND Flash Control Register	4.12
64h	NANDFSR	NAND Flash Status Register	4.13
68h	PMCR	Page Mode Control Register	4.14
70h	NFECCCS2	NAND Flash CS2 (CE0) 1-Bit ECC Register	4.15
74h	NFECCCS3	NAND Flash CS3 (CE1) 1-Bit ECC Register	4.16
78h	NFECCCS4	NAND Flash CS4 (CE2) 1-Bit ECC Register	4.17
7Ch	NFECCCS5	NAND Flash CS5 (CE3) 1-Bit ECC Register	4.18
BCh	NANDF4BECCLR	NAND Flash 4-Bit ECC Load Register	4.19
C0h	NANDF4BECC1R	NAND Flash 4-Bit ECC 1 Register	4.20
C4h	NANDF4BECC2R	NAND Flash 4-Bit ECC 2 Register	4.21
C8h	NANDF4BECC3R	NAND Flash 4-Bit ECC 3 Register	4.22
CCh	NANDF4BECC4R	NAND Flash 4-Bit ECC 4 Register	4.23
D0h	NANDFEA1R	NAND Flash Error Address 1 Register	4.24
D4h	NANDFEA2R	NAND Flash Error Address 2 Register	4.25
D8h	NANDFEV1R	NAND Flash Error Value 1 Register	4.26
DCh	NANDFEV2R	NAND Flash Error Value 2 Register	4.27
End of Table 4-1			

4.2 Revision Code and Status Register (RCSR)

The Revision Code and Status register contains the revision number and identification data. It also indicates the endian mode (Figure 4-1). Refer to the device specific datasheet for the register value for your device.

Figure 4-1 Revision Code and Status Register

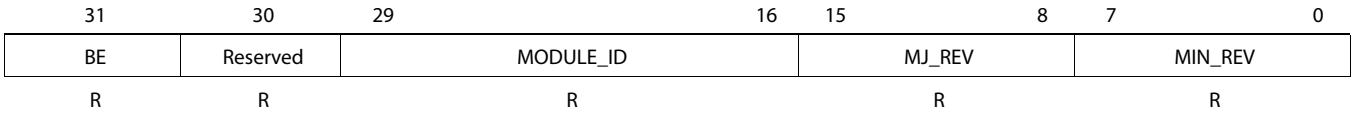

Table 4-2 Revision Code and Status Register (RCSR) Details

Bit	Field	Reset Value	Description
31	BE		Defines EMIF16 endianness. 0 – Little Endian 1 – Big Endian
30	Reserved	0x0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
29-16	MOD_ID	0x46	Module ID Bits
15-8	MJ_REV	0x4	Major Revision
7-0	MIN_REV	0x0	Minor Revision
End of Table 4-2			

4.3 Async Wait Cycle Config Register (AWCCR)

The Async Wait Cycle Config Register is as shown in Figure 4-2.

Figure 4-2 Async Wait Cycle Config Register

31	30	29	28	27 ... 24	23 ... 22	21 ... 20
Reserved	Reserved	WP1	WP0	Reserved	CS5_WAIT	CS4_WAIT
RW - 0x1	RW - 0x1	RW - 0x1	RW - 0x1	R - 0x0	RW	RW

19 ... 18	17 ... 16	15 ... 8	7 ... 0
CS3_WAIT	CS2_WAIT	Reserved	MAX_EXT_WAIT
RW	RW	R-0x0	RW-0x80

Table 4-3 Async Wait Cycle Config Register (AWCCR) Details (Part 1 of 2)

Bit	Field	Reset Value	Description
31	Reserved	0x1	Reserved. The reserved bit location is always read as 1.
30	Reserved	0x1	Reserved. The reserved bit location is always read as 1.
29	WP1	0x1	Defines the wait polarity for WAIT[1] 0 – Wait if WAIT[1] is low 1 – Wait if WAIT[1] is high
28	WP0	0x1	Defines the wait polarity for WAIT[0] 0 – Wait if WAIT[0] is low 1 – Wait if WAIT[0] is high
27-24	Reserved	0x0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
23-22	CS5_WAIT		WAIT map bits for CE3: 0x0 – WAIT[0] is used. 0x1 – WAIT[1] is used. 0x2 – Reserved. 0x3 – Reserved.
21-20	CS4_WAIT		WAIT map bits for CE2: 0x0 – WAIT[0] is used. 0x0 – WAIT[1] is used. 0x0 – Reserved. 0x0 – Reserved.
19-18	CS3_WAIT		WAIT map bits for CE1: 0x0 – WAIT[0] is used. 0x0 – WAIT[1] is used. 0x0 – Reserved. 0x0 – Reserved.
17-16	CS2_WAIT		WAIT map bits for CE0: 0x0 – WAIT[0] is used. 0x0 – WAIT[1] is used. 0x0 – Reserved. 0x0 – Reserved.

Table 4-3 Async Wait Cycle Config Register (AWCCR) Details (Part 2 of 2)

Bit	Field	Reset Value	Description
15-8	Reserved	0x0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
7-0	MAX_EXT_WAIT	0x80	Maximum extended wait cycles. EMIF16 will wait for (MAX_EXT_WAIT + 1) x 16 cycles before an extended asynchronous cycles is terminated.
End of Table 4-3			

4.4 Async 1 Config Register (A1CR)

The Async 1 Config Register (A1CR) (Figure 4-3) contains fields that program the setup, strobe and hold times for reads and writes to CE0. It also allows for programming the turnaround time between accesses and page size for page mode reads.

Figure 4-3 Async 1 Config Register (A1CR)

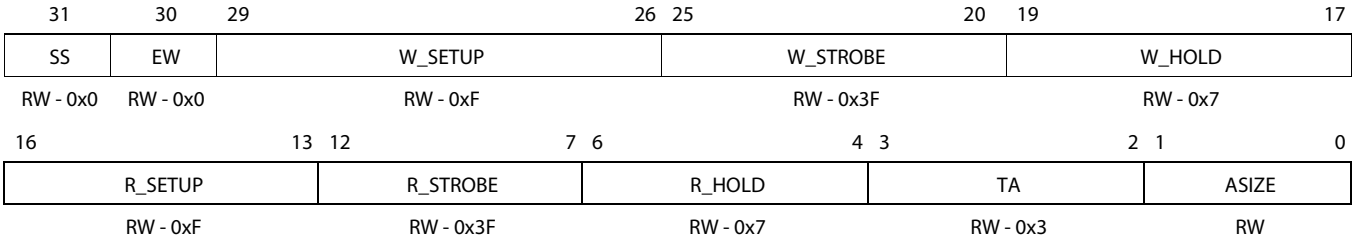

Table 4-4 Async 1 Config Register (A1CR) Details (Part 1 of 2)

Bit	Field	Reset Value	Description
31	SS	0x0	Select Strobe mode. 0x0 – Disable Select Strobe mode 0x1 – Enable Select Strobe mode.
30	EW	0x0	Extended Wait Mode 0 – Disable extended wait mode 1 – Enable extended wait mode on WAIT pins
29-26	W_SETUP	0xF	Write Strobe Setup cycles. Number of EMIF16 clock cycles from EMIFA[23:0],EMIFD[15:0], $\overline{\text{EMIFBE}}$[1:0] and $\overline{\text{CE}}$ being set, to $\overline{\text{EMIFWE}}$ asserted, minus one cycle. The reset value is 16 cycles.
25-20	W_STROBE	0x3F	Write Strobe Duration cycles. Number of EMIF16 clock cycles for which $\overline{\text{EMIFWE}}$ is held active, minus one cycle. The reset value is 64 cycles. This field cannot be zero when EW = 1.
19-17	W_HOLD	0x7	Write Strobe Hold cycles. Number of EMIF16 clock cycles for which EMIFA[23:0], EMIFD[15:0], $\overline{\text{EMIFBE}}$[1:0] and $\overline{\text{CE}}$ are held valid after $\overline{\text{EMIFWE}}$ has been deasserted, minus one cycle. The reset value is 8 cycles.
16-13	R_SETUP	0xF	Read Strobe Setup cycles. Number of EMIF16 clock cycles from EMIFA[23:0], $\overline{\text{EMIFBE}}$[1:0] and $\overline{\text{CE}}$ being set to $\overline{\text{EMIFOE}}$ asserted, minus one cycle. The reset value is 16 cycles.
12-7	R_STROBE	0x3F	Read Strobe Duration cycles. Number of EMIF16 clock cycles for which $\overline{\text{EMIFOE}}$ is held active, minus one cycle. The reset value is 64 cycles. This field cannot be zero when EW = 1.
6-4	R_HOLD	0x7	Read Strobe Hold cycles. Number of EMIF16 clock cycles for which EMIFA[23:0], $\overline{\text{EMIFBE}}$[1:0] and $\overline{\text{CE}}$ are held valid after $\overline{\text{EMIFOE}}$ has been deasserted, minus one cycle. The reset value is 8 cycles.

Table 4-4 Async 1 Config Register (A1CR) Details (Part 2 of 2)

Bit	Field	Reset Value	Description
3-2	TA	0x3	Turn Around cycles. Number of EMIF16 clock cycles between the end of one asynchronous memory access and the start of another asynchronous memory access, minus one cycle. This delay is not incurred between a read followed by a read, or a write followed by a write to the same chip select. The reset value is 4 cycles.
1-0	ASIZE		Asynchronous Memory Size. Defines the width of the data bus. 0 – 8-bit data bus 1 – 16-bit data bus 2,3 – Reserved
End of Table 4-4			

4.5 Async 2 Config Register (A2CR)

Bit fields and their operation are exactly the same as A1CR, except that programmed values will be applied for CE1.

4.6 Async 3 Config Register (A3CR)

Bit fields and their operation are exactly the same as A1CR, except that programmed values will be applied for CE2.

4.7 Async 4 Config Register (A4CR)

Bit fields and their operation are exactly the same as A1CR, except that programmed values will be applied for CE3.

4.8 Interrupt Raw Register (IRR)

The interrupt bits in the Interrupt Raw Register are set after the corresponding interrupt condition occurs, regardless of whether the interrupt has been enabled or disabled. The IRR is shown in Figure 4-4 and Table 4-5.

Figure 4-4 Interrupt Raw Register (IRR)

31	6	5	2	1	0
Reserved		WR		Reserved	AT
R - 0x0		RW - 0x0		R - 0x0	RW - 0x0

Table 4-5 Interrupt Raw Register (IRR) Details

Bit	Field	Reset Value	Description
31-6	Reserved	0x0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect
5-2	WR	0x0	Wait Rise. Set to 1 by hardware to indicate rising edge on the corresponding EMIFWAIT pin has been detected. The WP0-1 bits in the Async Wait Cycle Config register have no effect on these bits. Writing a 1 will clear these bits as well as the WR_MASKED bits in the Interrupt Masked register. Writing a 0 has no effect.
1	Reserved	0x0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect
0	AT	0x0	Asynchronous Timeout. Set to 1 by hardware to indicate that during an extended asynchronous memory access cycle, the WAIT signal did not go inactive within the number of cycles defined by the MAX_EXT_WAIT field in Async Wait Cycle Config register. Writing a 1 will clear this bit as well as the AT_MASKED bit in the Interrupt Masked register. Writing a 0 has no effect.
End of Table 4-5			

4.9 Interrupt Masked Register (IMR)

The Interrupt Masked Register (IMR) is shown in Figure 4-5 and Table 4-6.

Figure 4-5 Interrupt Masked Register (IMR)

31 6	5 2	1	0
Reserved	WR_MASKED	Reserved	AT_MASKED
R - 0x0	RW - 0x0	R - 0x0	RW - 0x0

Table 4-6 Interrupt Masked Register (IMR) Details

Bit	Field	Reset Value	Description
31-6	Reserved	0x0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect
5-2	WR_MASKED	0x0	Masked Wait Rise. Set to 1 by hardware to indicate rising edge on the corresponding WAIT pin has been detected only if WR_MASK_SET bit has been set in Interrupt Mask Set Register. The WP0-1 bits in the Async Wait Cycle Config register have no effect on these bits. Writing a 1 will clear these bits as well as the WR bits in the Interrupt Raw register. Writing a 0 has no effect.
1	Reserved	0x0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect
0	AT_MASKED	0x0	Masked Asynchronous Timeout. Set to 1 by hardware to indicate that during an extended asynchronous memory access cycle, the WAIT signal did not go inactive within the number of cycles defined by the MAX_EXT_WAIT field in Async Wait Cycle Config register, only if AT_MASK_SET is set in Interrupt Mask Set Register. Writing a 1 will clear this bit as well as the AT bit in the Interrupt Raw register. Writing a 0 has no effect.
End of Table 4-6			

4.10 Interrupt Mask Set Register (IMSR)

The Interrupt Mask Set Register (IMSR) is shown in Figure 4-6 and Table 4-7.

Figure 4-6 Interrupt Mask Set Register (IMSR)

31 6	5 2	1	0
Reserved	WR_MASK_SET	Reserved	AT_MASK_SET
R - 0x0	RW - 0x0	R - 0x0	RW - 0x0

Table 4-7 Interrupt Mask Set Register (IMSR) Details

Bit	Field	Reset Value	Description
31-6	Reserved	0x0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect
5-2	WR_MASK_SET	0x0	Mask set for WR_MASKED bits in the Interrupt Masked Register. Writing a 1 will enable the interrupts, and set these bits as well as the WR_MASK_CLR bits in the Interrupt Mask Clear register. Writing a 0 has no effect.
1	Reserved	0x0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect
0	AT_MASK_SET	0x0	Mask set for AT_MASKED bit in the Interrupt Masked Register. Writing a 1 will enable the interrupt, and set this bit as well as the AT_MASK_CLR bit in the Interrupt Mask Clear register. Writing a 0 has no effect.
End of Table 4-7			

4.11 Interrupt Mask Clear Register (IMCR)

The Interrupt Mask Clear Register (IMCR) is shown in Figure 4-7 and Table 4-8.

Figure 4-7 Interrupt Mask Clear Register (IMCR)

31 6	5 2	1	0
Reserved	WR_MASK_CLR	Reserved	AT_MASK_CLR
R - 0x0	RW - 0x0	R - 0x0	RW - 0x0

Table 4-8 Interrupt Mask Clear Register (IMCR) Details

Bit	Field	Reset Value	Description
31-6	Reserved	0x0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect
5-2	WR_MASK_CLR	0x0	Mask clear for WR_MASKED bits in the Interrupt Masked Register. Writing a 1 will disable the interrupts, and set these bits as well as the WR_MASK_SET bits in the Interrupt Mask Set register. Writing a 0 has no effect.
1	Reserved	0x0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect
0	AT_MASK_CLR	0x0	Mask clear for AT_MASKED bit in the Interrupt Masked Register. Writing a 1 will disable the interrupt, and set this bit as well as the AT_MASK_SET bit in the Interrupt Mask Set register. Writing a 0 has no effect.
End of Table 4-8			

4.12 NAND Flash Control Register (NANDFCR)

The NANDFCR register is shown in Figure 4-8 and described in Table 4-9.

Figure 4-8 NAND Flash Control Register (NANDFCR)

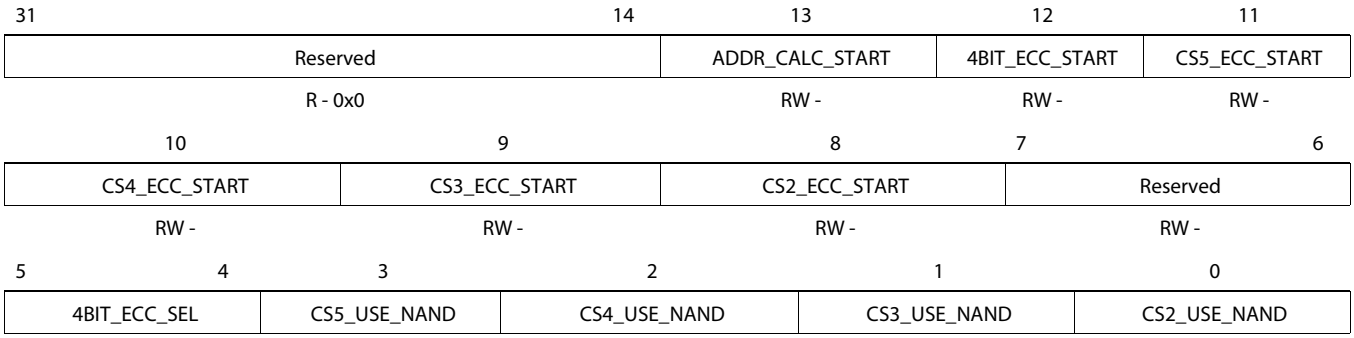

Table 4-9 NAND Flash Control Register (NANDFCR) Details (Part 1 of 2)

Bit	Field	Reset Value	Description
31-14	Reserved	0x0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect
13	ADDR_CALC_START	0x0	NAND Flash 4-bit ECC error address and error value calculation start. Set to 1 to start 4-bit ECC error address and error value calculation on read syndrome. This bit is cleared when any of the NAND Flash Error Address registers or NAND Flash Error Value registers are read. Writing a 0 has no effect.
12	4BIT_ECC_START	0x0	NAND Flash 4-bit ECC start for the selected chip select. Set to 1 to start 4-bit ECC calculation on data for NAND Flash on chip select selected by 4BIT_ECC_SEL. This bit is cleared when any of the NAND Flash 4-Bit ECC registers are read. Writing a 0 has no effect.
11	CS5_ECC_START	0x0	NAND Flash 1-bit ECC start for chip select CE3. Set to 1 to start 1-bit ECC calculation on data for NAND Flash on CE3. This bit is cleared when NAND Flash CS5 1-Bit ECC register is read. Writing a 0 has no effect.
10	CS4_ECC_START	0x0	NAND Flash 1-bit ECC start for chip select CE2. Set to 1 to start 1-bit ECC calculation on data for NAND Flash on CE2. This bit is cleared when NAND Flash CS4 1-Bit ECC register is read. Writing a 0 has no effect.
9	CS3_ECC_START	0x0	NAND Flash 1-bit ECC start for chip select CE1. Set to 1 to start 1-bit ECC calculation on data for NAND Flash on CE1. This bit is cleared when NAND Flash CS3 1-Bit ECC register is read. Writing a 0 has no effect.
8	CS2_ECC_START	0x0	NAND Flash 1-bit ECC start for chip select CE0. Set to 1 to start 1-bit ECC calculation on data for NAND Flash on CE0. This bit is cleared when NAND Flash CS2 (CE0) 1-Bit ECC register is read. Writing a 0 has no effect.
7-6	Reserved	0x0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect

Table 4-9 NAND Flash Control Register (NANDFCR) Details (Part 2 of 2)

Bit	Field	Reset Value	Description
5-4	4BIT_ECC_SEL	0x0	NAND Flash 4-bit ECC chip select selection. This field selects the chip select on which the 4-bit ECC will be calculated. 0x0 - Selects chip select CE0. 0x1 - Selects chip select CE1. 0x2 - Selects chip select CE2. 0x3 - Selects chip select CE3.
3	CS5_USE_NAND	0x0	NAND Flash mode for chip select CE3. Set to 1 if using NAND Flash on CE3.
2	CS4_USE_NAND	0x0	NAND Flash mode for chip select CE2. Set to 1 if using NAND Flash on CE2.
1	CS3_USE_NAND	0x0	NAND Flash mode for chip select CE1. Set to 1 if using NAND Flash on CE1.
0	CS1_USE_NAND	0x0	NAND Flash mode for chip select CE0. Set to 1 if using NAND Flash on CE0
End of Table 4-9			

4.13 NAND Flash Status Register (NANDFSR)

The NAND Flash Status Register is shown in Figure 4-9 and described in Table 4-10.

Figure 4-9 NAND Flash Status Register (NANDFSR)

31 18	17 16	15 12
Reserved	ERR_NUM	Reserved
R - 0x0	R - 0x0	R - 0x0

11 8	7 4	3 0
CORR_State	Reserved	WAIT_STATE
R - 0x0	RW - 0x0	R - 0x0

Table 4-10 NAND Flash Status Register (NANDFSR) Details

Bit	Field	Reset Value	Description
31-18	Reserved	0x0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
17-16	ERR_NUM	0x0	4-bit ECC error number. This field shows the number for errors found after the error address calculation and error value calculation is done. 0x0 – 1 error found. 0x1 – 2 errors found. 0x2 – 3 errors found. 0x3 – 4 errors found.
15-12	Reserved	0x0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
11-8	CORR_STATE	0x0	4-bit ECC state value when performing error address and error value calculation. 0x0 – No error. 0x1 – Errors cannot be corrected (five or more errors). The number of errors calculated (ERR_NUM field) differs from the number of errors searched. 0x2 – Error correction complete (errors on bit 8 or 9). 0x3 – Error correction complete (error exists). 0x4 – Reserved. 0x5 – Calculating number of errors. 0x6 and 0x7 – Preparing for error search. 0x8 – Searching for errors. 0x9, 0xA, and 0xB – Reserved. 0xC, 0xD, 0xE, and 0xF – Calculating error value.
7-4	Reserved	0x0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
3-0	WAIT_STAT		These bits show the raw status of the EMIFWAIT[1:0] input. The WP1-0 bits in the Async Wait Cycle Config register have no effect on these bits.
End of Table 4-10			

4.14 Page Mode Control Register (PMCR)

The Page Mode Control Register is shown in Figure 4-10 and described in Table 4-11.

Figure 4-10 Page Mode Control Register (PMCR)

31 26	25 24	23 18	
CS5_PG_DEL	CS5_PG_SIZE	CS5_PG_MD_EN	CS4_PG_DEL
RW - 0x3F	RW	RW	RW - 0x3F
17	**16**	**15 10**	**9**
CS4_PG_SIZE	CS4_PG_MD_EN	CS3_PG_DEL	CS3_PG_SIZE
RW	RW	RW - 0x3F	RW
8	**7 2**	**1**	**0**
CS3_PG_MD_EN	CS2_PG_DEL	CS2_PG_SIZE	CS2_PG_MD_EN
RW	RW - 0x3F	RW	RW

Table 4-11 Page Mode Control Register (PMCR) Details (Part 1 of 2)

Bit	Field	Reset Value	Description
31-26	CS5_PG_DEL	0x3F	Page access delay for NOR Flash connected on CE3. Number of EMIF16 clock cycles required for the page read data to be valid, minus one cycle. This value must not be set to 0.
25	CS5_PG_SIZE		Page Size for NOR Flash connected on CE3. 0x1 – 8 word page. 0x0 – 4 word page.
24	CS5_PG_MD_EN		Page Mode enable for NOR Flash connected on CE3. 0x1 – Use page mode. 0x0 – Disable page mode.
23-18	CS4_PG_DEL	0x3F	Page access delay for NOR Flash connected on CE2. Number of EMIF16 clock cycles required for the page read data to be valid, minus one cycle. This value must not be set to 0.
17	CS4_PG_SIZE		Page Size for NOR Flash connected on CE2. 0x1 – 8 word page. 0x0 – 4 word page.
16	CS4_PG_MD_EN		Page Mode enable for NOR Flash connected on CE2. 0x1 – Use page mode. 0x0 – Disable page mode.
15-10	CS3_PG_DEL	0x3F	Page access delay for NOR Flash connected on CE1. Number of EMIF16 clock cycles required for the page read data to be valid, minus one cycle. This value must not be set to 0.
9	CS3_PG_SIZE		Page Size for NOR Flash connected on CE1. 0x1 – 8 word page. 0x0 – 4 word page.
8	CS3_PG_MD_EN		Page Mode enable for NOR Flash connected on CE1. 0x1 – Use page mode. 0x0 – Disable page mode.
7-2	CS2_PG_DEL	0x3F	Page access delay for NOR Flash connected on CE0. Number of EMIF16 clock cycles required for the page read data to be valid, minus one cycle. This value must not be set to 0.

Table 4-11 Page Mode Control Register (PMCR) Details (Part 2 of 2)

Bit	Field	Reset Value	Description
1	CS2_PG_SIZE		Page Size for NOR Flash connected on CE0. 0x1 – 8 word page. 0x0 – 4 word page.
0	CS2_PG_MD_EN		Page Mode enable for NOR Flash connected on CE0. 0x1 – Use page mode. 0x0 – Disable page mode.
End of Table 4-11			

4.15 NAND Flash CS2 (CE0) 1-Bit ECC Register (NFECCCS2R)

The NAND Flash CS2 1-Bit ECC Register is used for NAND Flash connected to CE0. It is shown in Figure 4-11 and described in Table 4-12.

Figure 4-11 NAND Flash CS2 (CE0) 1-Bit ECC Register (NFECCCS2R)

31 28	27	26	25	24	23	22	21	20
Reserved	p2048o	P1024o	P512o	P256o	P128o	P64o	P32o	P16o
R - 0x0	R - 0x0	R - 0x0	R - 0x0	R - 0x0	R - 0x0	R - 0x0	R - 0x0	R - 0x0
19	18	17	16	15 12	11	10	9	8
p8o	p4o	p2o	p1o	Reserved	p2048o	P1024o	P512o	P256o
R - 0x0	R - 0x0	R - 0x0	R - 0x0	R - 0x0	R - 0x0	R - 0x0	R - 0x0	R - 0x0
7	6	5	4	3	2	1	0	
P128o	P64o	P32o	P16o	p8o	p4o	p2o	p1o	
R - 0x0	R - 0x0	R - 0x0	R - 0x0	R - 0x0	R - 0x0	R - 0x0	R - 0x0	

Table 4-12 NAND Flash CS2 (CE0) 1-Bit ECC Register (NFECCCS2R) Details

Bit	Field	Reset Value	Description
31-28	Reserved	0x0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
27	p2048o	0x0	1-Bit ECC code calculated while reading/writing NAND Flash.
26	p1024o	0x0	
25	p512o	0x0	For 8-bit NAND Flash, p1o, p2o and p4o are column parities. p8o to p2048o are row parities.
24	p256o	0x0	
23	p128o	0x0	
22	p64o	0x0	
21	p32o	0x0	
20	p16o	0x0	
19	p8o	0x0	For 16-bit NAND Flash, p1o, p2o, p4o and p8o are column parities. p16o to p2048o are row parities.
18	p4o	0x0	
17	p2o	0x0	
16	p1o	0x0	
15-12	Reserved	0x0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
11	p2048e	0x0	1-Bit ECC code calculated while reading/writing NAND Flash.
10	p1024e	0x0	
9	p512e	0x0	For 8-bit NAND Flash, p1e, p2e and p4e are column parities. p8e to p2048e are row parities.
8	p256e	0x0	
7	p128e	0x0	
6	p64e	0x0	
5	p32e	0x0	
4	p16e	0x0	For 16-bit NAND Flash, p1e, p2e, p4e and p8e are column parities. p16e to p2048e are row parities.
3	p8e	0x0	
2	p4e	0x0	
1	p2e	0x0	
0	p1e	0x0	
End of Table 4-12			

4.16 NAND Flash CS3 (CE1) 1-Bit ECC Register (NFECCCS3R)

The NAND Flash CS3 1-Bit ECC Register is exactly the same as NAND Flash CS2 1-Bit ECC Register, only difference being the former is used for device on CE1.

4.17 NAND Flash CS4 (CE2) 1-Bit ECC Register (NFECCCS4R)

The NAND Flash CS4 1-Bit ECC Register is exactly the same as NAND Flash CS2 1-Bit ECC Register, only difference being the former is used for device on CE2.

4.18 NAND Flash CS5 (CE3) 1-Bit ECC Register (NFECCCS5R)

The NAND Flash CS5 1-Bit ECC Register is exactly the same as NAND Flash CS2 1-Bit ECC Register, only difference being the former is used for device on CE3.

4.19 NAND Flash 4-Bit ECC Load Register (NANDF4BECCLR)

The NAND Flash 4-Bit ECC Load Register is shown in Figure 4-12 and described in Table 4-13.

Figure 4-12 NAND Flash 4-Bit ECC Load Register (NANDF4BECCLR)

31	10	9	0
Reserved		4BIT_ECC_LOAD	
R - 0x0		RW - 0x0	

Table 4-13 NAND Flash 4-Bit ECC Load Register (NANDF4BECCLR) Details

Bit	Field	Reset Value	Description
31-10	Reserved	0x0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect
9-0	4BIT_ECC_LOAD	0x0	4-Bit ECC Load. This register is used to load 4-bit ECC values when performing syndrome calculation during NAND Flash reads.
End of Table 4-13			

4.20 NAND Flash 4-Bit ECC 1 Register (NANDF4BECC1R)

The NAND Flash 4-Bit ECC 1 register is shown in Figure 4-13 and described in Table 4-14.

Figure 4-13 NAND Flash 4-Bit ECC 1 Register (NANDF4BECC1R)

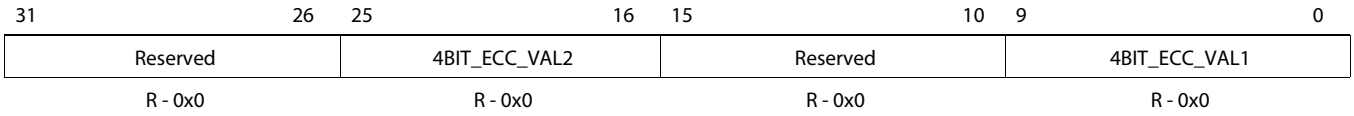

Table 4-14 NAND Flash 4-Bit ECC 1 Register (NANDF4BECC1R) Details

Bit	Field	Value	Description
31-26	Reserved	0x0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect
25-16	4BIT_ECC_VAL2	0x0	4-Bit ECC or syndrome value 2 calculated while writing or reading NAND Flash.
15-10	Reserved	0x0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect
9-0	4BIT_ECC_VAL1	0x0	4-Bit ECC or syndrome value 1 calculated while writing or reading NAND Flash.
End of Table 4-14			

4.21 NAND Flash 4-Bit ECC 2 Register (NANDF4BECC2R)

The NAND Flash 4-Bit ECC 2 register is shown in Figure 4-14 and described in Table 4-15.

Figure 4-14 NAND Flash 4-Bit ECC 2 Register (NANDF4BECC2R)

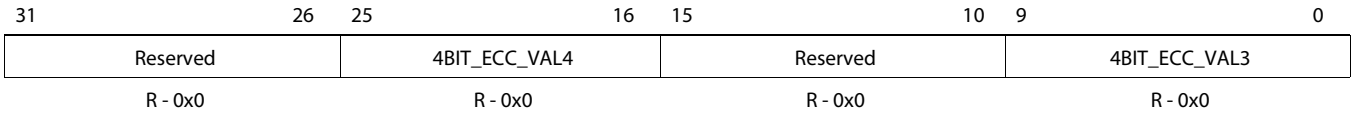

Table 4-15 NAND Flash 4-Bit ECC 2 Register (NANDF4BECC2R) Details

Bit	Field	Value	Description
31-26	Reserved	0x0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect
25-16	4BIT_ECC_VAL4	0x0	4-Bit ECC or syndrome value 4 calculated while writing or reading NAND Flash.
15-10	Reserved	0x0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect
9-0	4BIT_ECC_VAL3	0x0	4-Bit ECC or syndrome value 3 calculated while writing or reading NAND Flash.
End of Table 4-15			

4.22 NAND Flash 4-Bit ECC 3 Register (NANDF4BECC3R)

The NAND Flash 4-Bit ECC 3 register is shown in Figure 4-15 and described in Table 4-16.

Figure 4-15 NAND Flash 4-Bit ECC 3 Register (NANDF4BECC3R)

31 26	25 16	15 10	9 0
Reserved	4BIT_ECC_VAL6	Reserved	4BIT_ECC_VAL5
R - 0x0	R - 0x0	R - 0x0	R - 0x0

Table 4-16 NAND Flash 4-Bit ECC 3 Register (NANDF4BECC3R) Details

Bit	Field	Value	Description
31-26	Reserved	0x0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect
25-16	4BIT_ECC_VAL6	0x0	4-Bit ECC or syndrome value 6 calculated while writing or reading NAND Flash.
15-10	Reserved	0x0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect
9-0	4BIT_ECC_VAL5	0x0	4-Bit ECC or syndrome value 5 calculated while writing or reading NAND Flash.
End of Table 4-16			

4.23 NAND Flash 4-Bit ECC 4 Register (NANDF4BECC4R)

The NAND Flash 4-Bit ECC 4 register is shown in Figure 4-16 and described in Table 4-17.

Figure 4-16 NAND Flash 4-Bit ECC 4 Register (NANDF4BECC4R)

31 26	25 16	15 10	9 0
Reserved	4BIT_ECC_VAL8	Reserved	4BIT_ECC_VAL7
R - 0x0	R - 0x0	R - 0x0	R - 0x0

Table 4-17 NAND Flash 4-Bit ECC 4 Register (NANDF4BECC4R) Details

Bit	Field	Value	Description
31-26	Reserved	0x0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect
25-16	4BIT_ECC_VAL8	0x0	4-Bit ECC or syndrome value 8 calculated while writing or reading NAND Flash.
15-10	Reserved	0x0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect
9-0	4BIT_ECC_VAL7	0x0	4-Bit ECC or syndrome value 7 calculated while writing or reading NAND Flash.
End of Table 4-17			

4.24 NAND Flash Error Address 1 Register (NANDFEA1R)

The NAND Flash Error Address 1 register is shown in Figure 4-17 and described in Table 4-18.

Figure 4-17 NAND Flash Error Address 1 Register (NANDFEA1R)

31 26	25 16	15 10	9 0
Reserved	ERR_ADDR2	Reserved	ERR_ADDR1
R - 0x0	R - 0x0	R - 0x0	R - 0x0

Table 4-18 NAND Flash Error Address 1 Register (NANDFEA1R) Details

Bit	Field	Value	Description
31-26	Reserved	0x0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect
25-16	ERR_ADDR2	0x0	4-Bit error address 2.
15-10	Reserved	0x0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect
9-0	ERR_ADDR1	0x0	4-Bit error address 1.
End of Table 4-18			

4.25 NAND Flash Error Address 2 Register (NANDFEA2R)

The NAND Flash Error Address 2 register is shown in Figure 4-18 and described in Table 4-19.

Figure 4-18 NAND Flash Error Address 2 Register (NANDFEA2R)

31 26	25 16	15 10	9 0
Reserved	ERR_ADDR4	Reserved	ERR_ADDR3
R - 0x0	R - 0x0	R - 0x0	R - 0x0

Table 4-19 NAND Flash Error Address 2 Register (NANDFEA2R) Details

Bit	Field	Value	Description
31-26	Reserved	0x0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect
25-16	ERR_ADDR4	0x0	4-Bit error address 4.
15-10	Reserved	0x0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect
9-0	ERR_ADDR3	0x0	4-Bit error address 3.
End of Table 4-19			

4.26 NAND Flash Error Value 1 Register (NANDFEV1R)

The NAND Flash Error Value 1 register is shown in Figure 4-19 and described in Table 4-20.

Figure 4-19 NAND Flash Error Value 1 Register (NANDFEV1R)

31 26	25 16	15 10	9 0
Reserved	ERR_VAL2	Reserved	ERR_VAL1
R - 0x0	R - 0x0	R - 0x0	R - 0x0

Table 4-20 NAND Flash Error Value 1 Register (NANDFEV1R) Details

Bit	Field	Value	Description
31-26	Reserved	0x0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect
25-16	ERR_VAL2	0x0	4-Bit error value 2.
15-10	Reserved	0x0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect
9-0	ERR_VAL1	0x0	4-Bit error value 1.
End of Table 4-20			

4.27 NAND Flash Error Value 2 Register (NANDFEV2R)

The NAND Flash Error Value 2 register is shown in Figure 4-20 and described in Table 4-21.

Figure 4-20 NAND Flash Error Value 2 Register (NANDFEV2R)

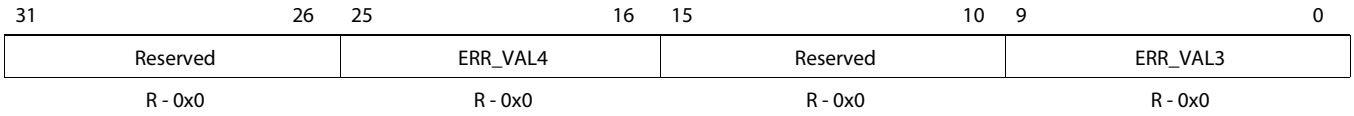

Table 4-21 NAND Flash Error Value 2 Register (NANDFEV2R) Details

Bit	Field	Value	Description
31-26	Reserved	0x0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect
25-16	ERR_VAL4	0x0	4-Bit error value 4.
15-10	Reserved	0x0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect
9-0	ERR_VAL3	0x0	4-Bit error value 3.
End of Table 4-21			

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