KeyStone Architecture
Power Sleep Controller (PSC)

User's Guide

Literature Number: SPRUGV4C
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Preface

About This Manual

This document describes the functionality, operational details, and programming information for the Power Sleep Controller (PSC) module in KeyStone architecture devices.

Notational Conventions

This document uses the following conventions:

- Commands and keywords are in **boldface** font.
- Arguments for which you supply values are in *italic* font.
- Terminal sessions and information the system displays are in screen font.
- Information you must enter is in **boldface screen font**.
- Elements in square brackets ([ ]) are optional.

Notes use the following conventions:

NOTE: Means reader take note. Notes contain helpful suggestions or references to material not covered in the publication.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

CAUTION

Indicates the possibility of service interruption if precautions are not taken.

WARNING

Indicates the possibility of damage to equipment if precautions are not taken.

Related Documentation from Texas Instruments

C66x CorePac User Guide	SPRUGW0
C66x CPU and Instruction Set Reference Guide	SPRUGH7
Hardware Design Guide for KeyStone Devices	SPRABI2

Introduction

NOTE: The information in this document should be used in conjunction with information in the device-specific Keystone Architecture data manual that applies to the part number of your device.

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1.1 Purpose of the Peripheral

The purpose of the Power Sleep Controller (PSC) is to reduce power when a module is not being utilized. The PSC is responsible for controlling device power by turning off unused power domains or gating off clocks to individual modules. The PSC provides the user with an interface to control several important power and clock operations. These operations are the focus of this document.

1.2 Terminology Used in This Document

Term	Definition
DSP	Digital Signal Processor
GPSC	Global Power/Sleep Controller; manages the LPSCs
LPSC	Local Power/Sleep Controller; one per module
PSC	Power/Sleep Controller, including one GPSC and multiple LPSCs

1.3 Features

The PSC includes the following features:

- Provides software interface to:
  - Control module power on/off
  - Control module clock on/off
  - Control C66x local resets
- Supports emulation features: power, clock, and reset

Architecture

This chapter describes the architecture details of the Power/Sleep Controller.

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2.1 Power and Clock Domains

The KeyStone devices have several power domains to enable minimizing power dissipation for unused logic on the device. The Global Power/Sleep Controller (GPSC) is used to control the power gating of various power domains.

In addition, clock gating to each of the logic blocks is managed by the Local Power/Sleep Controllers (LPSCs) of each module. For modules with a dedicated clock or multiple clocks, the LPSC communicates with the PLL controller to enable and disable that module's clock(s) at the source. For modules that share a clock with other modules, the LPSC controls the clock gating.

Many modules reside in the AlwaysOn domain that always has power and clocks provided. These consist primarily of the infrastructure components that are responsible for the clock and reset control (PLL Controller and PSC), the switch fabric that connects all of the modules, and modules that do not need dynamic enable/disable because they do not consume a significant amount of power.

For power domain and clock domain assignments, refer to the data manual for your particular KeyStone device.

2.2 Power Domain and Module States Defined

The PSC module organizes modules into different power domains and into different modules (clock domains). Note that there is no relationship between a power domain and a module. These are completely separate entities and may be controlled separately.

2.2.1 Power Domain States

A power domain can be in only one of two states: ON or OFF, defined as follows:

- **ON:** Power to the power domain is on. Logic / memories are awake.
- **OFF:** Power to the power domain is off. Logic / memories are turned off.

The AlwaysOn power domain is always in the ON state when the device is powered on. The other power domains can be in either the ON or OFF state; i.e., the logic / memory for a specific module can remain powered down if it is not used.

2.2.2 Module States

A module can be in one of two states: Enable or SwRstDisable. As shown in Table 2-1, these two states correspond to combinations of module reset asserted or de-asserted and module clock on or off. Note that module reset is defined to completely reset a given module, such that all hardware is put back into its default state.

Table 2-1. Module States

Module State	Module Reset	Module Clock
Enable	De-asserted	ON
SwRstDisable	Asserted	OFF

The module states are defined as follows:

- **Enable:** A module in the Enable state has its module reset de-asserted and its clock on. This is the normal run-time state for a given module.
- **SwRstDisable:** A module in the SwResetDisable state has its module reset asserted and its clock OFF.

2.2.3 Local Reset

In addition to module reset described in the previous section, the C66x core can be reset using a special local reset. When local reset is asserted, the internal memories (L1P, L1D, and L2) for the core are still accessible. The local reset resets only the corresponding C66x core, not the rest of the chip. Local reset is intended to be used by the watchdog timers to reset the C66x core in the event of an error. The procedures for asserting and de-asserting local reset are as follows (Y denotes the module domain number):

1. Set **MDCTL[Y].LRSTZ** to 0x0 to assert local reset.
2. Set **MDCTL[Y].LRSTZ** to 0x1 to de-assert local reset. The C66x core immediately executes program instructions after reset is de-asserted. Note that the boot sequence does not re-occur unless there is a device-level reset. Execution of code previously in L2 begins execution.

2.3 Executing State Transitions

This section describes how to execute state transitions for power domains and modules. Examples show how to enable only power domains, only modules, or a combination. Although the user has complete control of the sequencing, see Section 2.3.4 for recommendations.

2.3.1 Power Domain State Transitions

This section describes the basic procedure for transitioning the state of a power domain.

NOTE: As mentioned previously, there are multiple power domains in the device. The AlwaysOn power domain is always in the ON state when the device is powered-on, and therefore it is not possible to transition this domain to the OFF state. Conversely, the other domains are in the OFF or ON state when the device is powered-on. Transitions between ON and OFF states need to follow the procedure below. Please refer to device specific data manual and peripheral user's guide for any other considerations especially while turning off the power domain.

The procedure for power domain state transitions follows (X denotes the power domain number, Y denotes the module domain number):

1. Wait for **PTSTAT.GOSTAT[X]** to clear to 0x0. Wait for any previously initiated transitions to finish before initiating a new transition.
2. Set **PDCTL[X].NEXT** for an ON (0x1) or OFF (0x0) transition. Note: When **PTCMD.GO[X]** is set to 0x1 in the next step, the **PDCTL[X].NEXT** field of this power domain and the **MDCTL[Y].NEXT** field of the module in this power domain are evaluated. Therefore, you may set the **MDCTL[Y].NEXT** field for multiple modules before executing this step.
3. Set **PTCMD.GO[X]** to 0x1 to initiate the state transition(s). The PSC turns on or off the logic / memory for that particular domain.
4. Wait for **PTSTAT.GOSTAT[X]** to clear to 0x0. The domain is safely in the new state only after **PTSTAT.GOSTAT[X]** is cleared to 0x0.

2.3.2 Module State Transitions

This section describes the procedure for transitioning the module state.

NOTE: The following procedure is applicable for all LPSC-controlled modules. To transition the module state, one must be aware of several system considerations. Transitions between Enable and Disable states need to follow the procedure below. Please refer to device specific data manual and peripheral user's guide for any other considerations especially while transitioning a module to Disable state. Also, before transitioning a module to Enable, if the logic / memories are not in the AlwaysOn power domain, they must be turned on before or in parallel with the transition. See Section 2.3.1.

The procedure for module state transitions follows (X denotes the power domain number, Y denotes the module domain number):

1. Wait for **PTSTAT.GOSTAT[X]** to clear to 0x0. Wait for any previously initiated transitions to finish before initiating a new transition.
2. Set **MDCTL[Y].NEXT** to Enable (0x3) or Disable (0x0). Note that you may set transitions in multiple **MDCTL[Y].NEXT** fields in this step as long as the corresponding power domain is on.
3. Set **PTCMD.GO[X]** to 0x1 to initiate the transition(s).
4. Wait for **PTSTAT.GOSTAT[X]** to clear to 0x0. The module is safely in the new state only after **PTSTAT.GOSTAT[X]** clears to 0x0.

2.3.3 Concurrent Power Domain/Module State Transitions

This section describes the basic procedure for transitioning the state of a power domain and module domain for modules that are not in the AlwaysOn domain. This may be done separately as described in the sections above, if desired.

The procedure for concurrent power domain/module state transitions follows (X denotes the power domain number, Y denotes the module domain number):

1. Wait for **PTSTAT.GOSTAT[X]** to clear to 0x0. Wait for any previously initiated transitions to finish before initiating a new transition.
2. Set **PDCTL[X].NEXT** for an ON (0x1) transition.
3. Set **MDCTL[Y].NEXT** to Enable (0x3). Note that you may set transitions in multiple **MDCTL.NEXT** fields in this step as long as the corresponding power domain is on.
4. Set **PTCMD.GO[X]** 0x1 to initiate the state transition(s). The PSC will turn on the logic / memory for that particular domain, starts the module clock, then de-asserts the module reset.
5. Wait for **PTSTAT.GOSTAT[X]** to clear to 0x0. The domain is safely in the new state only after **PTSTAT.GOSTAT[X]** is cleared to 0x0.

2.3.4 Recommendations for Power Domain/Module Sequencing

As noted in Section 2.2 and Section 2.3, a particular peripheral's power domain must be enabled before the module is enabled.

Unless there is a system-level reason to perform each function separately, the recommendation is to use the sequence listed in Section 2.2.3 rather than individual sequencing. Even though a single write to the appropriate GO bit starts the power domain and module transition, it is still sequenced such that the memory / logic is certain to turn on before the module is enabled. Thus, there is no ill effect in performing these together.

It is important to know that when a power domain is enabled, all logic / memories for that module are immediately turned on and moved to an active state. This means that there will be a spike in current consumption at that particular time. In other words, di/dt will be affected. To minimize the effect on di/dt of enabling power domains, it is recommended to power up modules one at a time. It is also recommended that all modules be initialized early in the application to avoid a large spike in di/dt during normal operation where the application may already be drawing a substantial amount of current from the supply.

2.4 Emulation Support in the PSC

The PSC supports commands that allow emulation tools to have some control over the state of power domains and modules.

In particular, the PSC supports the following emulation commands:

- Power on and enable features:
  - **Force Power:** Allows emulation to force the power domain into an ON state.
  - **Force Active:** Allows emulation to force the power domain into an ON state and force the module into the Enable state.
- Reset features:
  - **Assert Reset:** Allows emulation to assert the module's local reset.

- **Wait Reset:** Allows emulation to keep local reset asserted for an extended period of time after software initiates local reset de-assert.
- **Block Reset:** Allows emulation to block software initiated local and module resets.

Local reset applies only to the C66x core domains; module reset applies to all other domains.

Registers

This chapter details the PSC registers.

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3.1 Power and Sleep Controller (PSC) Register Map

For details of the PSC memory map and registers, refer to the data manual for your particular KeyStone device.

3.2 Register Descriptions

This section describes, in detail, the module registers with a register figure and a field description table for each. Each register figure identifies the bit field, the register name, read/write capability, and the default value.

3.2.1 Peripheral Identification Register (PID)

The peripheral identification register is shown in Figure 3-1 and described in Table 3-1.

Figure 3-1. Peripheral Identification Register (PID)

31	16	15	0
PID		PID	
R-4482h		R-y	

Legend: R = Read only; - *n* = value after reset; -y = device-specific

Table 3-1. Peripheral Identification Register (PID) Details

Bit	Field	Description
31-0	PID	Peripheral ID used to differentiate different modules in the system.

3.2.2 Voltage Control Identification Register (VCNTLID)

The voltage control identification register is shown in Figure 3-2 and described in Table 3-2.

This register captures the SmartReflex Class-0 VCNTL selection coming from EFUSE. For more details on SmartReflex and VCNTL mapping to the core voltage, see the *Hardware Design Guide for KeyStone Devices* in Related Documentation from Texas Instruments.

Figure 3-2. Voltage Control Identification Register (VCNTLID)

31 22	21 16	15 0
Reserved	VCNTL	Reserved
R-0	R-0	R-0

Legend: R = Read only; - *n* = value after reset

Table 3-2. Voltage Control Identification Register (VCNTLID) Details

Bit	Field	Description
31-22	Reserved	Reads return 0 and writes have no effect.
21-16	VCNTL	Reflects SmartReflex Class-0 VCNTL selection coming from EFUSE.
15-0	Reserved	Reads return 0 and writes have no effect.

3.2.3 Power Domain Transition Command Register (PTCMD)

The power domain transition command register is shown in Figure 3-3 and described in Table 3-3.

Figure 3-3. Power Domain Transition Command Register (PTCMD)

31	0
GO[X] (1)	
W-0	

Legend: R = Read only; W = Write only

(1) X denotes the power domain number. Power domain assignments varies by device. See the device specific data manual for details.

Table 3-3. Power Domain Transition Command Register (PTCMD) Details

Bit	Field	Value	Description
31-0	GO[X]	1	Power domain GO transition command (X denotes power domain number). Write 1 to cause the state transition interrupt generation block to evaluate the new PTNEXT and MDCTL.NEXT states as the application desired states.

3.2.4 Power Domain Transition Status Register (PTSTAT)

The power domain transition status register is shown in Figure 3-4 and described in Table 3-4.

Figure 3-4. Power Domain Transition Status Register (PTSTAT)

31	0
GOSTAT[X] (1)	
R-0	

Legend: R = Read only; W = Write only

(1) X denotes the power domain number. Power domain assignments varies by device. See the device specific data manual for details.

Table 3-4. Power Domain Transition Status Register (PTSTAT) Details

Bit	Field	Description
31-0	GOSTAT[X]	Power domain transition status (X denotes power domain number). • 0 = No transition in progress. • 1 = Power domain is transitioning (i.e., either the power domain is transitioning or modules in this power domain are transitioning).

3.2.5 Power Domain Status Register (PDSTATx)

The power domain status register is shown in Figure 3-5 and described in Table 3-5.

KeyStone devices contain PDSTAT0 to PDSTAT31 registers. Refer to the data manual for your specific part for details on which PDSTAT registers the part includes.

Figure 3-5. Power Domain Status Register (PDSTATx)

31 10	9 8	7 2	1 0
Reserved	Reserved	Reserved	STATE
R-0	R-1	R-0	R (1)

Legend: R = Read only; W = Write only; - *n* = value after reset

(1) Default value after reset: AlwaysOn domain -1; other domains -0.

Table 3-5. Power Domain Status Register (PDSTATx) Details

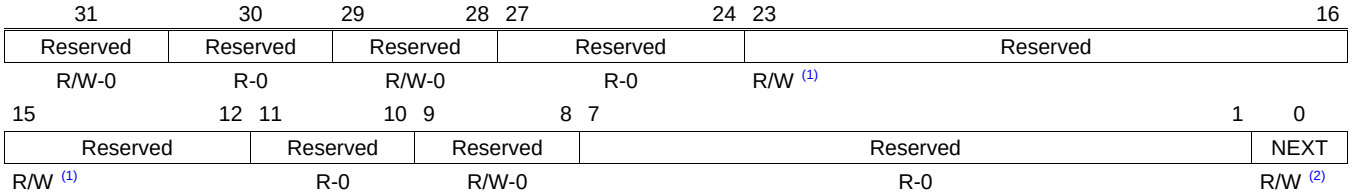
Bit	Field	Description
31-2	Reserved	Reserved.
1-0	STATE	Power domain status. • 0 = Power domain is in the OFF state. • 1 = Power domain is in the ON state.

3.2.6 Power Domain Control Register (PDCTLx)

The power domain control register is shown in Figure 3-6 and described in Table 3-6.

KeyStone devices contain PDCTL0 to PDCTL31 registers. Refer to the data manual for your specific part for details on which PDCTL registers the part includes.

Figure 3-6. Power Domain Control Register (PDCTLx)



Legend: R = Read only; W = Write only; - *n* = value after reset

(1) Default value after reset: AlwaysOn domain -0x01; other domains -0x33.
(1) Default value after reset: AlwaysOn domain -0xB; other domains -0x8.
(2) Default value after reset: AlwaysOn domain -1; other domains -0.

Table 3-6. Power Domain Control Register (PDCTLx) Details

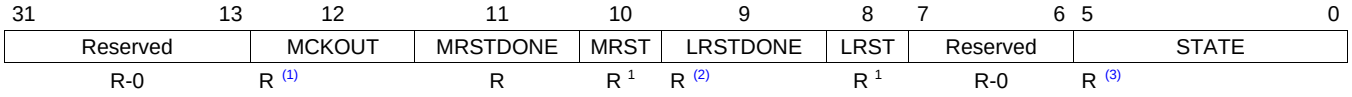
Bit	Field	Description
31-1	Reserved	Reserved.
0	NEXT	Power domain next state. • 0 = Power domain OFF. • 1 = Power domain ON.

3.2.7 Module Status Register (MDSTATy)

The module status register is shown in Figure 3-7 and described in Table 3-7.

KeyStone devices contain MDSTAT0 to MDSTAT31 registers. Refer to the data manual for your specific part for details on which MDSTAT registers the part includes.

Figure 3-7. Module Status Register (MDSTATy)



Legend: R = Read only; W = Write only; - *n* = value after reset

(1) Default value after reset: C66x domain and Never-Gated domain -1; other domains -0.
(2) Default value after reset: C66x domain -0; other domains -1.
(3) Default value after reset: C66x domain and Never-Gated domain -0x3; other domains -0.

Table 3-7. Module Status Register (MDSTATy) Details

Bit	Field	Description
31-13	Reserved	Reserved.
12	MCKOUT	Module clock output status. Shows status of module clock; on/off. • 0 = Module clock is off. • 1 = Module clock is on.
11	MRSTDONE	Module reset done. Software is responsible for checking that mode reset is done before accessing the module. • 0 = Module reset is not done. • 1 = Module reset is done.
10	MRST	Module reset status. Reflects actual state of module reset. • 0 = Module reset is asserted. • 1 = Module reset is de-asserted.
9	LRSTDONE	Local reset done. Software is responsible for checking that local reset is done before accessing this module. • 0 = Local reset is not done. • 1 = Local reset is done.
8	LRST	Module local reset status. (This bit applies to C66x domains only.) • 0 = Local reset is asserted. • 1 = Local reset is de-asserted.
7-6	Reserved	Reserved
5-0	STATE	Module state status. Indicates current module status. • 0x0 = SwRstDisable state. • 0x3 = Enable state. • Others = Reserved.

3.2.8 Module Control Register (MDCTLy)

The module control register is shown in Figure 3-8 and described in Table 3-8.

KeyStone devices contain MDCTL0 to MDCTL31 registers. Refer to the data manual for your specific part for details on which MDCTL registers the part includes.

Figure 3-8. Module Control Register (MDCTLy)

31	30 13	12	11 9	8	7 5	4 0
Reserved	Reserved	RESETISO	Reserved	LRST	Reserved	NEXT
R/W-0	R-0	R/W-0	R/W-0	R/W-1	R-0	R/W [1]

Legend: R = Read only; W = Write only; - *n* = value after reset

[1] Default value after reset: C66x domain and Never-Gated domain -0x3; other domains -0.

Table 3-8. Module Control Register (MDCTLy) Details

Bit	Field	Description
31-13	Reserved	Reserved.
12	RESETISO	Reset isolation. • 0 = No reset isolation • 1 = Enable reset isolation. LPSC will block global device resets and will not pause clocks during reset transitions. Applicable only for modules that support reset isolation. See the device data manual for a list of modules that support reset isolation. There may be additional requirements to enable reset isolation, see the device data manual for details.
11-9	Reserved	Reserved
8	LRST	Module local reset control. (This bit applies to C66x modules only.) • 0 = Assert local reset. • 1 = De-assert local reset.
7-5	Reserved	Reserved.
4-0	NEXT	Module next state. • 0x0 = SwRstDisable state. • 0x3 = Enable state. • Other = Reserved.

Revision History

Changes from B Revision (Nov 2011) to C Revision **Page**

- Changed from OFF to OFF or ON. 9
- Added "Transitions between ON and OFF states need to follow the procedure below. Please refer to device specific data manual and peripheral user's guide for any other considerations especially while turning off the power domain."..... 9
- Changed ON (0x1) to ON (0x1) or OFF (0x0). 9
- Changed "The PSC turns on..." to "The PSC turns on or off..."..... 9
- Updated Note. 9
- Added "...or Disable (0x0)" 10

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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